



Preliminary

MY9941

## 4 Channels Constant Current LED Driver With Cascade DMX512 Protocol and Differential Interface

### General Description

The MY9941, 4 channels constant current LED driver with 14bits grayscale APDM (Adaptive Pulse Density Modulation) control, supports standard/4x DMX512 protocol and fully differential interface suited for long distance cascade applications. The distinctive DMX512 decoding approach could decode precisely a standard DMX512 signal. And each device loads one/two/three/four grayscale data according to two slot selection pins. The differential interface provides wide common-mode range to support long distance transmission without common-ground power systems.

The device operates over 7V to 40V input voltage range and provides 4 open-drain constant current sinking outputs that are rated to 40V and delivers up to 350mA of high accuracy current to each string of LED. The current at each output is programmable by means of four external current setting resistors. The MY9941 provides the gamma correction, gamma value is 2.2, to transform 8bits DMX data to 14bits APDM data in order to enhance brightness contrast. The 14bits adaptive pulse density modulation makes sure that the frame refresh rate is higher than 2KHz. And an accurate oscillator is built in for free running APDM grayscale control and DMX512 decoder.

Furthermore, MY9941 also supports 4X DMX512 interface to enhance data refresh rate by four times. MY9941 could drive High Power LED directly by shorting the output channels and changing the slot data number. The POL function makes MY9941 as a PWM generator to support driving high power LEDs. MY9941 is available in SSOP24/TSSOP20 packages and specified over the -40°C to +85°C ambient temperature range.

### Applications

- Standard DMX512 protocol system
- Full Color Mesh Display
- Architectural and Decorative Lighting

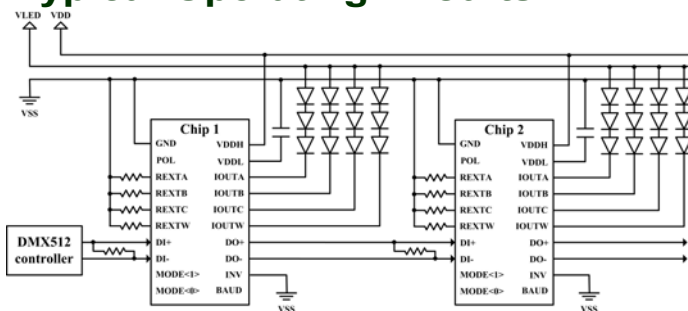
### Features

- ◆ White / CW.WW / R.G.B / R.G.B.W applications
- ◆ One / Two / Three / Four slots data selection for different LED configuration applications
- ◆ 7V to 40V Operating supply voltage
- ◆ 350mA Maximum constant current output (Per channel)
- ◆ Current setting by 4 external resistors
- ◆ 40V Rated output channels for long LED strings
- ◆ ±1.5% (typ.) LED Current accuracy between channels
- ◆ ±3% (typ.) LED Current accuracy between chips
- ◆ Auto-addressing cascade architecture
- ◆ Standard DMX512 protocol decoder (USITT DMX512-A)
- ◆ 4X DMX512 protocol selection (Baud rate=1MHz)
- ◆ Distinctive differential output corresponding with DMX512 format for long distance cascade
- ◆ Wide common-mode range for differential input signals
- ◆ Non-polarity connection for differential data input
- ◆ 14bits grayscale resolution with Adaptive Pulse Density Modulation
- ◆ Gamma, 2.2, to transform 8bits DMX to 14bits APDM data
- ◆ Frame refresh rate > 2000Hz as a LED driver
- ◆ Frame refresh rate > 120Hz as a PWM generator
- ◆ Traditional non-scramble constant current waveform for high power LED applications (PWM generator only)
- ◆ Built-in oscillator for grayscale control and DMX512 decoder
- ◆ -40°C to +85°C Ambient temperature range

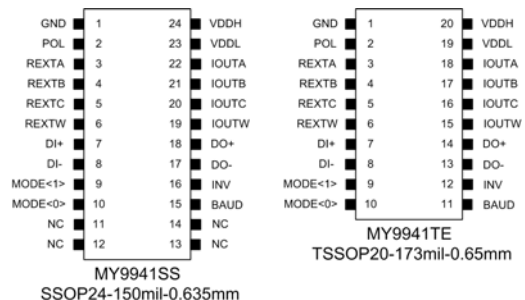
### Order information

PART	PIN PACKAGE	
MY9941SS	SSOP24-150mil-0.635mm	2500 pcs/Reel
MY9941TE	TSSOP20-173mil-0.65mm	2500 pcs/Reel

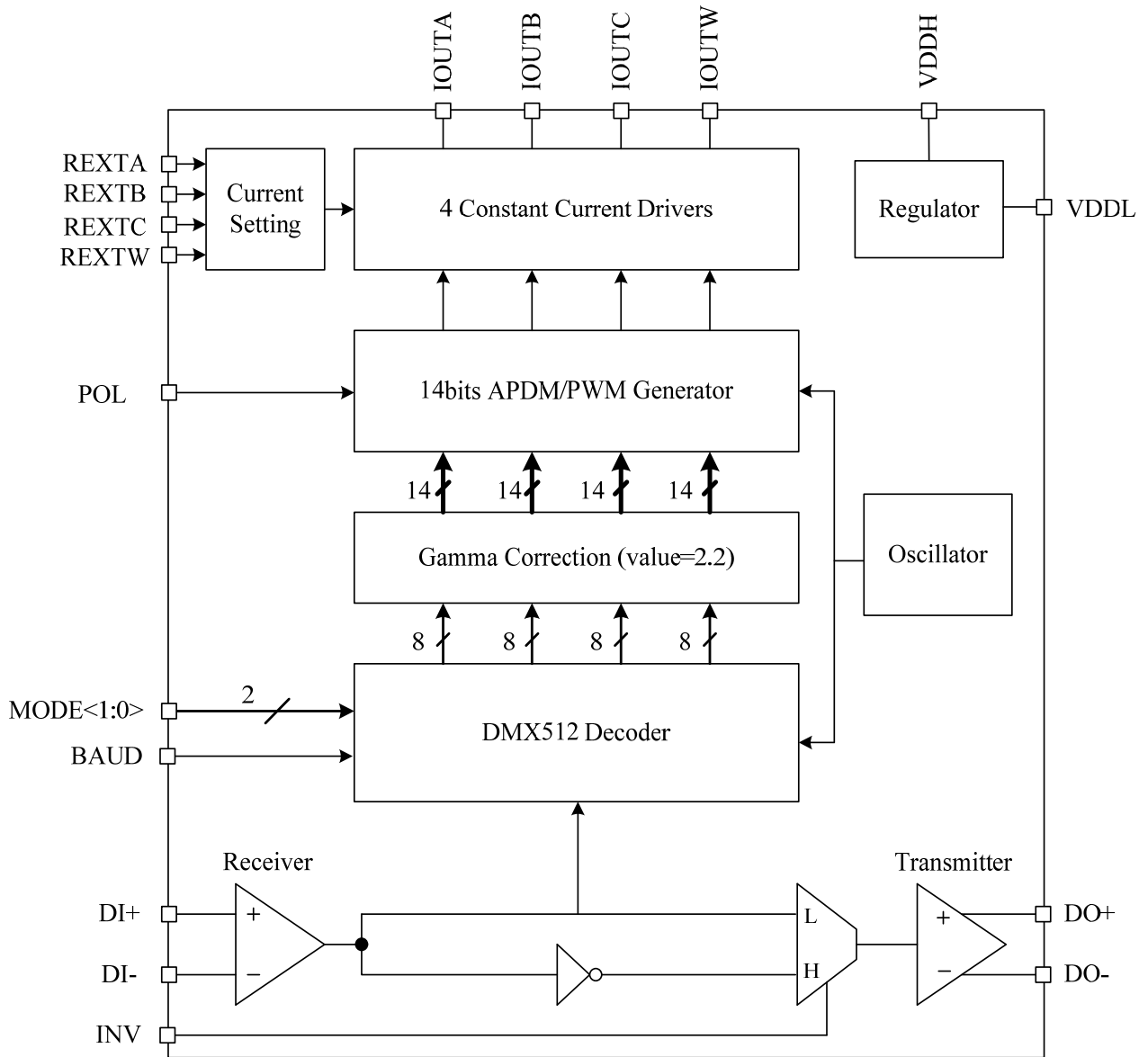
### Typical Operating Circuits



### Pin Configuration



## Block Diagram

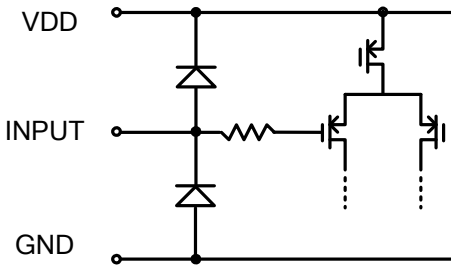


## Pin Assignment

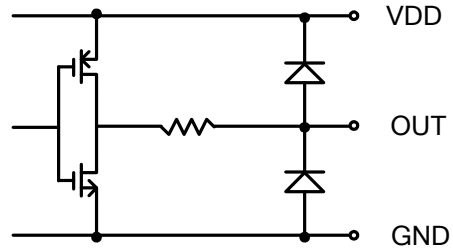
IN No.		PIN NAME	FUNCTION
SSOP24	TSSOP20		
1	1	GND	Ground terminal.
2	2	POL	Output current polarity selection: “L” : work as a PWM generator (traditional non-scrambled waveform) “H(floating)” : work as a LED driver (APDM waveform)
3 4 5 6	3 4 5 6	REXTA REXTB REXTC REXTW	External resistors connected between REXT and GND for IOUTA, IOUTB, IOUTC and IOUTW output current value setting.
7	7	DI+	Positive input terminal of differential DMX signal.
8	8	DI-	Negative input terminal of differential DMX signal.
9	9	MODE<1>	Slot data selection: (Please refer to page14) MODE<1:0>=L & L : four slots mode MODE<1:0>=L & H(floating) : one slot mode MODE<1:0>=H(floating) & L : two slots mode MODE<1:0>=H(floating) & H(floating) : three slots mode
10	10	MODE<0>	
15	11	BAUD	DMX data rate selection: “L” : 4 times DMX data rate (4x) “H(floating)” : standard DMX data rate (1x)
16	12	INV	Differential DMX output polarity selection: “L” : DMXOUT is negative to increase the amount of cascade chips “H(floating)” : DMXOUT is positive
17	13	DO-	Negative output terminal of differential DMX signal.
18	14	DO+	Positive output terminal of differential DMX signal.
19 20 21 22	15 16 17 18	IOUTW IOUTC IOUTB IOUTA	Output terminals for constant current output
23	19	VDDL	Voltage regulator output. Connecting a capacitor, <b>10uF</b> , between VDDL pin and GND pin to stabilize the output voltage, 5V.
24	20	VDDH	Supply voltage terminal.
11, 12, 13, 14		NC	Unconnected

## Equivalent Circuit of Inputs and Output

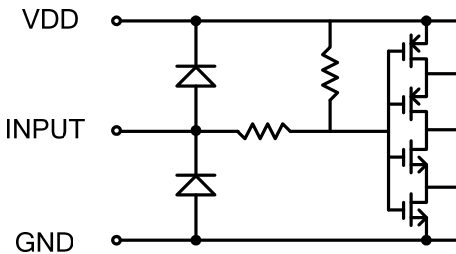
### 1. DI+, DI- terminals



### 2. DO+, DO- terminals



### 3. POL, MODE<1:0>, BAUD, INV terminals



## Maximum Ratings (Ta=25°C, Tj(max) = 150°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	VDDH	44	V
Regulator Voltage	VDDL	7	V
Input Voltage	VIN	-0.3 ~ VDDL+0.3	V
Output Current	IOUT	370	mA
Output Voltage	VOUT	-0.3 ~ 40	V
Thermal Resistance (On 4-layer PCB)	Rth(j-a)	70.5 (SS:SSOP24-173mil-0.65mm )	°C/W
		32 (TE:TSSOP20-173mil-0.65mm )	
Operating Ambient Temperature	Top	-40 ~ 85	°C
Storage Temperature	Tstg	-55 ~ 150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only and functional operation of the device at these or any other condition beyond those specified is not supported.

(2) All voltage values are with respect to ground terminal.

## Electrical Characteristics (VDDL = 5.0 V, Ta = 25°C unless otherwise noted)

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Differential Output voltage (Unloaded)	VOD1	I <sub>o</sub> =0mA, figure 1		—	5	V
Differential Output voltage (loaded)	VOD2	R=27Ω, figure 1	0.7	—	1.5	
Differential Common-mode Output Voltage	VOC	R=27Ω, figure 1	—	—	3	
Differential Input Threshold Voltage	VTH	-7V ≤ V <sub>CM</sub> ≤ 12V	-0.2		0.2	
Differential Input Hysteresis	ΔVTH	V <sub>CM</sub> =0V		70		mV
Differential Input Resistance	RIN		192			kΩ
Differential Output Short-Circuit Current, V <sub>out</sub> =High	IOS1	V <sub>out</sub> =-7V			TBD	mA
Differential Output Short-Circuit Current, V <sub>out</sub> =Low	IOS2	V <sub>out</sub> =10V	TBD			mA
Input Current of Differential Input	IDI	VIN=12V		50		uA
		VIN=-7V		-30		
Regulator Output Voltage	VDDL	VDDH=7~40V		5		V
Current Setting Feedback Voltage	V <sub>rext</sub>	VDDH=40V R <sub>rext</sub> =20Ω and V <sub>o</sub> =1V		0.4		V
IOUT Leakage Current	ILK	V <sub>o</sub> =40V			0.1	uA
Output Current Skew (Channel-to-Channel) *1	dIOUT1	VOUT = 1.0 V R <sub>rext</sub> = 16 Ω	—	±1.5	±3	%
Output Current Skew (Chip-to-Chip) *2	dIOUT2		—	±3	±6	%
Output Current Skew (Channel-to-Channel) *1	dIOUT1	VOUT = 1.0 V R <sub>rext</sub> = 2.6 Ω	—	±1.5	±3	%
Output Current Skew (Chip-to-Chip) *2	dIOUT2		—	±3	±6	%
Output Voltage Regulation*3	% / VOUT	R <sub>rext</sub> = 16 Ω VOUT = 7 V ~ 40 V	—	—	±0.1	% / V
Supply Voltage Regulation*4	% / VDDH	R <sub>rext</sub> = 16Ω VDDH = 7 V ~ 40 V	—	±0.6	±1	
CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT

\*1 Channel-to-channel skew is defined by the formula below:

$$\Delta(\%) = \left[ \frac{I_{out_n}}{(I_{out_0} + I_{out_1} + \dots + I_{out_{15}})} - 1 \right] * 100\%$$

\*2 Chip-to-Chip skew is defined by the formula below:

$$\Delta(\%) = \left[ \frac{(I_{out_0} + I_{out_1} + \dots + I_{out_{15}}) - (Ideal\ Output\ Current)}{16} \right] * 100\%$$

\*3 Output voltage regulation is defined by the formula below:

$$\Delta(\%/V) = \left[ \frac{I_{out_n}(@V_{out_n} = 3V) - I_{out_n}(@V_{out_n} = 1V)}{I_{out_n}(@V_{out_n} = 3V)} \right] * \frac{100\%}{3V - 1V}$$

\*4 Supply voltage regulation is defined by the formula below:

$$\Delta(\%/V) = \left[ \frac{I_{out_n}(@V_{DDH} = 40V) - I_{out_n}(@V_{DDH} = 7V)}{I_{out_n}(@V_{DD} = 7V)} \right] * \frac{100\%}{40V - 7V}$$

Supply Current	$I_{DD1(off)}$	all pins are open unless VDD and GND	—	1.7	2.5	mA
	$I_{DD2(off)}$	input signal is static $R_{rest} = 16 \Omega$ all outputs turn off	—	2.3	3.1	
	$I_{DD1(on)}$	input signal is static $R_{rest} = 16 \Omega$ all outputs turn on	—	2.4	3.2	
	$I_{DD3(off)}$	input signal is static $R_{rest} = 2.6 \Omega$ all outputs turn off	—	6.0	6.5	
	$I_{DD2(on)}$	input signal is static $R_{rest} = 2.6 \Omega$ all outputs turn on	—	6.1	6.6	

### Switching Characteristics (VDDL = 5.0V, Ta = 25°C unless otherwise noted)

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay From DI to DO ( "L" to "H" )	tpLH	VDDH=40V $R_{DIFF}=54\Omega$ $R_{LOAD}=196k\Omega$ $C_L=100pF$ DI(diff)=1.5V	—	40		ns
Propagation Delay From DI to DO ( "H" to "L" )	tpHL		—	40		
Propagation Delay Skew	tskew		5			
DO rise time	tr(DO)		—	20		
DO fall time	tf(DO)			20		
Output Current Rise Time	tor		100			
Output Current Fall Time	tof		100	—		
Internal Grayscale Clock Frequency	FGCK			2		MHz

### Test Circuits

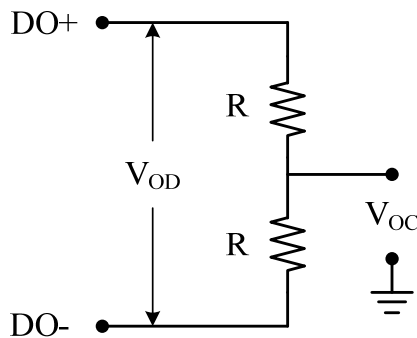


Figure1. Differential Output DC Test Circuit

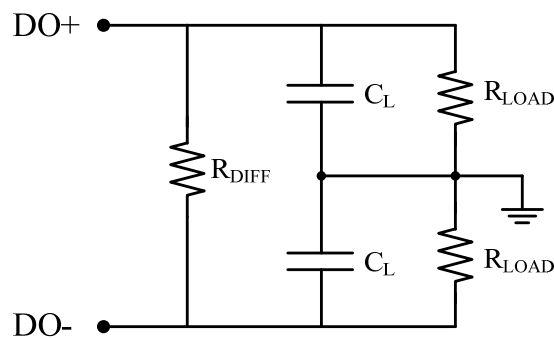


Figure2. Differential Output Timing Test Circuit

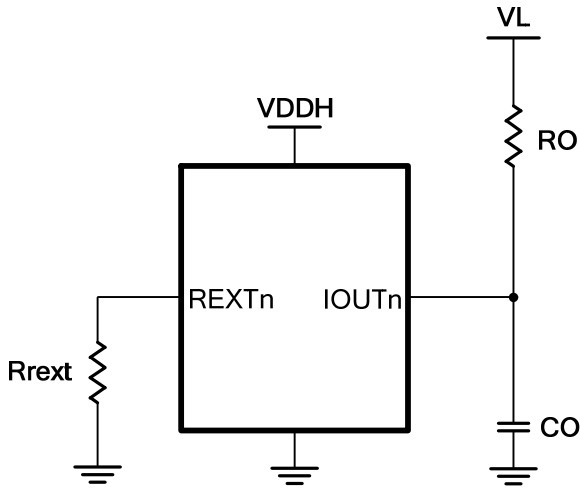
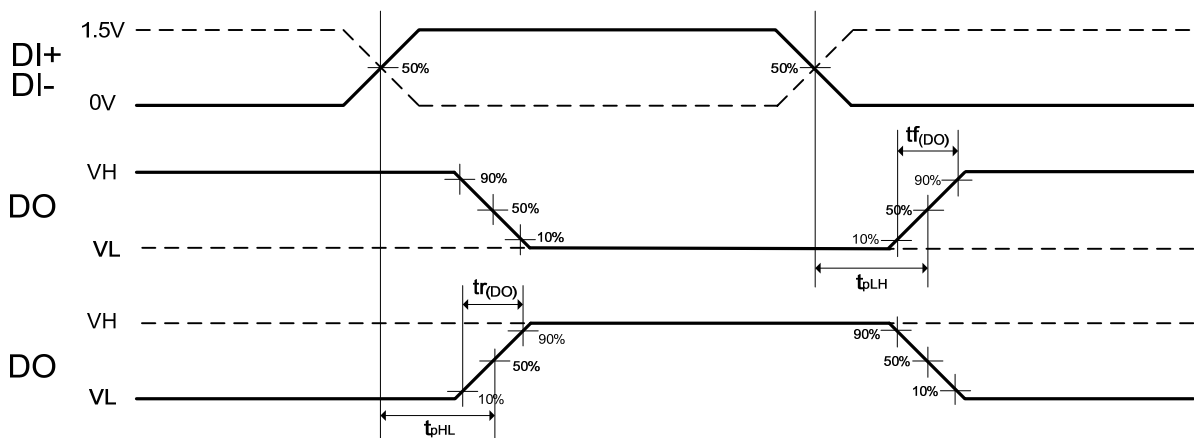


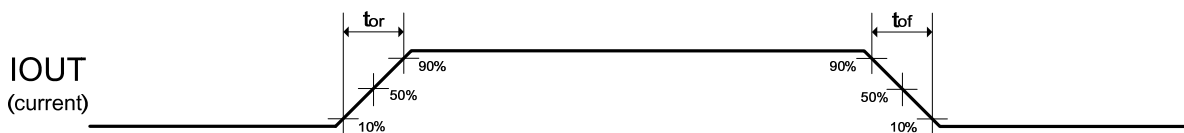
Figure3. IOUT Switching Characteristics Test Circuit

### Timing Diagram

1. DI to DO



2. IOUT



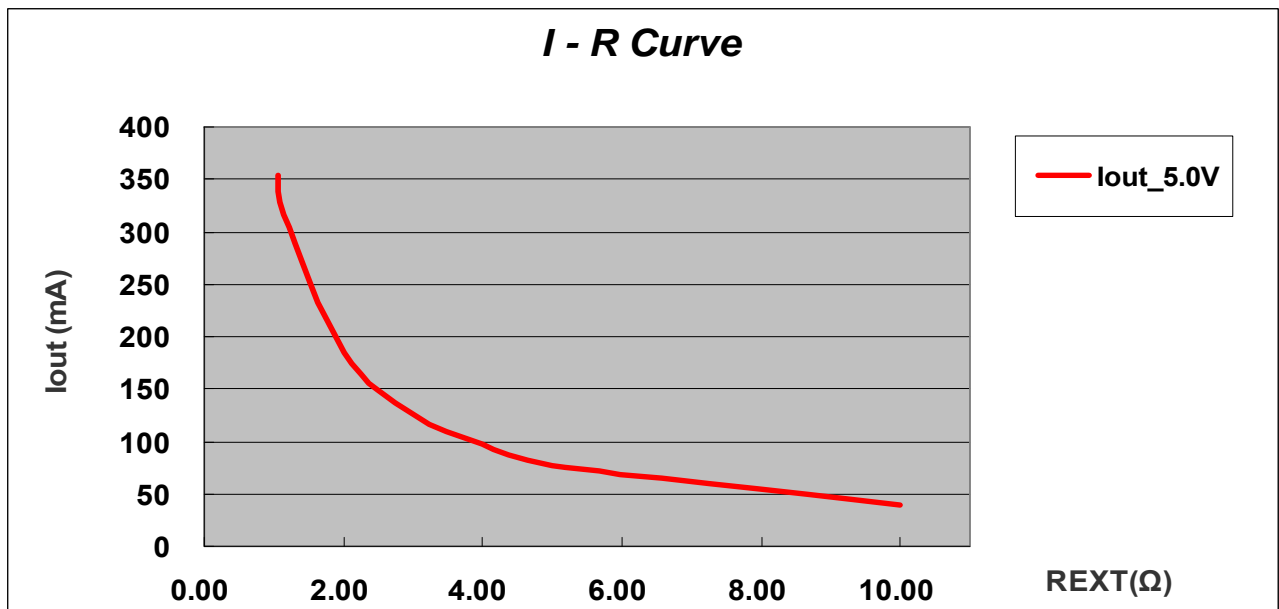
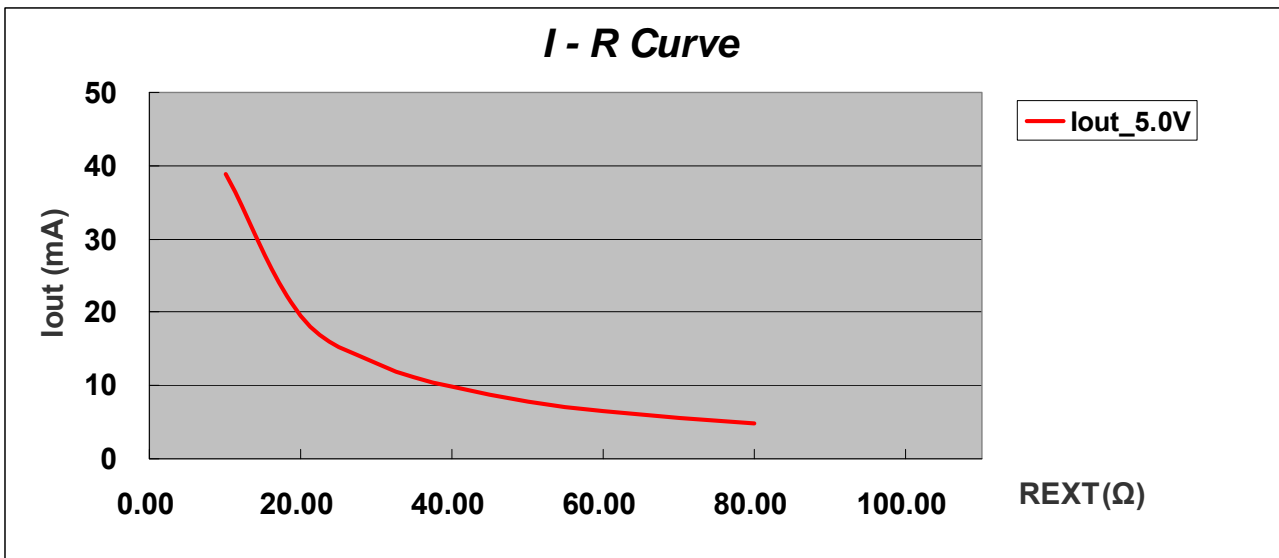
## Reference Resistor

The constant current values are determined by an external resistor placed between REXT pin and GND pin. The following formula is utilized to calculate the current value:

$$I_{out}(mA) = V_{R_{ext}}(V) / R_{ext}(k\Omega) = 0.4V / R_{ext}(k\Omega)$$

Where  $R_{ext}$  is a resistor placed between REXT and GND

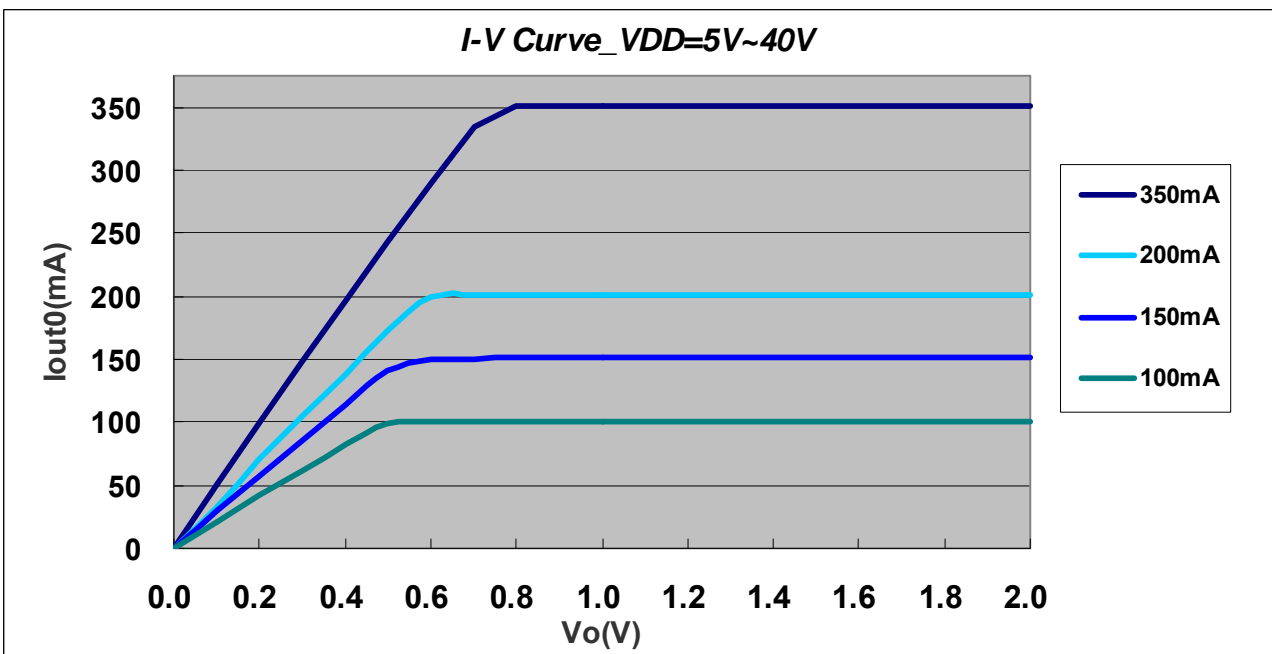
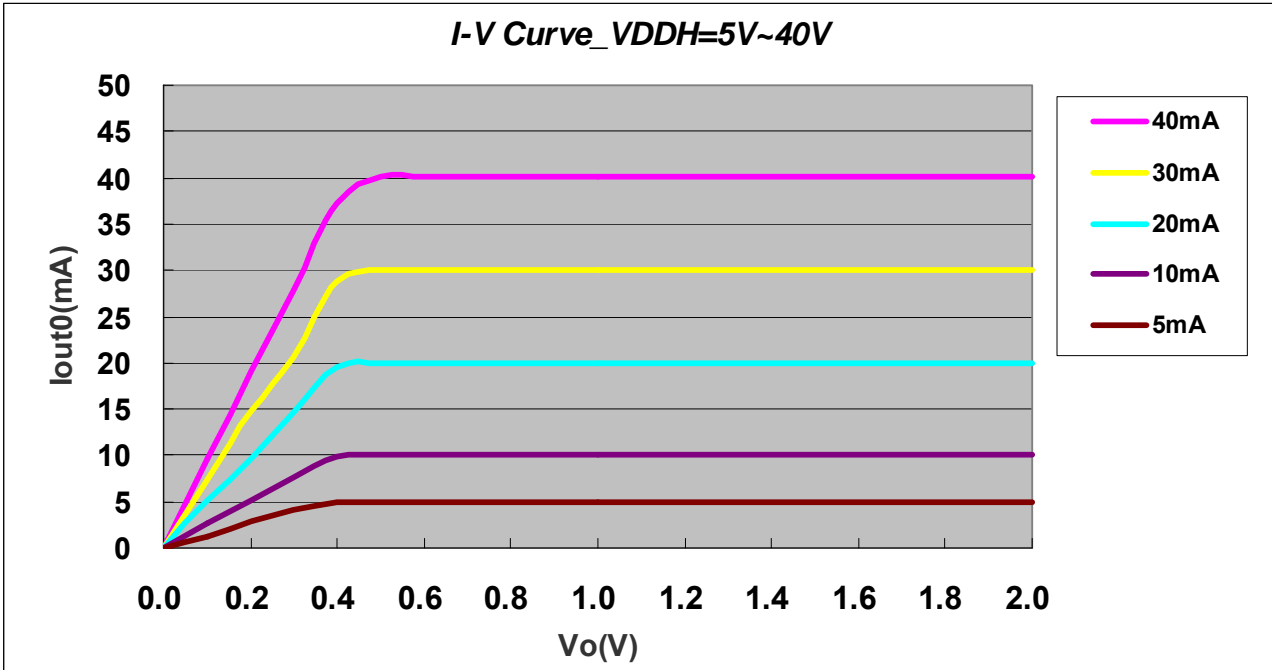
For example,  $I_{out}$  is 20mA when  $R_{ext}=20\Omega$  and  $I_{out}$  is 50mA when  $R_{ext}=8\Omega$



## Constant-Current Output

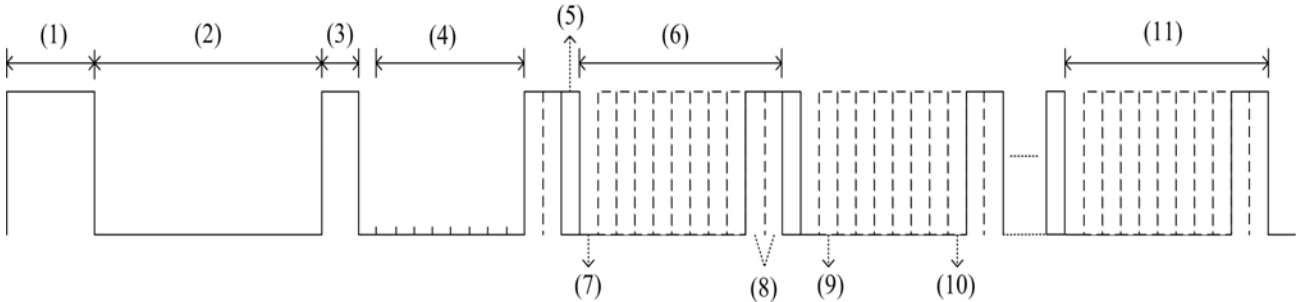


The current characteristics could maintain invariable in the influence of loading voltage. Therefore, the MY9941 could minimize the interference of different LED forward voltages and produce the constant current. The following figures illustrate the suitable output voltage should be determined in order to keep an excellent performance.



**Standard DMX512 Protocol (BAUD=H)**

DMX512 is a standard that describes a method of digital data transmission between controllers and lighting equipment and accessories. MY9941 supports DMX512 protocol in accordance with USITT DMX512-A standard except for the Break time and the MBB time when the INV pin is set to LOW.



Reference	Description	Duration
(1)	Mark Time Before Break (MBB)	0us~1s (more limitations as INV=L)
(2)	Break	$88\mu s \leq T_{Break}$ (more limitations as INV=L)
(3)	Mark Time After Break (MAB)	4us~1s
(4)	Start Code (Slot 0 data)	$32\mu s \pm 2\%$ <b>(Start Code must be null)</b>
(5)	Mark Time Between Slot	0s~1s
(6)	Slot Time	$44\mu s \pm 2\%$
(7)	Start Bit	$4\mu s \pm 2\%$
(8)	Stop Bits	$4\mu s \pm 2\%$
(9)	Least Significant Data Bit	$4\mu s \pm 2\%$
(10)	Most Significant Data Bit	$4\mu s \pm 2\%$
(11)	The Number of Slots	Not Limited

\* Power-On Procedure (only needed as INV=L):

Users have to keep the input signal in high level over 440us after power-on and then transmit a DMX signal.

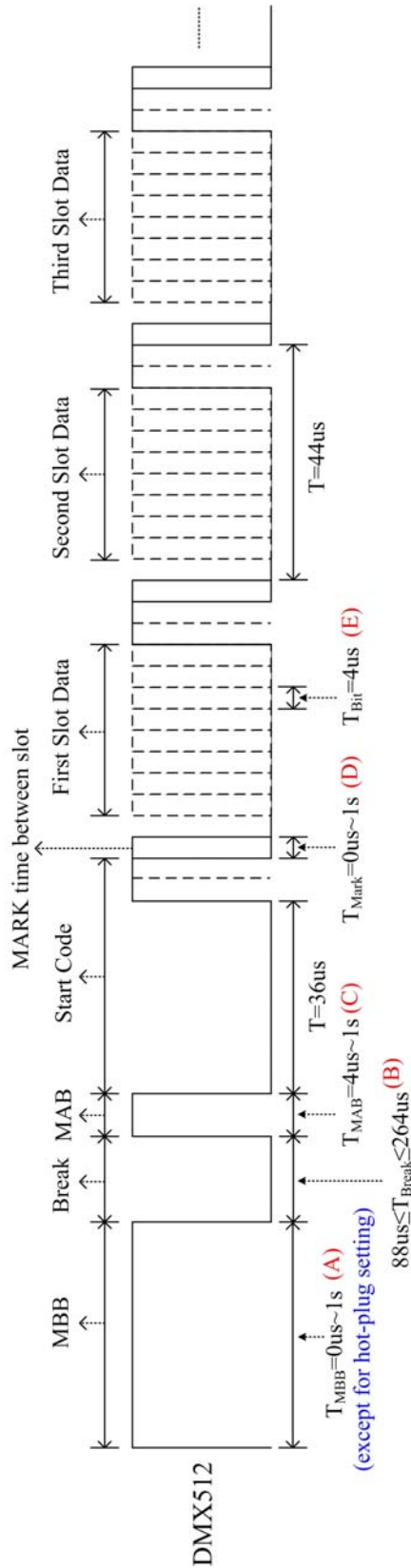
\* Hot-Plug Setting (only needed as INV=L):

The MBB time ( or the MAB time or the Mark Time Between Slot ) has to be set over 440us in order to avoid that Hot-Plug operations disrupt the decoding process.

\* When INV=L, the Break time must be limited in the range of  $88\mu s \leq T_{Break} \leq 264\mu s$ .

\* Power-On procedure, Hot-Plug setting and Break time limitation could be neglected when INV=H or floating.

Standard DMX512 Interface (BAUD=H, INV=L)



<< Power-On procedure >>

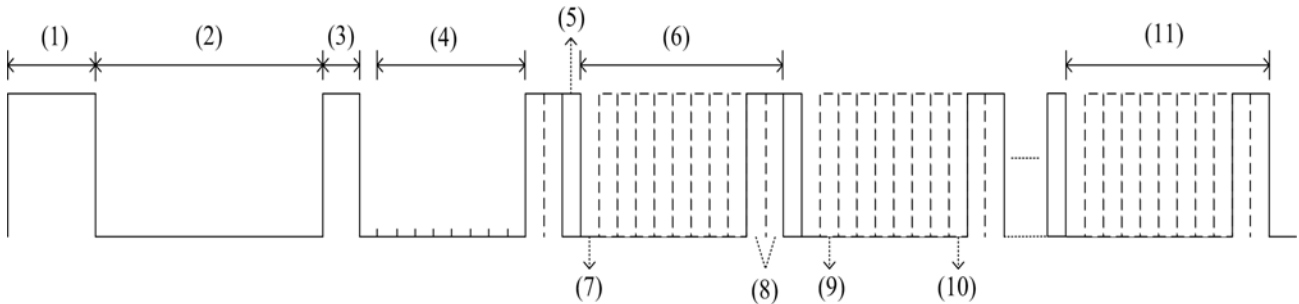
Users have to keep the input signal in high level over 440us and then transmit a DMX512 signal.

<< Hot-plug setting >>

Users have to keep  $T_{MBB}$  ( or  $T_{MAB}$  or the Mark time between slot ) in high level over 440us when transmitting a DMX512 signal.

## 4X DMX512 Protocol (BAUD=L)

DMX512 is a standard that describes a method of digital data transmission between controllers and lighting equipment and accessories. MY9941 also supports 4X DMX512 protocol in order to enhance data refresh rate.



Reference	Description	Duration
(1)	Mark Time Before Break (MBB)	0us~1s (more limitations as INV=L)
(2)	Break	$22\mu s \leq T_{Break}$ (more limitations as INV=L)
(3)	Mark Time After Break (MAB)	1us~1s
(4)	Start Code (Slot 0 data)	$8\mu s \pm 2\%$ <b>(Start Code must be null)</b>
(5)	Mark Time Between Slot	0s~1s
(6)	Slot Time	$11\mu s \pm 2\%$
(7)	Start Bit	$1\mu s \pm 2\%$
(8)	Stop Bits	$1\mu s \pm 2\%$
(9)	Least Significant Data Bit	$1\mu s \pm 2\%$
(10)	Most Significant Data Bit	$1\mu s \pm 2\%$
(11)	The Number of Slots	Not Limited

**\* Power-On Procedure (only needed as INV=L):**

Users have to keep the input signal in high level over 110us after power-on and then transmit a 4X DMX signal.

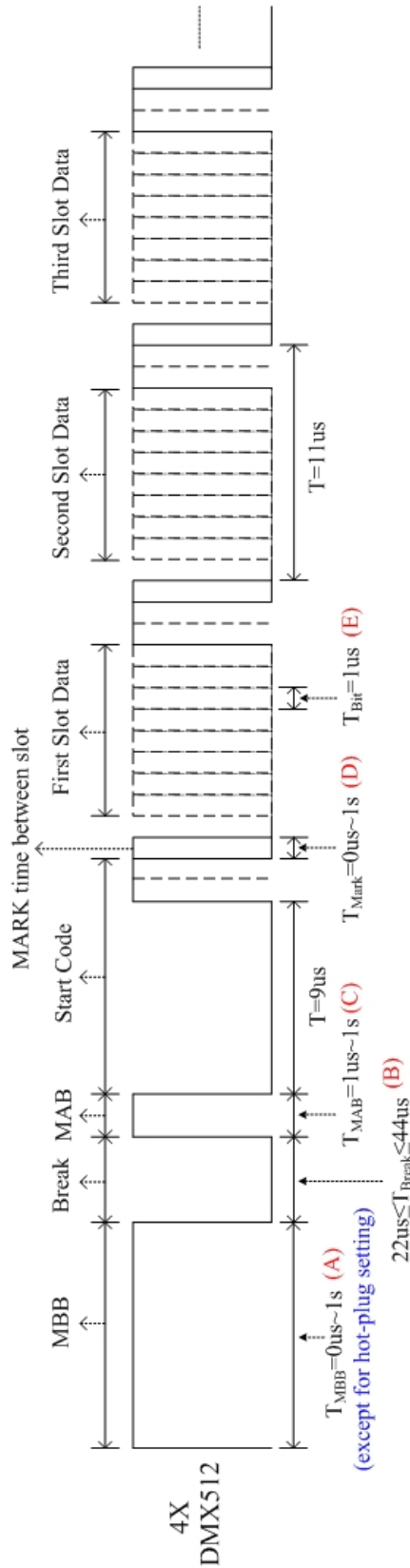
**\* Hot-Plug Setting (only needed as INV=L):**

The MBB time ( or the MAB time or the Mark Time Between Slot ) has to be set over 110us in order to avoid that Hot-Plug operations disrupt the decoding process.

**\* When INV=L, the Break time must be limited in the range of  $22\mu s \leq T_{Break} \leq 66\mu s$ .**

**\* Power-On procedure, Hot-Plug setting and Break time limitation could be neglected when INV=H or floating.**

4X DMX512 Interface (BAUD=L, INV=L)



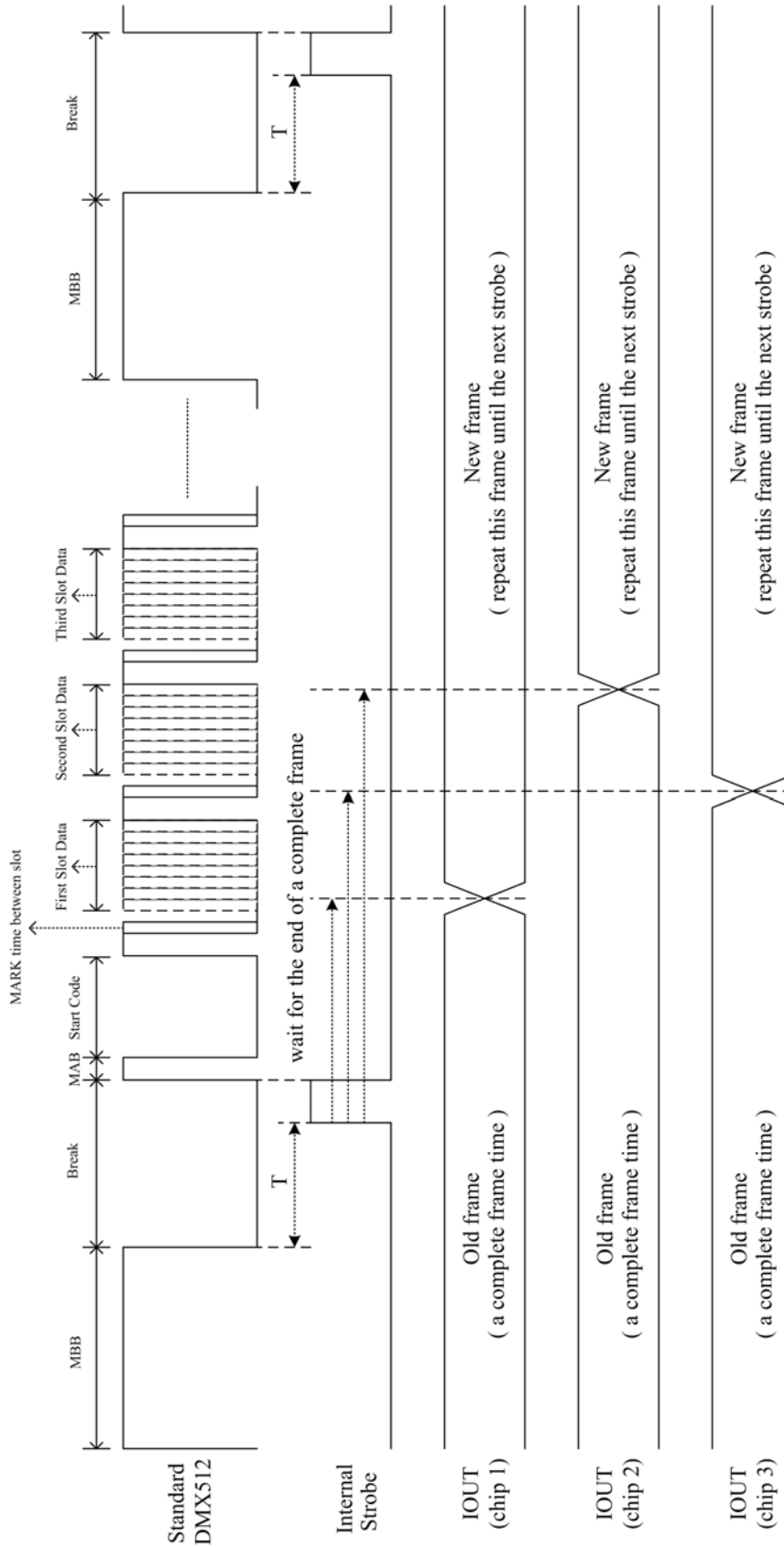
<< Power-On procedure >>

Users have to keep the input signal in high level over 110us and then transmit a 4X DMX signal.

<< Hot-plug setting >>

Users have to keep  $T_{MBB}$  ( or  $T_{MAB}$  or the Mark time between slot ) in high level over 110us when transmitting a 4X DMX512 signal.

## Frame Latch (Break)

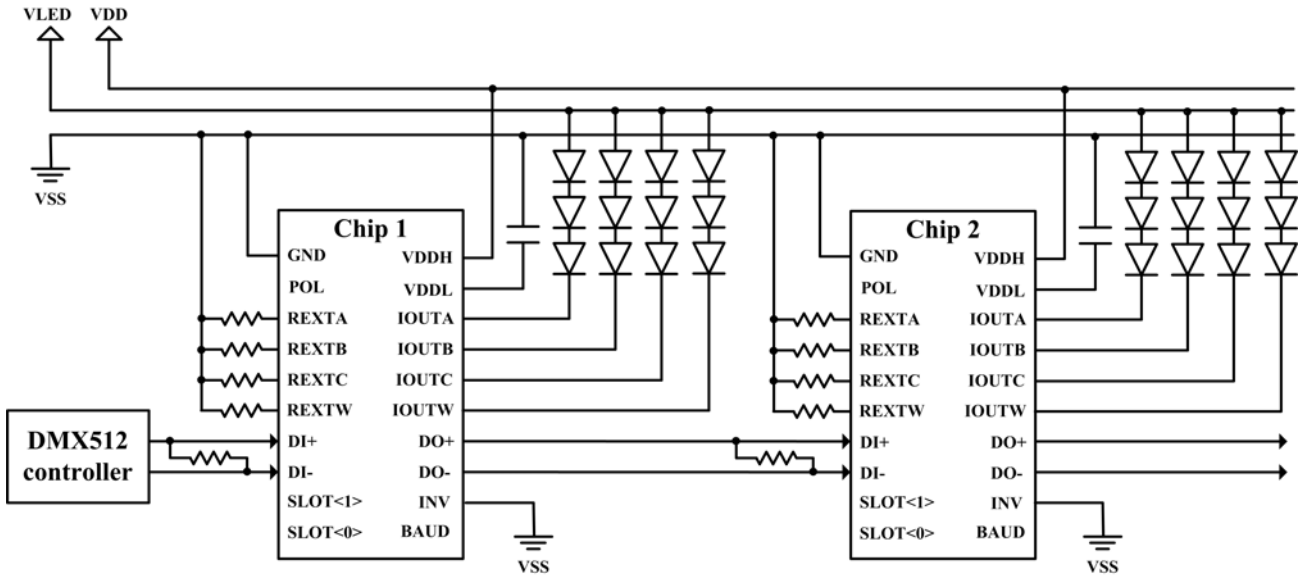


\*\* Free-running frame latch: the next data are loaded into devices after the previous frame is accomplished in order to maintain the completeness of frame.

\*\* A complete frame time is determined by the internal oscillator's frequency of each chip

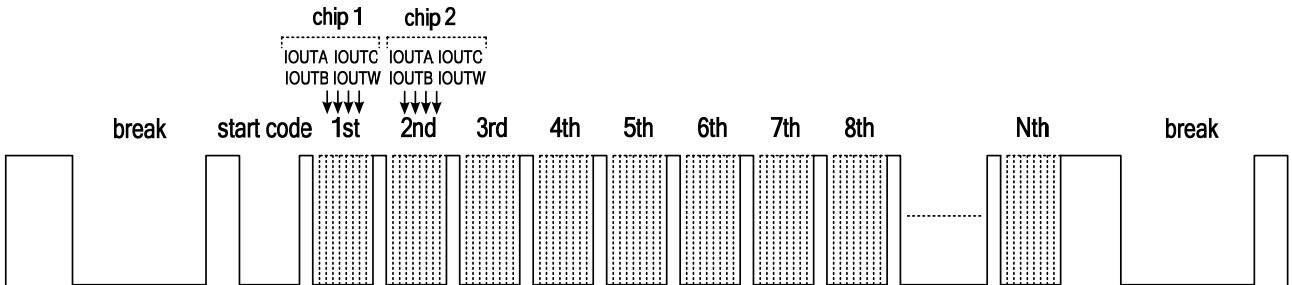
\*\* A complete frame time =  $16394 * (0.5\mu s \pm \text{deviation})$  and the maximum deviation is 0.1us

Auto-addressing Approach and Slot Data Selection

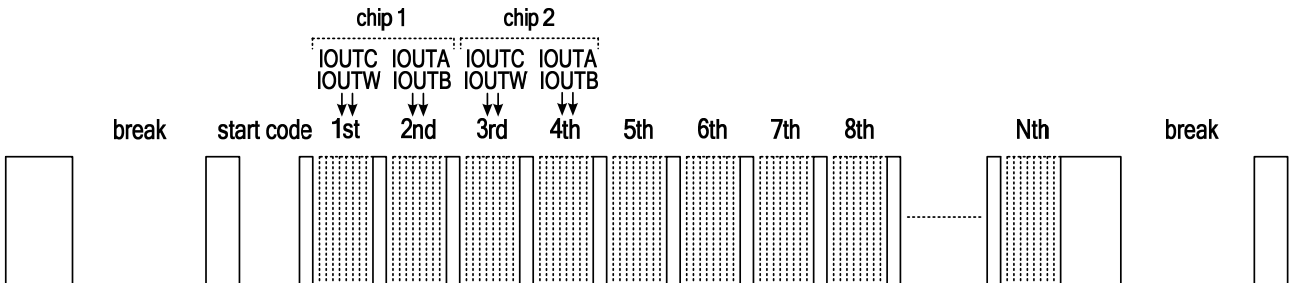


When a lot of MY9941 are connected in cascade, each device addresses automatically and loads grayscale data according to two slot selection pins  $MODE<1:0>$ . The sequence of data loading is illustrated below.

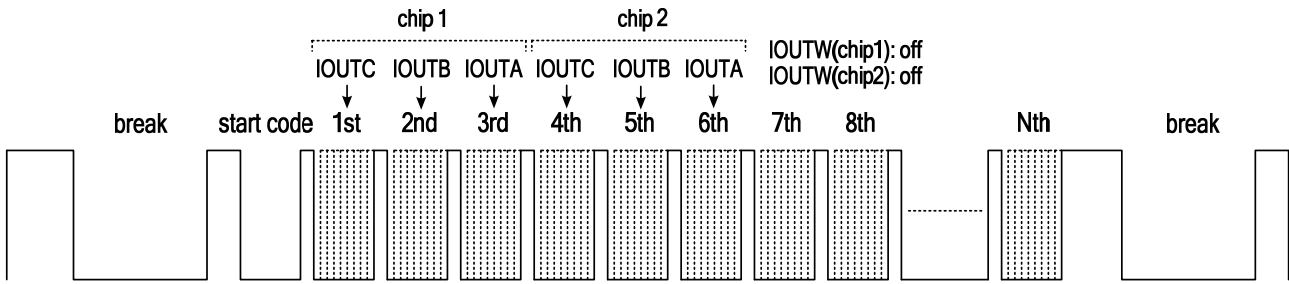
$MODE<1> : MODE<0> = L : H \rightarrow$  One slot mode



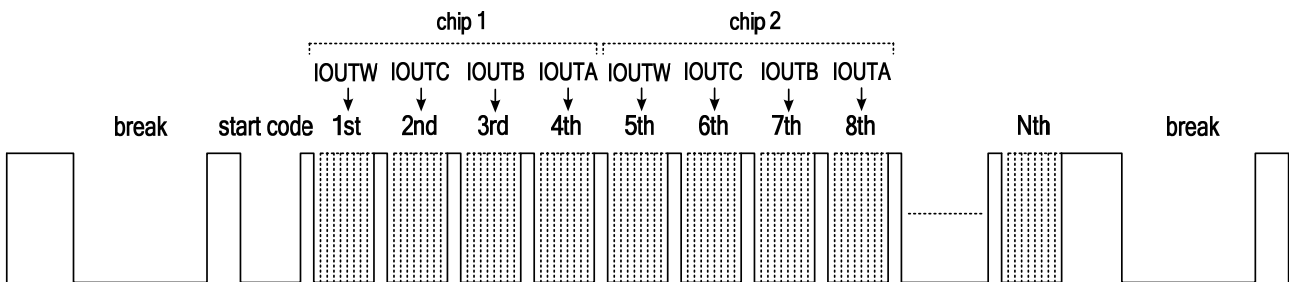
$MODE<1> : MODE<0> = H : L \rightarrow$  Two slots mode



MODE<1> : MODE<0> = H : H → Three slots mode

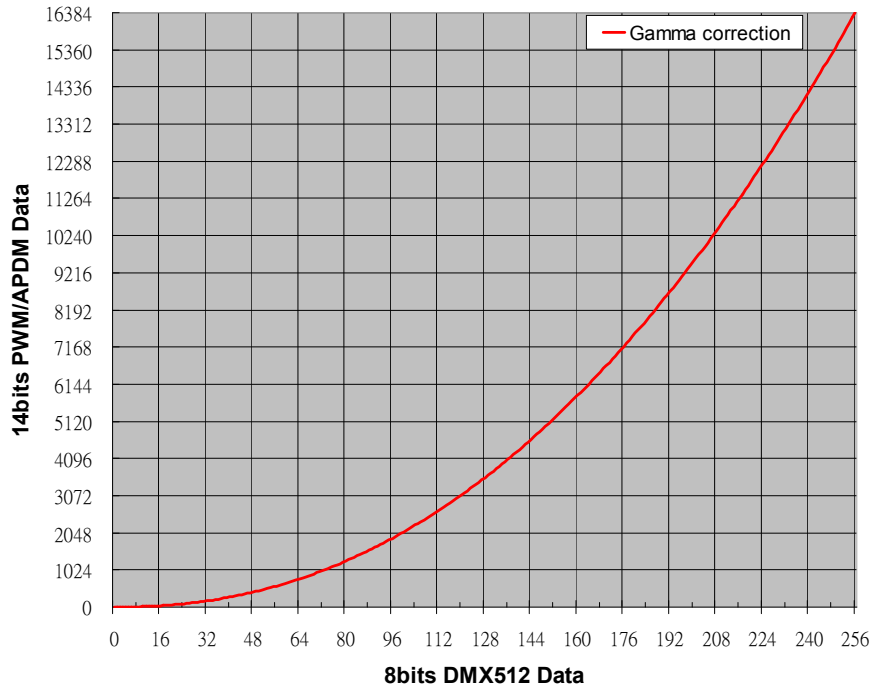


MODE<1> : MODE<0> = L : L → Four slots mode



## Gamma Correction

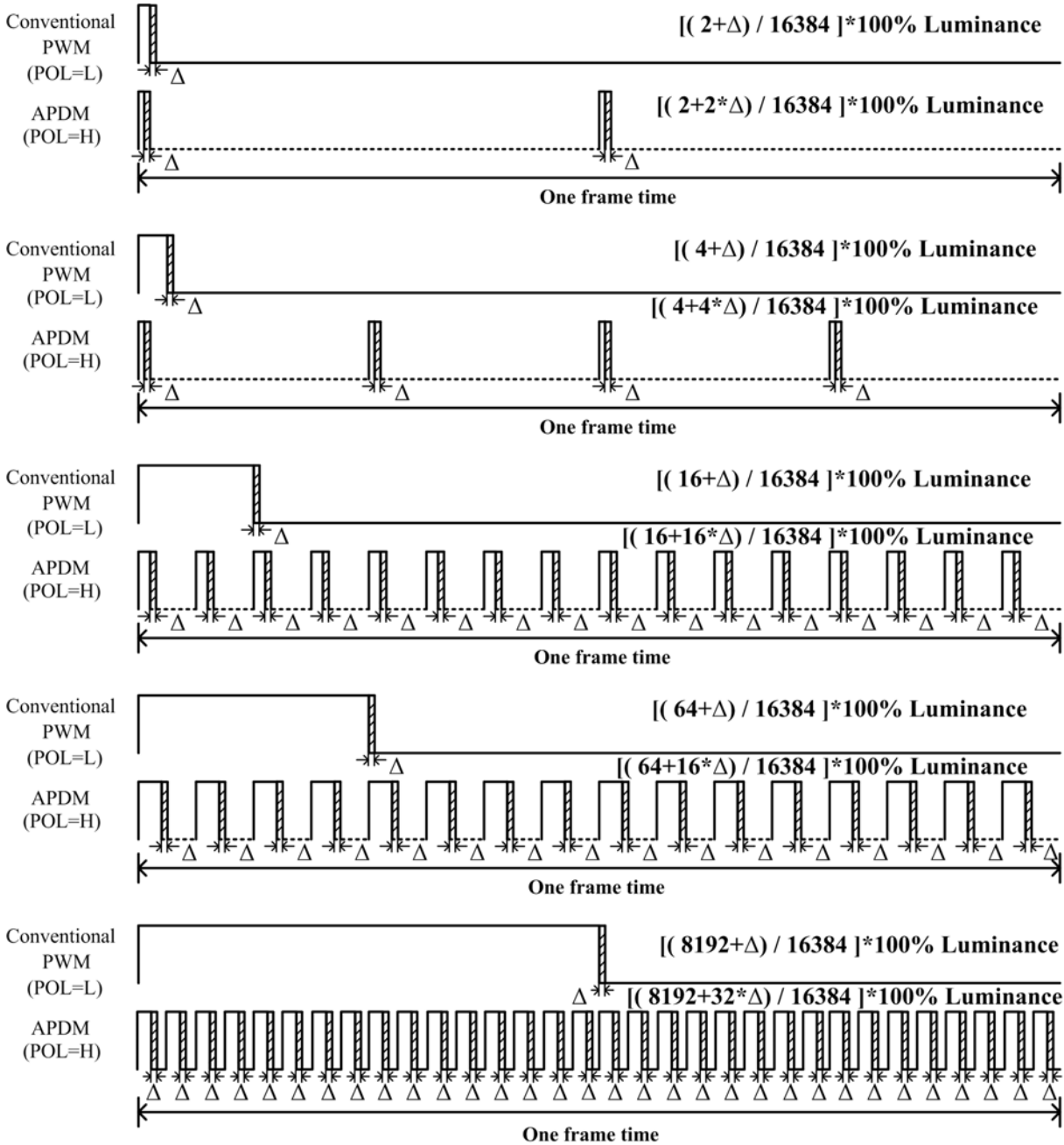
Gamma Correction (value=2.2)



MY9941 supports Gamma Correction function, 2.2, to transform 8bits DMX512 data to 14bits PWM/APDM data in order to enhance brightness contract.

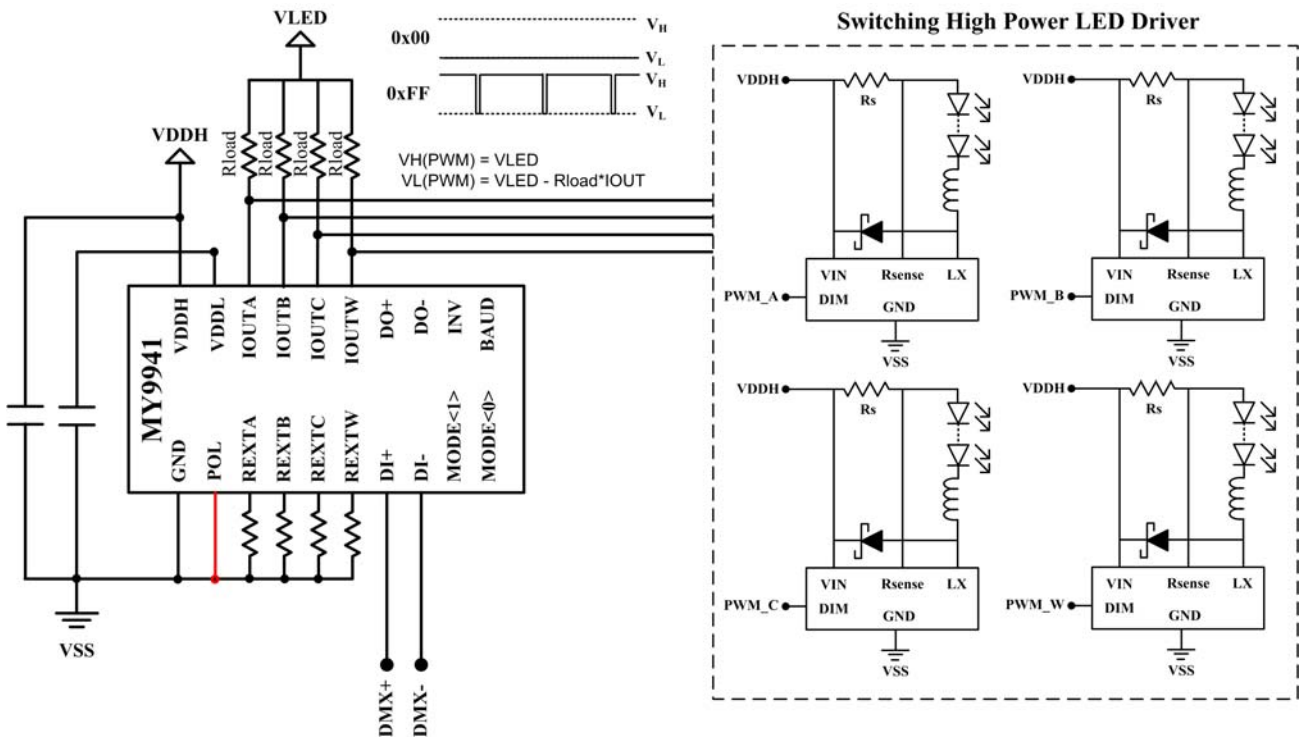


APDM (Adaptive Pulse Width Modulation, only for LED driver, POL=H)

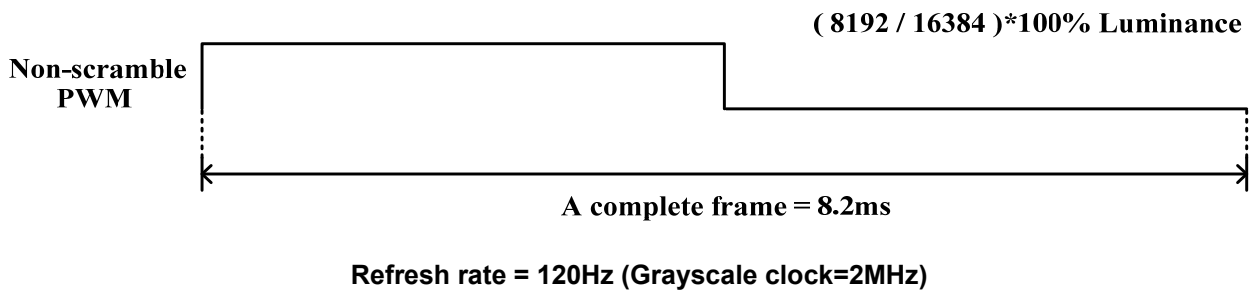


- ▲ The waveform is divided into 16 sections when the luminance is below 8192/16384.
- ▲ The waveform is divided into 32 sections when the luminance is over 8192/16384.
- ▲ MY-semi issues this APDM approach, Adaptive Pulse Width Modulation, in order to abate the non-ideal IOUT distortion due to non-symmetrical transient response at low luminance and improve the refresh rate at high luminance.
- ▲ The  $\Delta$ -width correction technique ( $\Delta \neq 0$ ) is used to compensate the non-ideal output current transient response.

## PWM generator (POL=L)

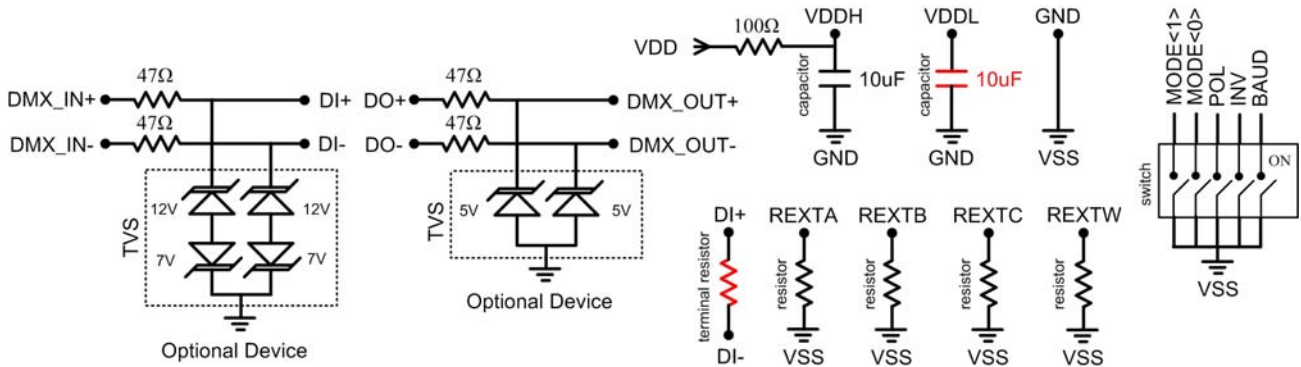
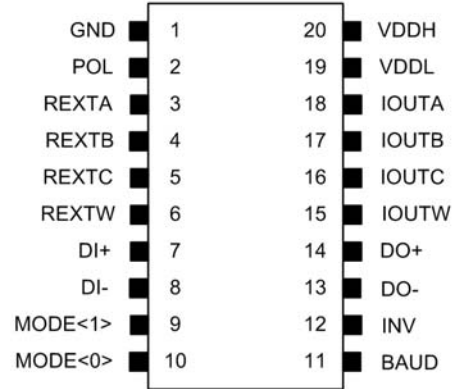
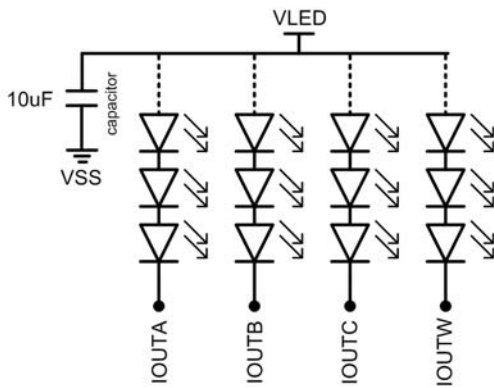


MY9941 could be set as a PWM generator to produce 14bits traditional non-scrambled PWM waveform for high power LED lighting applications. The POL pin is set to VSS and the IOUT pins are connected to VLED by Rload resistors in order to determine VH and VL level of PWM signal. The refresh rate of MY9941 is 120Hz as a PWM generator, POL=L.



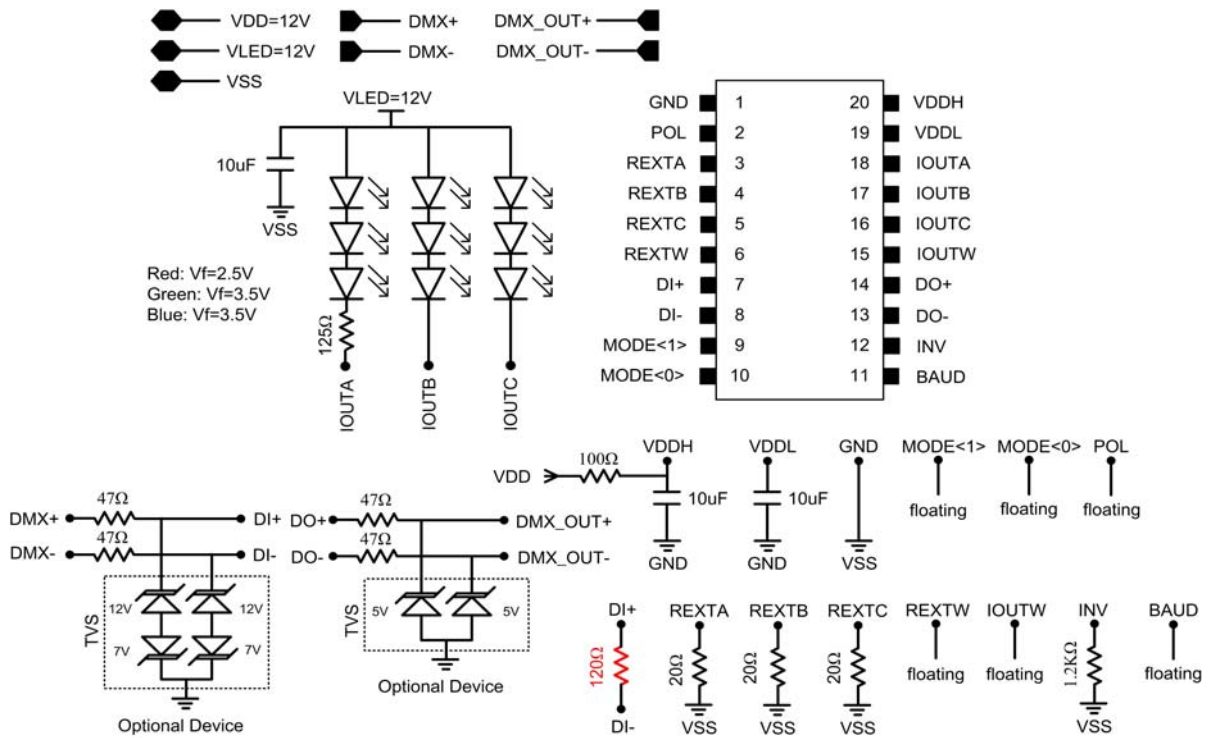
Application (LED Driver)

VDD=7V~40V

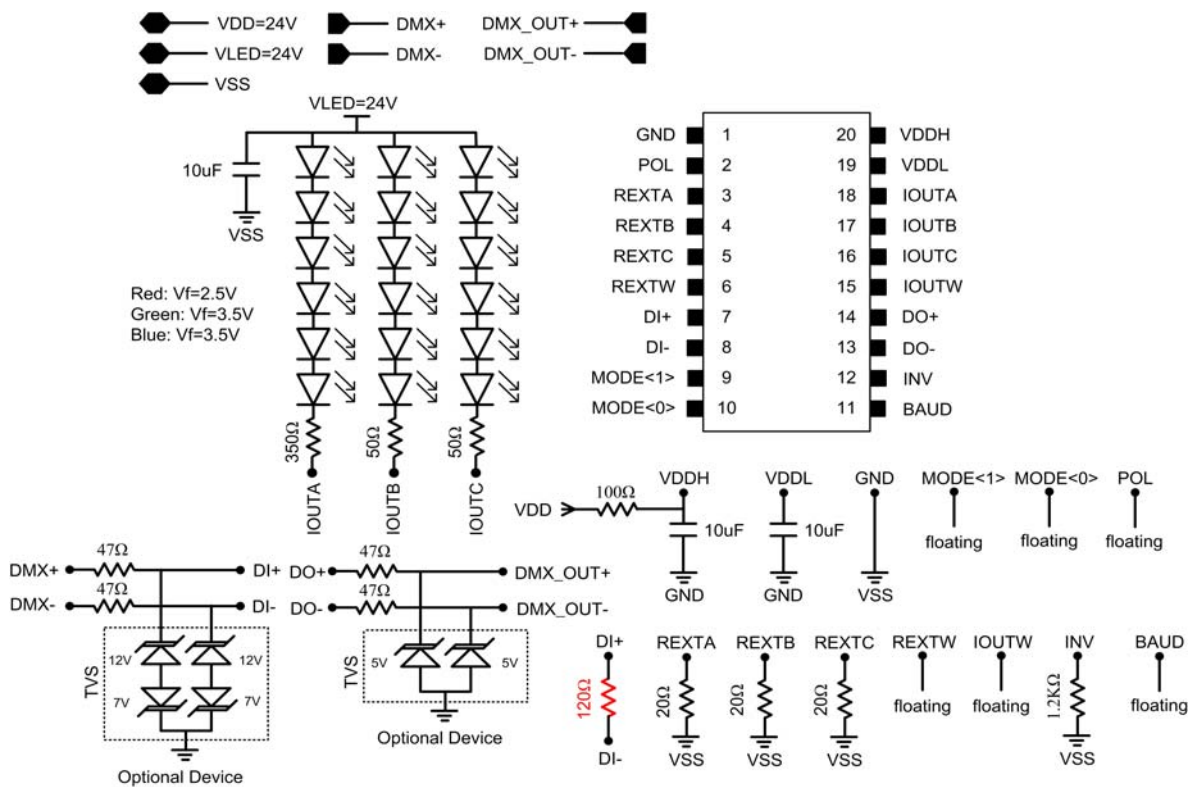


## Application sample (LED Driver)

VDD=VLED=12V, IOU=20mA, Three slots mode, Standard DMX512

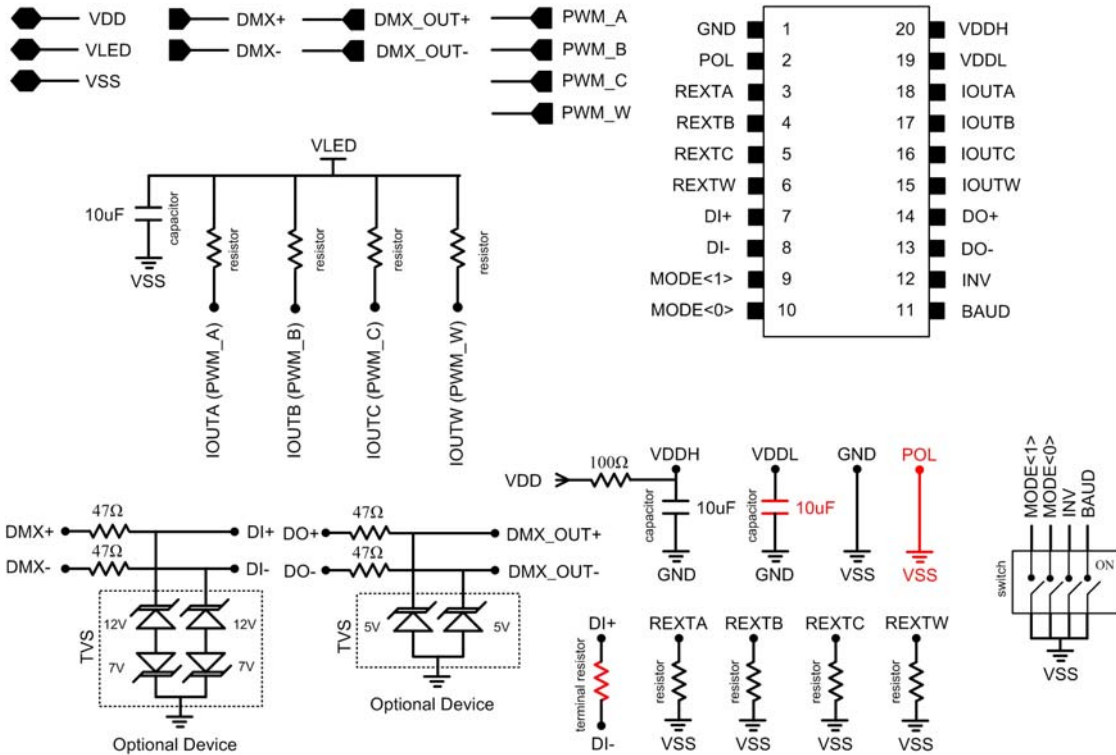


VDD=VLED=24V, IOU=20mA, Three slots mode, Standard DMX512



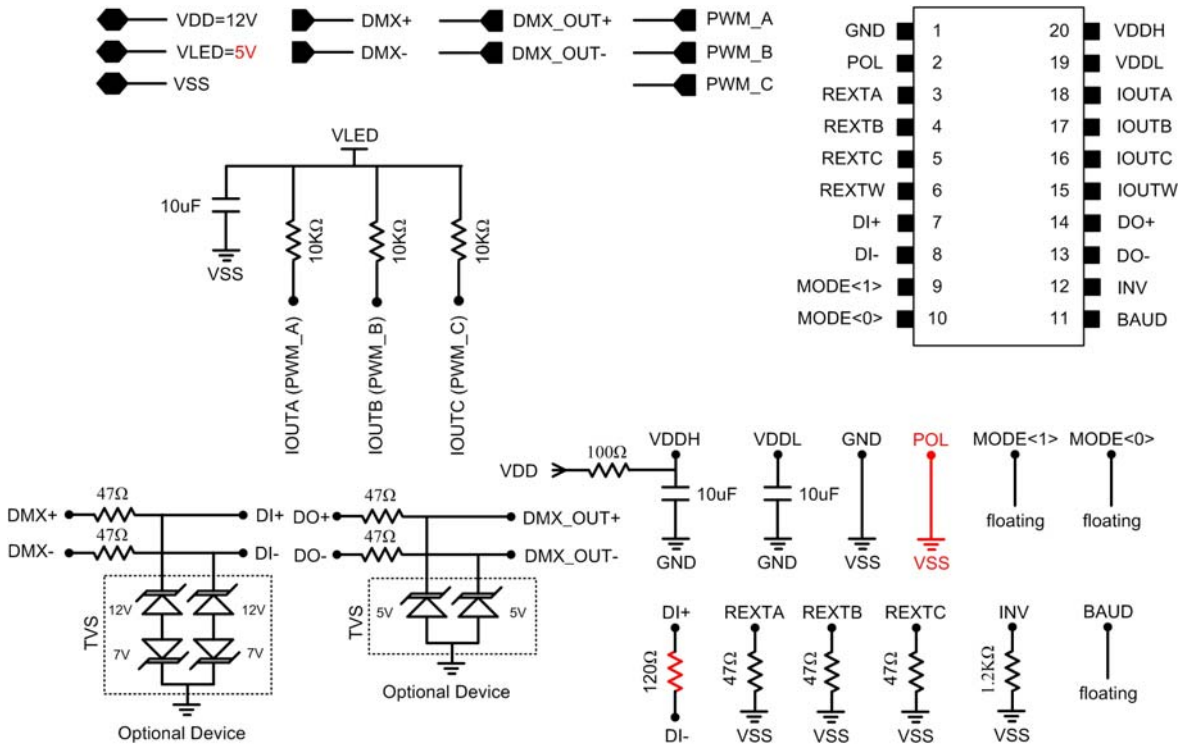
Application (PWM Generator)

VDD=7V~40V



Application Sample (PWM Generator)

VDD=12V, VH(PWM)=5V, VL(PWM)=0V, Standard DMX512 protocol



## Power Dissipation

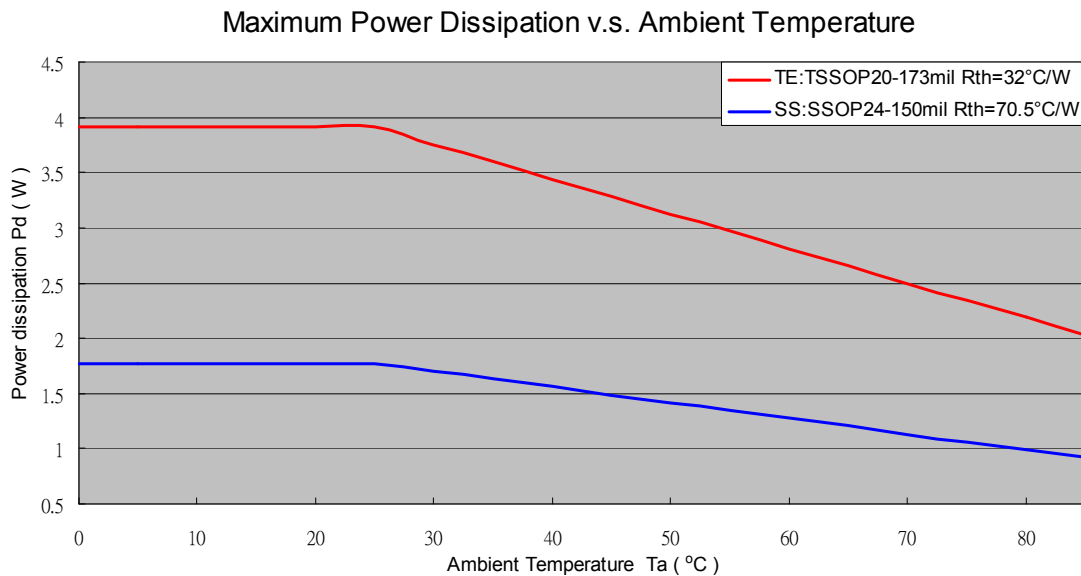
When all four output channels are turned on, the practical power dissipation is determined by the following equation:

$$PD (practical) = V_{DDH} \times I_{DDH} + V_{outA} \times I_{outA} \times DutyA + V_{outB} \times I_{outB} \times DutyB + V_{outC} \times I_{outC} \times DutyC + V_{outW} \times I_{outW} \times DutyW$$

In secure operating conditions, the power consumption of an integrated chip should be less than the maximum permissible power dissipation which is determined by the package type and ambient temperature. The formula for maximum power dissipation is described as follows:

$$PD (max) = \frac{T_j(max)(^{\circ}C) - T_a(^{\circ}C)}{R_{th(j-a)}(^{\circ}C/Watt)}$$

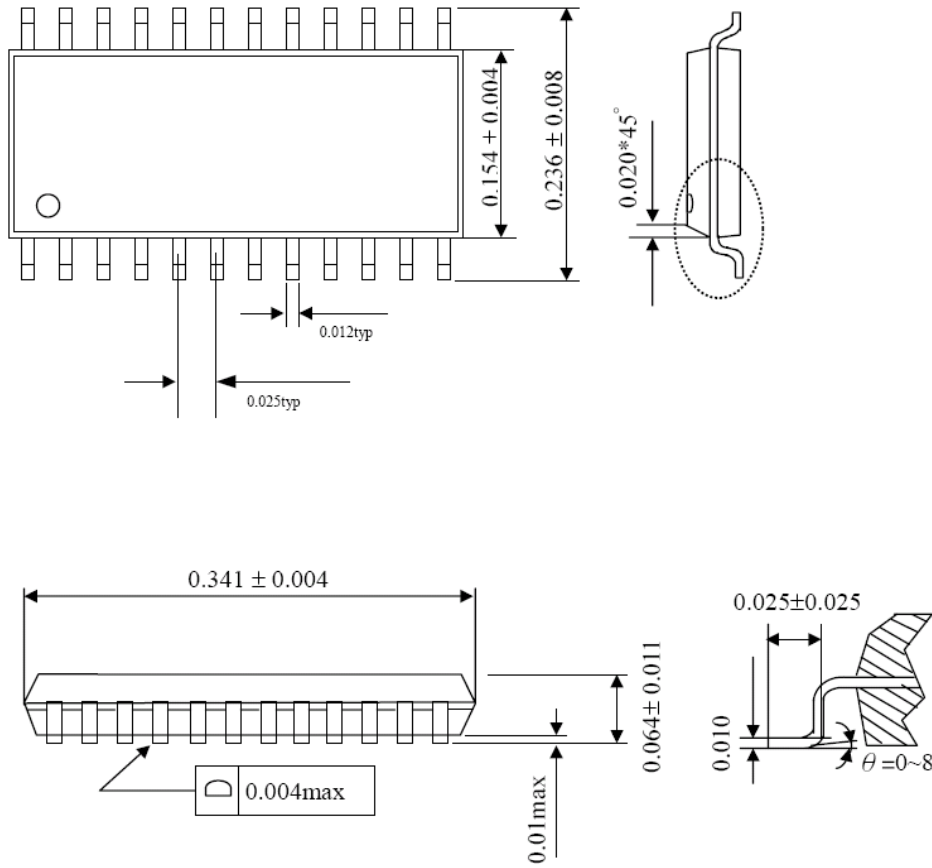
The PD(max) declines as the ambient temperature raises. Therefore, suitable operating conditions should be designed with caution according to the chosen package and the ambient temperature. The following figure illustrates the relation between the maximum power dissipation and the ambient temperature in the SSOP24/TSSOP20 packages.



Package Outline Dimension

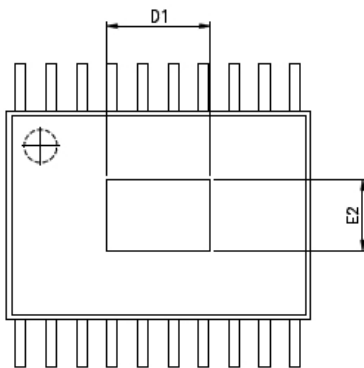
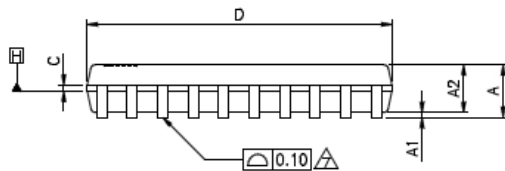
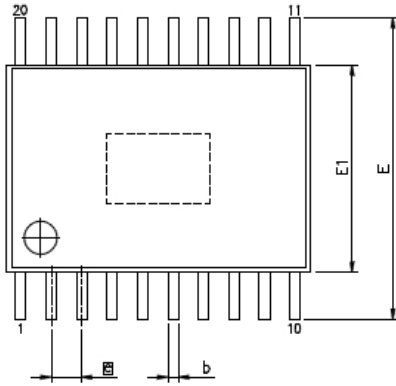
SSOP24-150mil-0.635mm

Unit: inch

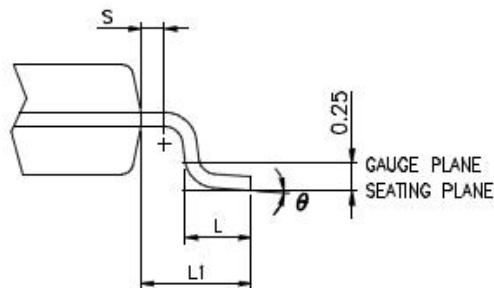
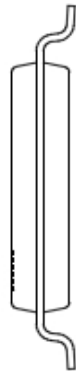


## Package Outline Dimension

TSSOP20-173mil-0.65mm



THERMALLY ENHANCED VARIATIONS ONLY



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	0.90	1.05
b	0.19	-	0.30
C	0.09	-	0.20
D	6.40	6.50	6.60
E1	4.30	4.40	4.50
E	6.40 BSC		
e	0.65 BSC		
L1	1.00 REF		
L	0.50	0.60	0.75
S	0.20	-	-
$\theta$	0°	-	8°

THERMALLY ENHANCED DIMENSIONS(SHOWN IN MM)

PAD SIZE	E2			D1		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
118X16E	2.60	2.80	3.00	3.79	3.99	4.19

NOTES:

- JEDEC OUTLINE :  
STANDARD : MO-153 AC REV.F  
THERMALLY ENHANCED : MO-153 ACT REV.F
- DIMENSION 'D' DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
- DIMENSION 'E1' DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
- DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE 'b' DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07 MM.
- DIMENSIONS 'D' AND 'E1' TO BE DETERMINED AT DATUM PLANE  $\square$ .



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