FSC-BT630

Bluetooth low energy 4.2 and 5 Specifications Module Datasheet

Version 1.0

Revision History

Version	Data	Notes	
1.0	2017/10/14	Initial Version	Devin Wan

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1. INTRODUCTION

Overview

FSC-BT630 is a wireless microcontroller (MCU) targeting Bluetooth 4.2 and Bluetooth 5 low energy applications.

Very low active RF and MCU current and low-power mode current consumption provide excellent battery lifetime and allow for operation on small coin cell batteries and in energy-harvesting applications.

FSC-BT630 contains a 32-bit ARM® Cortex®-M4 core that runs at 64 MHz as the main processor and a rich peripheral feature set that includes a unique ultra-low power sensor controller. This sensor controller is ideal for interfacing external sensors and for collecting analog and digital data autonomously while the rest of the system is in sleep mode. Thus, FSC-BT630 is great for a wide range of applications where long battery lifetime, small form factor, and ease of use is important.

It supports GAP, ATT/GATT, SMP, L2CAP profiles. It integrates Baseband controller in a small package (Integrated Ceramic antenna), so the designers can have better flexibilities for the product shapes.

Features

- Support the Bluetooth 4.2 core specification and 5 Specifications
- Low power
- RSSI (1 dB resolution)
- UART programming and data interface (baudrate can up to 921600bps)
- I2S audio interface
- I2C/AIO/PIO/PWM control interfaces
- Type 2 near field communication (NFC-A) tag with wakeup-on-field and touch-to-pair capabilities
- Postage stamp sized form factor
- Temperature sensor
- Digital microphone interface (PDM)
- Up to 3x SPI master/slave(Max)
- Quadrature decoder (QDEC)
- Embedded Bluetooth stack profiles support: SPP/iAP, HID, GATT, ANCS etc
- 3x real-time counter (RTC)
- OTA upgrade support
- MFI Support
- Support External Antenna
- RoHS compliant

Application

- Internet of Things (IoT)
  - Home automation
  - Sensor networks
  - Building automation
  - Industrial
  - Retail
- Personal area networks
  - Health/fitness sensor and monitor devices
  - Medical devices
  - Key fobs and wrist watches
- Interactive entertainment devices
  - Remote controls
  - Gaming controllers
- Beacons
  - A4WP wireless chargers and devices
  - Remote control toys
  - Computer peripherals and I/O devices: Mouse/Keyboard/Multi-touch track pad/Gaming

Module picture as below showing

Figure 1: FSC-BT630 Picture

2. General Specification

Table 1: General Specifications

Categories	Features	Implementation
Wireless Specification	Bluetooth Version	Bluetooth low energy (BLE) 4.2 and 5 Specifications
	Frequency	2.402 - 2.480 GHz
	Transmit Power	+4 dBm (Maximum)
	Receive Sensitivity	-96 dBm sensitivity in Bluetooth low energy mode (Typical)
	Antenna	2dBi Ceramic antenna
	Raw Data Rates (Air)	2 Mbps Bluetooth low energy mode 1 Mbps, 2 Mbps supported data rates
Host Interface and Peripherals	UART Interface	TX,RX,CTS/RTS(with EasyDMA)
		General Purpose I/O
		Default 115200,N,8,1
		Baudrate support from 1200 to 921600
		5, 6, 7, 8 data bit character(TBD)
	GPIO	13 (maximum – configurable) lines
		O/P drive strength (2~10 mA)
		Pull-up resistor (13 KΩ) control
		Read pin-level
	I2C Interface	Up to 2x I2C compatible 2-Wire master/slave (configurable from GPIO total)
		Up to 400 kbps(master)
	I2S Interface	Supports Master or Slave mode operation
		Simultaneous bi-directional (TX and RX) audio streaming
		Original I2S and left- or right-aligned format
		8, 16 and 24-bit sample width
		Low-jitter Master Clock generator
		Various sample rates
	ADC Interface	Analog input voltage range: 0~ VDD (VDD=3.6V)
		8/10/12-bit resolution, 14-bit resolution with oversampling
		6 channels (configured from GPIO total)
		Up to 200 ksps conversion
	PWM	16-bit resolution
		8-bit prescaler and clock divider
		Supports PWM interrupts
		supports input capture function
	PDM	Up to two PDM microphones configured as a Left/Right pair using the same data input
		16 kHz output sample rate, 16-bit samples
		EasyDMA support for sample buffering
		HW decimation filters
	NFC-A	13.56 MHz input frequency

	listen mode operation	Bit rate 106 kbps
	SPI	3 SPI instances(configurable from GPIO total)
		SPI Slave and SPI Master
		Bit rates for SPI Slave and Master - 8 Mbps
	Temperature sensor	Temperature range is greater than or equal to operating temperature of the device
		Resolution is 0.25 degrees
Profiles	Classic Bluetooth	No Support
	Bluetooth Low Energy	GATT Client & Peripheral - Any Custom Services
		BT5 Specifications
		MFI Support
Maximum Connections	Classic Bluetooth	No Support
	Bluetooth Low Energy	1Clients(TBD)
FW upgrade		Over the Air
		Via UART
		J-link
Supply Voltage	Supply	1.7 ~ 3.6V
Power Consumption		5.3 mA peak current in TX (0 dBm)
		6.6 mA peak current in TX (4 dBm)(TBD)
		5.4 mA peak current in RX
		~0.3uA - System OFF current, no RAM retention
		~1.2uA - System ON base current, no RAM retention
		~20nA - Additional RAM retention current per 4 KB RAM section
	Power fail comparator	<4uA - Current consumption when enabled
Physical	Dimensions	10mm X 11.9mm X 1.7mm; Pad Pitch 1.1mm
Environmental	Operating	-40°C to +85°C
	Storage	-40°C to +125°C
Miscellaneous	Lead Free	Lead-free and RoHS compliant
	Warranty	One Year
	Flash memory	Endurance: 10000(Write/erase cycles) Retention: 10 years at 40°C
Humidity		10% ~ 90% non-condensing
MSL grade:		MSL 1
ESD grade:		ESD HBM: 2KV ESD CDM: 500V

3. HARDWARE SPECIFICATION

3.1 Block Diagram and PIN Diagram

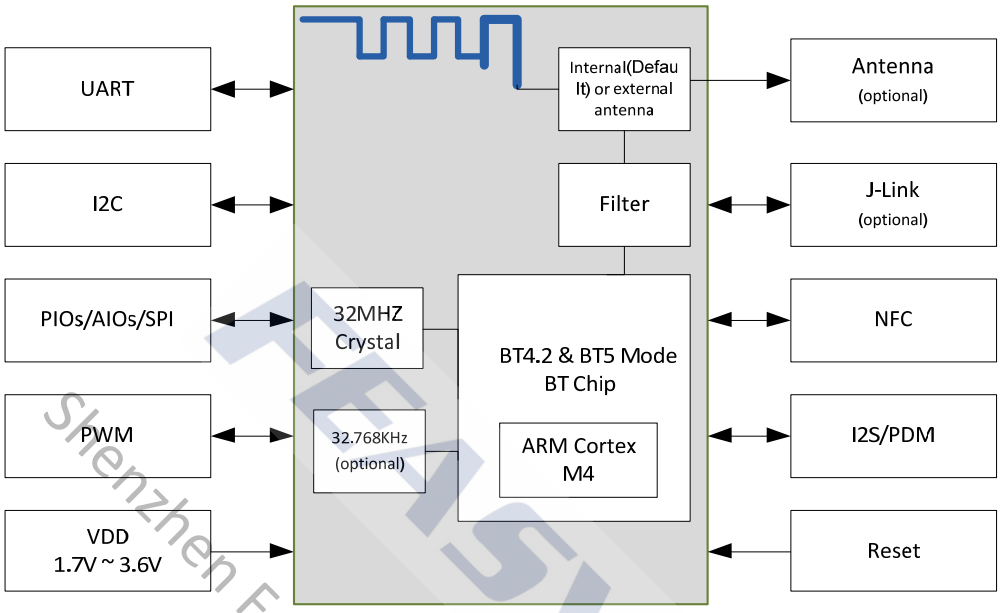


Figure 2: Block Diagram

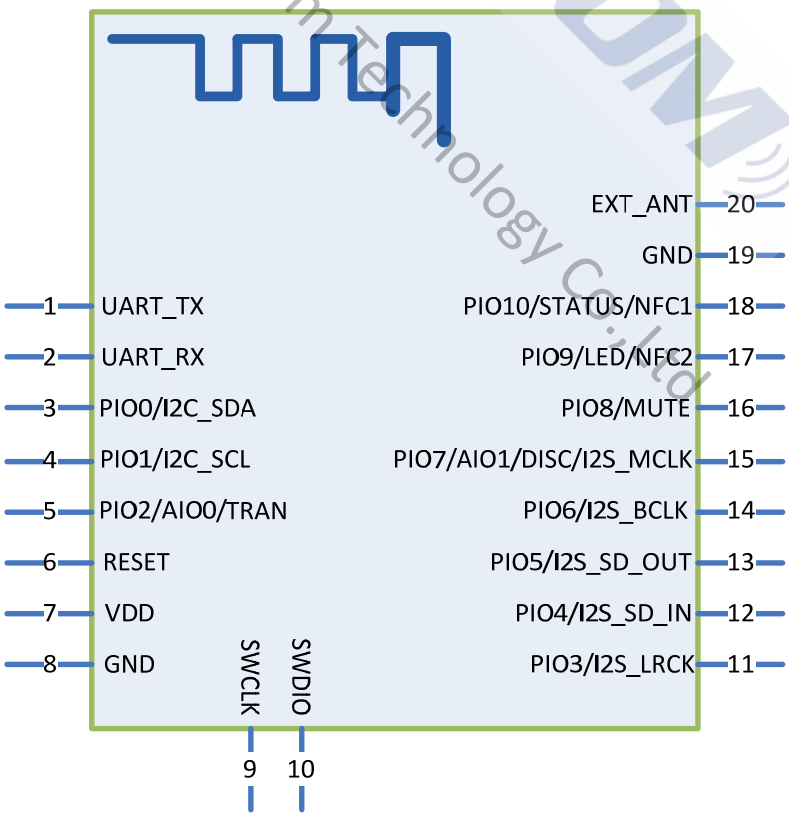


Figure 3: FSC-BT630 PIN Diagram(Top View)

3.2 PIN Definition Descriptions

Table 2: Pin definition

Pin	Pin Name	Type	Pin Descriptions	Notes
1	UART_TX	O	UART Data output	Note 1
2	UART_RX	I	UART Data input	Note 1
3	PIO0/I2C_SDA	I/O	Programmable input/output line	Note 2,3
4	PIO1/I2C_SCL	I/O	Programmable input/output line	Note 2,3
5	PIO2/AIO0/TRAN	I/O	Programmable input/output line Alternative Function 1: Analogue programmable I/O line. Alternative Function 2: Host MCU change UART transmission mode.	Note 2,4
6	RESET	I	External reset input: Active LOW, with an inter an internal pull-up. Set this pin low reset to initial state.	Note 3
7	VDD_3V3	Vdd	Power supply voltage 1.7 ~ 3.6V(default 3.3V)	
8	GND	Vss	Power Ground	
9	SWCLK	I	Serial wire debug clock input for debugand programming	
10	SWDIO	I/O	Serial wire debug I/O for debug and programming	
11	PIO3/I2S_LRCK	I/O	Programmable input/output line Alternative Function 1: I2S left right channel clock Alternative Function 2: Analogue programmable I/O line.	Note 2
12	PIO4/I2S_SD_IN	I	Programmable input/output line Alternative Function 1: I^2S data input Alternative Function 2: Analogue programmable I/O line.	Note 2
13	PIO5/I2S_SD_OUT	O	Programmable input/output line Alternative Function 1: I^2S data out Alternative Function 2: Analogue programmable I/O line.	Note 2
14	PIO6/I2S_BCLK	I/O	Programmable input/output line Alternative Function 1: I^2S bit clock pin Alternative Function 2: Analogue programmable I/O line.	Note 2
15	PIO7/AIO1/DISC/I2S_MCLK	I/O	Programmable input/output line Alternative Function 1: Analogue programmable I/O line. Alternative Function 2: I^2S Master clock pin. Alternative Function 3: Host MCU disconnect bluetooth. Alternative Function 4: Analogue programmable I/O line.	Note 2,5
16	PIO8/MUTE	I/O	Programmable input/output line Alternative Function: Mute Pin	Note 6
17	PIO9/LED/NFC2	I/O	Programmable input/output line Alternative Function 1: LED Alternative Function 2: NFC2	Note 7
18	PIO10/STATUS/NFC1	I/O	Programmable input/output line Alternative Function 1: BT Status	Note 8

			Alternative Function 2: NFC1	
19	GND	Vss	Power Ground	
20	EXT_ANT	O	RF signal output .	Note 9

Module Pin Notes:

Note 1	For customized module, this pin can be work as I/O Interface.
Note 2	I2C/PWM/SPI/PDM/UART(CTS/RTS) with EasyDMA (Support accomplishing the port mapping to other spare I/O Interface via modifying the firmware.)
Note 3	I2C Serial Clock and Data. It is essential to remember that pull-up resistors on both SCL and SDA lines are not provided in the module and MUST be provided external to the module.
Note 4	When bluetooth connection established, UART transmission mode will be determined by PIO2's level : High: Command Mode Low: Throughput Mode
Note 5	When bluetooth connection established,a riging edge of PIO7 will cause disconnection with remote device.
Note 6	Audio Mute Pin-- Mute ON: High Level; Mute OFF: Low Level.
Note 7	LED(Default)-- Power On: Light Slow Shinning ; Connected: Steady Lighting.
Note 8	BT Status(Default)-- Disconnected: Low Level; Connected: High Level.
Note 9	By default, this PIN is an empty feet. This PIN can connect to an external antenna to improve the Bluetooth signal coverage. If you need to use an external antenna, by modifying the module on the 0R resistance to block out the on-board antenna; Or contact Feasycom for modification.

4. PHYSICAL INTERFACE

4.1 Power Supply

The transient response of the regulator is important. If the power rails of the module are supplied from an external voltage source, the transient response of any regulator used should be 20μs or less. It is essential that the power rail recovers quickly.

This module has the following power supply features:

- On-chip LDO and DC/DC regulators
- Global System ON/OFF modes
- Individual RAM section power control for all system modes
- Analog or digital pin wakeup from System OFF
- Supervisor HW to manage power on reset, brownout, and power fail
- Auto-controlled refresh modes for LDO and DC/DC regulators to maximize efficiency
- Automatic switching between LDO and DC/DC regulator based on load to maximize efficiency

4.2 Reset

The module may be reset from several sources: Power-on Reset (POR), Low level on the nRESET Pin (nRST), Watchdog time-out reset (WDT), Wakeup from System OFF mode reset , Brown-out reset or Software Reset(SYSRESETREQ, CPU Reset, CHIPRST).

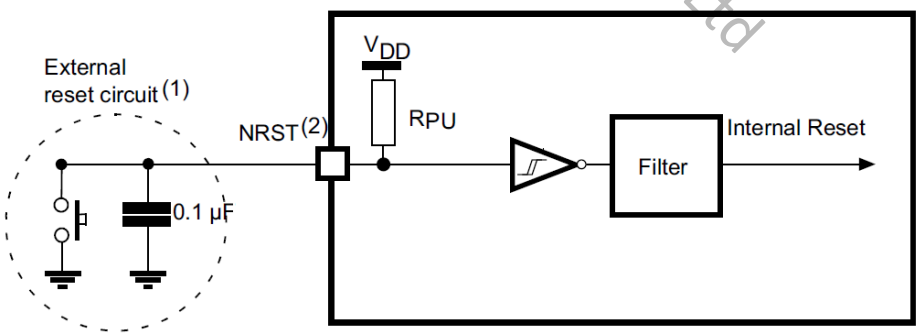
The RESET pin is an active low reset and is internally filtered using the internal low frequency clock oscillator. A reset will be performed between 1.5 and 4.0ms following RESET being active. It is recommended that RESET be applied for a period greater than 5ms.

At reset the digital I/O pins are set to inputs for bi-directional pins and outputs are tri-state. The PIOs have weak pull-ups.

Table 3: NRST pin characteristics

Parameter	Conditions	Min	Typ	Max	Unit
R_{PU} - Weak pull-up equivalent resistor(1)	VIN = VSS	30	40	50	KΩ
$V_{F(NRST)}$(2) - NRST Input filtered pulse		-	-	100	ns
$V_{NF(NRST)}$(2) - NRST Input not filtered pulse	VDD>1.2V	300	-	-	ns
T_{NRST_OUT} - Generated reset pulse duration	Internal Reset source	20	-	-	µs
V_{POF} - Nominal power level warning thresholds (falling supply voltage). Levels are configurable between Min. and Max. in 100mV increments.		1.7		2.8	V
$V_{BOR,OFF}$ - Brown out reset voltage range SYSTEM OFF mode		1.2		1.7	V
$V_{BOR,ON}$ - Brown out reset voltage range SYSTEM ON mode		1.5		1.7	V

1. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).
2. Guaranteed by design.



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the VIL(NRST) max level specified in *NRST pin characteristics*. Otherwise the reset is not taken into account by the device.

Figure 4： Recommended NRST pin protection

4.3 General Purpose Analog IO

The ADC is a differential successive approximation register (SAR) analog-to-digital converter.

Listed here are the main features of SAADC:

- 8/10/12-bit resolution, 14-bit resolution with oversampling
- Up to eight input channels
  - One channel per single-ended input and two channels per differential input
  - Scan mode can be configured with both single-ended channels and differential channels.
- Full scale input range (0 to VDD)
- Sampling triggered via a task from software or a PPI channel for full flexibility on sample frequency source from low power 32.768kHz RTC or more accurate 1/16MHz Timers
- One-shot conversion mode to sample a single channel
- Scan mode to sample a series of channels in sequence. Sample delay between channels is tack + tconv which may vary between channels according to user configuration of tack.
- Support for direct sample transfer to RAM using EasyDMA
- Interrupts on single sample and full buffer events
- Samples stored as 16-bit 2's complement values for differential and single-ended sampling
- Continuous sampling without the need of an external timer
- Internal resistor string
- Limit checking on the fly

4.4 General Purpose Digital IO

There are 13 general purpose digital IOs defined in the module. All these GPIOs can be configured by software to realize various functions, such as button controls, LED drives or interrupt signals to host controller, etc. Do not connect them if not use.

The I/O type of each I/O pins can be configured by software individually as Input or Push-pull output mode. After the chip is reset, the I/O mode of all pins is input mode with no pull-up and pull-down enable. Each I/O pin has an individual pull-up and pull-down resistor which is about 40 kΩ for VDD and Vss.

- Configurable output drive strength
- Internal pull-up and pull-down resistors
- Wake-up from high or low level triggers on all pins
- Trigger interrupt on state changes on any pin
- All pins can be used by the PPI task/event system
- One or more GPIO outputs can be controlled through PPI and GPIOTE channels
- All pins can be individually mapped to interface blocks for layout flexibility
- GPIO state changes captured on SENSE signal can be stored by LATCH register

4.5 I2S Interfaces

The I2S (Inter-IC Sound) module, supports the original two-channel I2S format, and left or right-aligned formats. It implements EasyDMA for sample transfer directly to and from RAM without CPU intervention.

The I2S peripheral has the following main features:

- Master and Slave mode
- Simultaneous bi-directional (TX and RX) audio streaming
- Original I2S and left- or right-aligned format
- 8, 16 and 24-bit sample width
- Low-jitter Master Clock generator
- Various sample rates

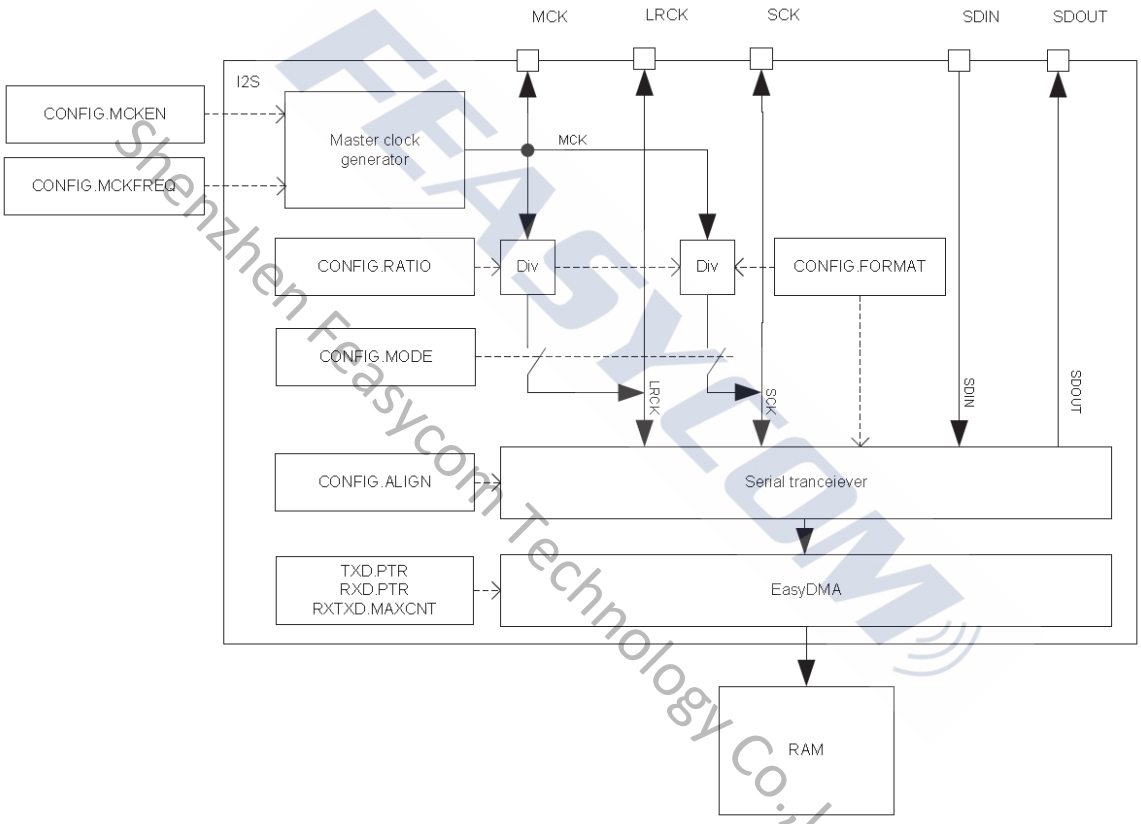


Figure 5: I2S master

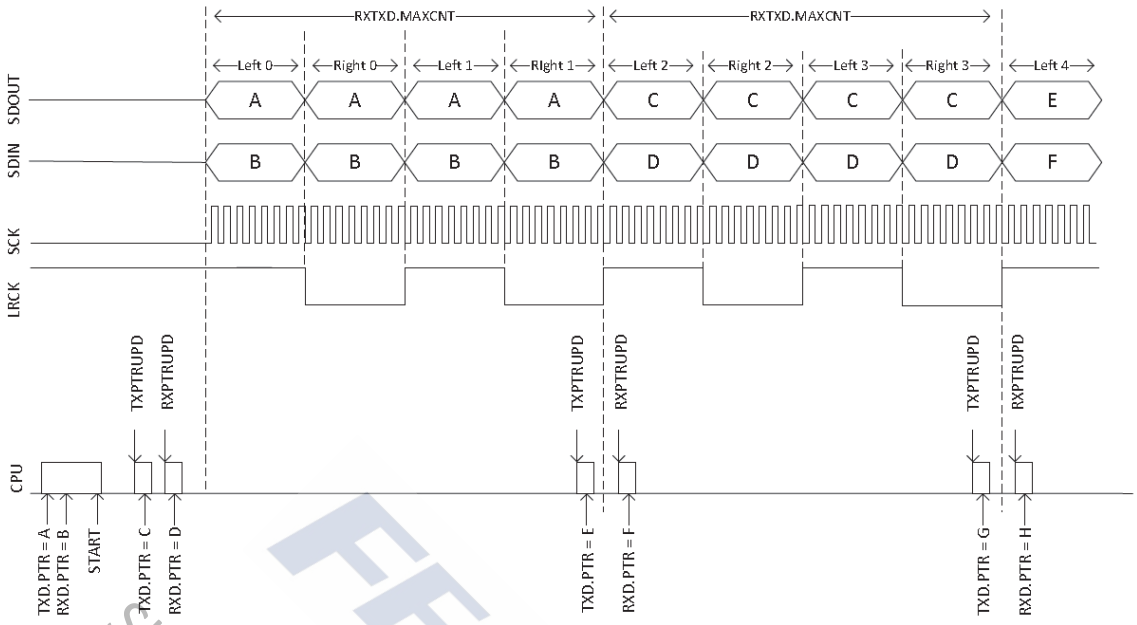


Figure 6: Transmitting and receiving. CONFIG.FORMAT = Aligned, CONFIG.SWIDTH = 8Bit,CONFIG.CHANNELS = Stereo, RXTXD.MAXCNT = 1.

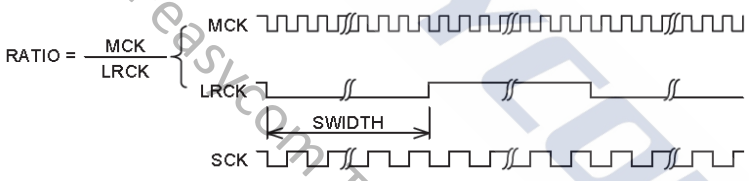


Figure 7: Relation between RATIO, MCK and LRCK

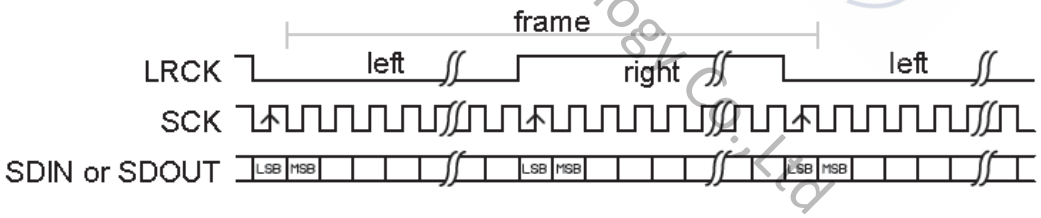


Figure 8: I2S format. CONFIG.SWIDTH equalling half-frame size.

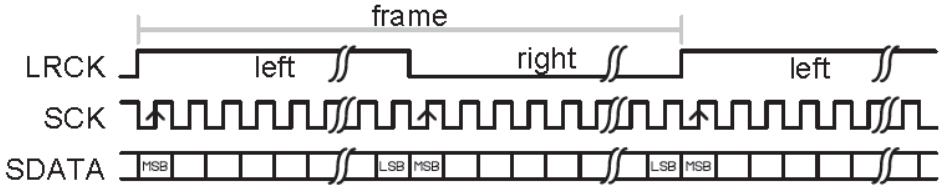


Figure 9: Aligned format. CONFIG.SWIDTH equalling half-frame size

4.6 SPI Interfaces

The SPI master provides a simple CPU interface which includes a TXD register for sending data and an RXD register for receiving data. This section is added for legacy support for now.

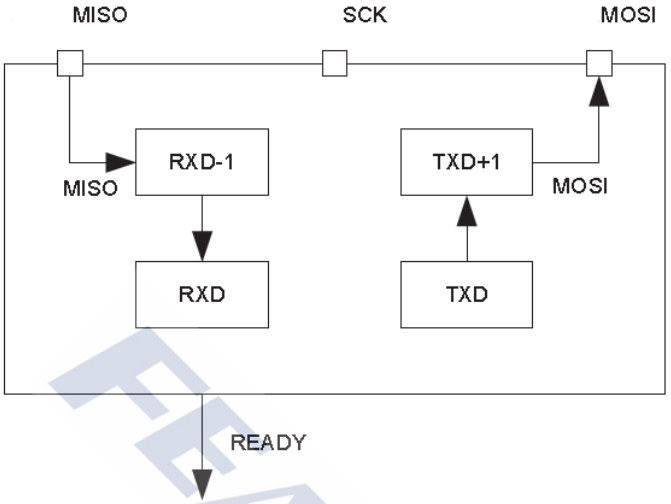


Figure 10: SPI master

The TXD and RXD registers are double-buffered to enable some degree of uninterrupted data flow in and out of the SPI master.

The SPI master does not implement support for chip select directly. Therefore, the CPU must use available GPIOs to select the correct slave and control this independently of the SPI master. The SPI master supports SPI modes 0 through 3.

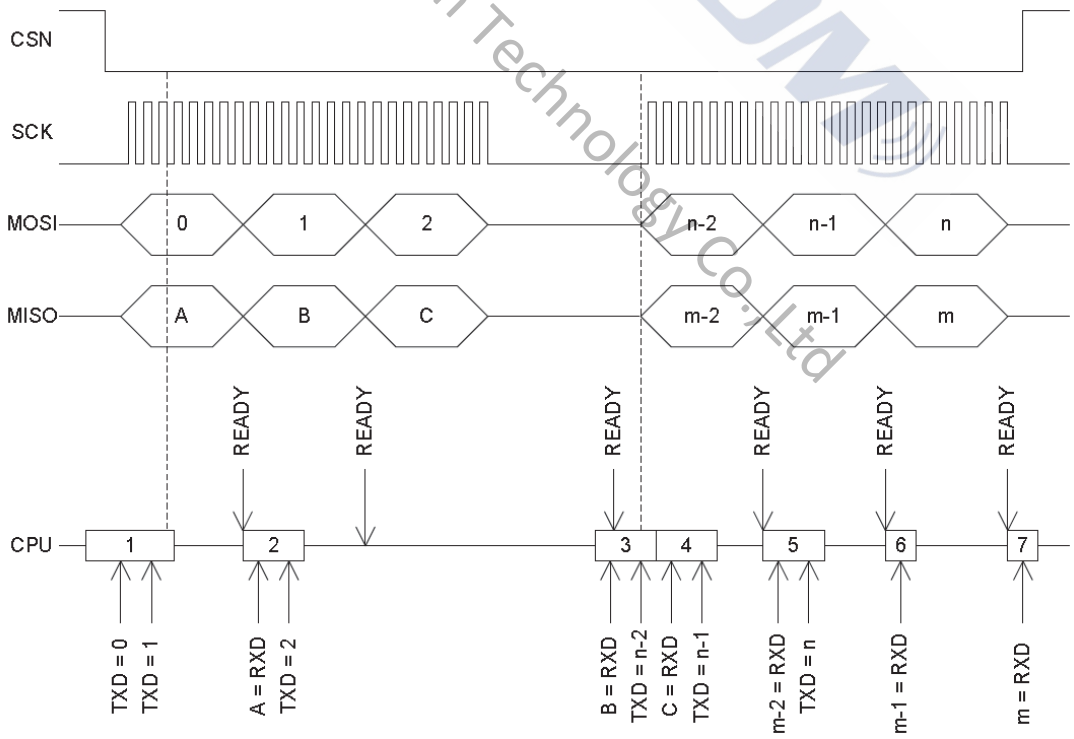


Figure 11: SPI master transaction sequence 1

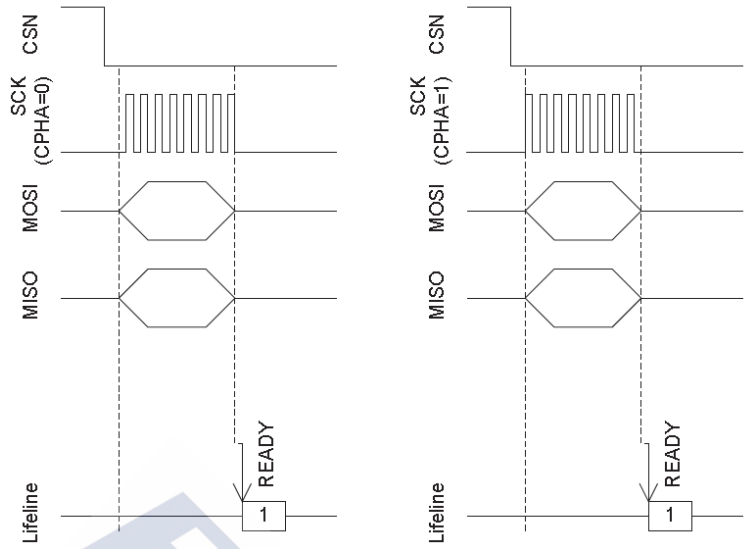


Figure 12: SPI master transaction sequence 2

4.7 RF Interface

For this Module, the default mode for antenna is internal ,it also has the interface for external antenna. If you need to use an external antenna, by modifying the module on the 0R resistance to block out the on-board antenna; Or contact Feasycom for modification.The user can connect a 50 ohm antenna directly to the RF port.

- 2402–2480 MHz Bluetooth 4.2 and Bluetooth 5
- 2 Mbps Bluetooth low energy mode
- 1 Mbps, 2 Mbps supported data rates
- TX power -20 to +4 dBm in 4 dB steps
- -96 dBm sensitivity in Bluetooth® low energy mode
- Single-pin antenna interface
- RSSI (1 dB resolution)

The RADIO includes a Device Address Match unit and an interframe spacing control unit that can be utilized to simplify address white listing and interframe spacing respectively, in Bluetooth Smart and similar applications.

The RADIO also includes a Received Signal Strength Indicator (RSSI) and a bit counter. The bit counter generates events when a preconfigured number of bits have been sent or received by the RADIO.

4.8 Serial Interfaces

4.8.1 UART

FSC-BT630 provides one channels of Universal Asynchronous Receiver/Transmitters(UART)(Full-duplex asynchronous communications). The UART Controller performs a serial-to-parallel conversion on data received from the peripheral and a parallel-to-serial conversion on data transmitted from the CPU. Each UART Controller channel supports ten types of interrupts.

This is a standard UART interface for communicating with other serial devices. The UART interface provides a simple mechanism for communicating with other serial devices using the RS232 protocol.

When the module is connected to another digital device, UART_RX and UART_TX transfer data between the two devices. The remaining two signals, UART_CTS and UART_RTS, can be used to implement RS232 hardware flow control where both are active low indicators.

This module output is at 3.3V CMOS logic levels (tracks VCC). Level conversion must be added to interface with an RS-232 level compliant interface.

Some serial implementations link CTS and RTS to remove the need for handshaking. We do not recommend linking CTS and RTS except for testing and prototyping. If these pins are linked and the host sends data when the FSC-BT630 deasserts its RTS signal, there is significant risk that internal receive buffers will overflow, which could lead to an internal processor crash. This drops the connection and may require a power cycle to reset the module. We recommend that you adhere to the correct CTS/RTS handshaking protocol for proper operation.

- Full-duplex operation
- Automatic hardware flow control
- Parity checking and generation for the 9th data bit
- EasyDMA
- Up to 1 Mbps baudrate
- Return to IDLE between transactions supported (when using HW flow control)
- One stop bit
- Least significant bit (LSB) first

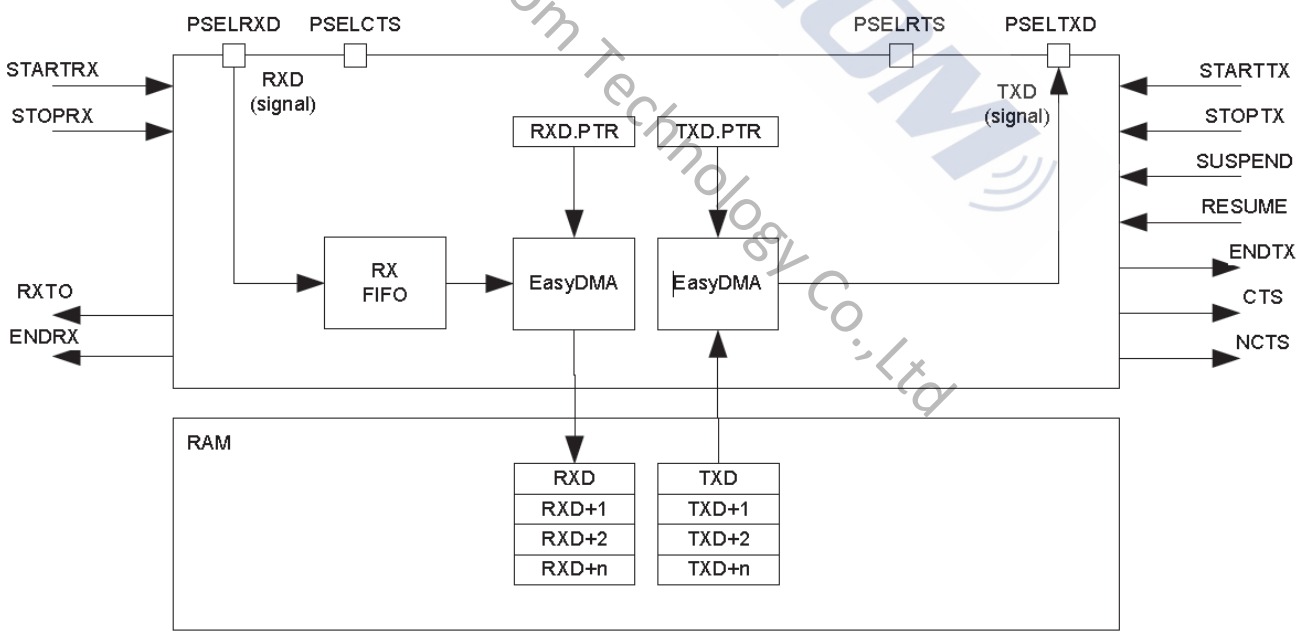


Figure 13: UART configuration

The GPIOs used for each UART interface can be chosen from any GPIO on the device and are independently configurable. This enables great flexibility in device pinout and efficient use of board space and signal routing.

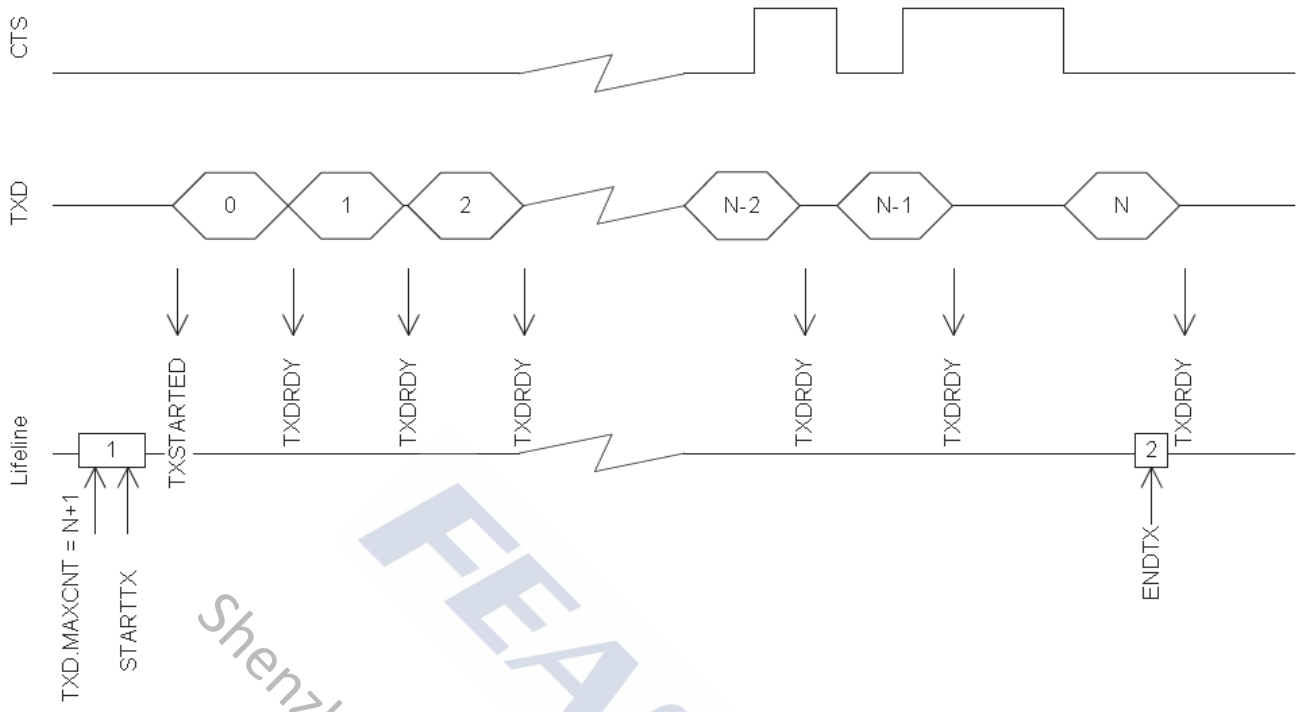


Figure 14: UART transmission

Table 4: Possible UART Settings

Parameter	Possible Values	
Baudrate	Minimum	1200 baud (≤2%Error)
	Standard	115200bps(≤1%Error)
	Maximum	921600bps(≤1%Error)
Flow control		RTS/CTS, or None
Parity		None, Odd or Even
Number of stop bits		1
Bits per channel		8

When connecting the module to a host, please make sure to follow .

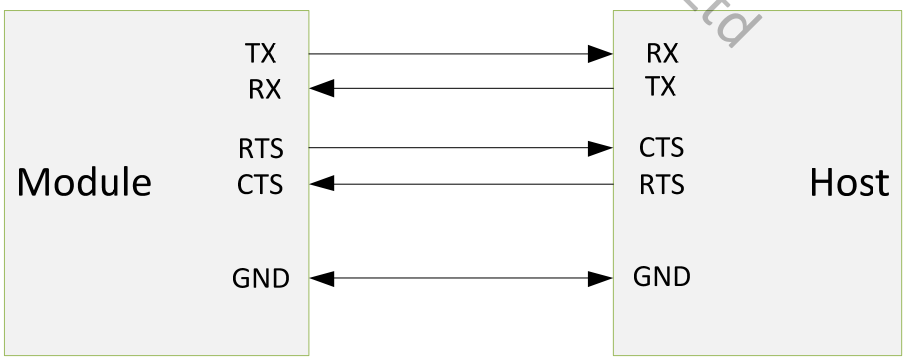


Figure 15: UART Connection

4.8.2 I2C Interface

I2C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I2C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously.

Data is transferred between a Master and a Slave synchronously to SCL on the SDA line on a byte-by-byte basis. Each data byte is 8-bit long. There is one SCL clock pulse for each data bit with the MSB being transmitted first. An acknowledge bit follows each transferred byte. Each bit is sampled during the high period of SCL; therefore, the SDA line may be changed only during the low period of SCL and must be held stable during the high period of SCL. A transition on the SDA line while SCL is high is interpreted as a command (START or STOP). Please refer to the following figure for more details about I2C Bus Timing.

The device on-chip I2C logic provides the serial interface that meets the I2C bus standard mode specification. The I2C port handles byte transfers autonomously. The I2C H/W interfaces to the I2C bus via two pins: SDA and SCL. Pull up resistor is needed for I2C operation as these are open drain pins. When the I/O pins are used as I2C port, user must set the pins function to I2C in advance.

The I2C master is compatible with I2C operating at 100 kHz and 400 kHz.

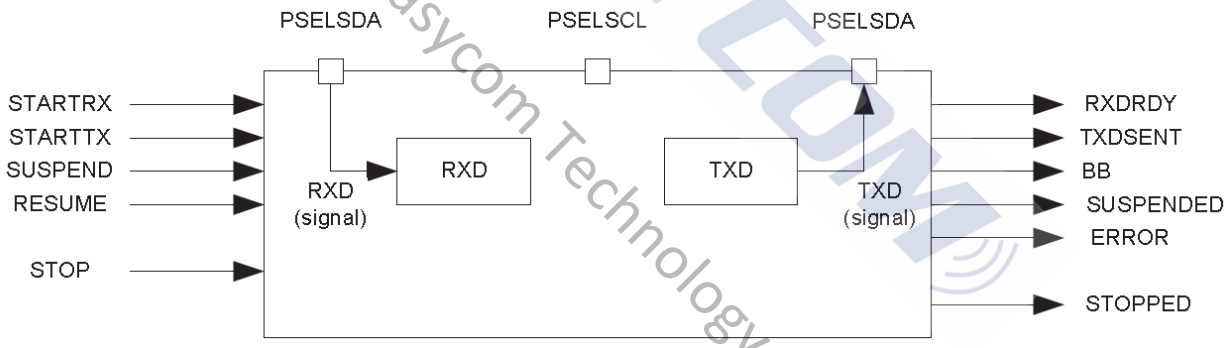


Figure 16: I2C master's main features

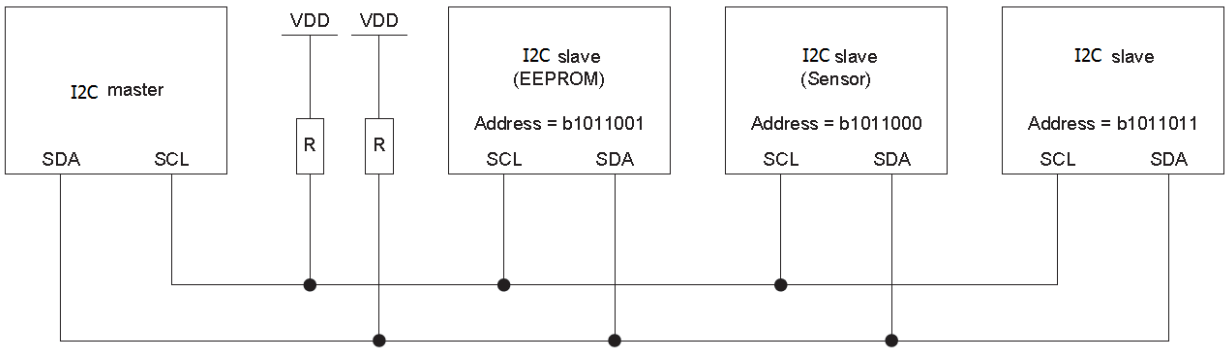


Figure 17: A typical I2C setup comprising one master and three slaves

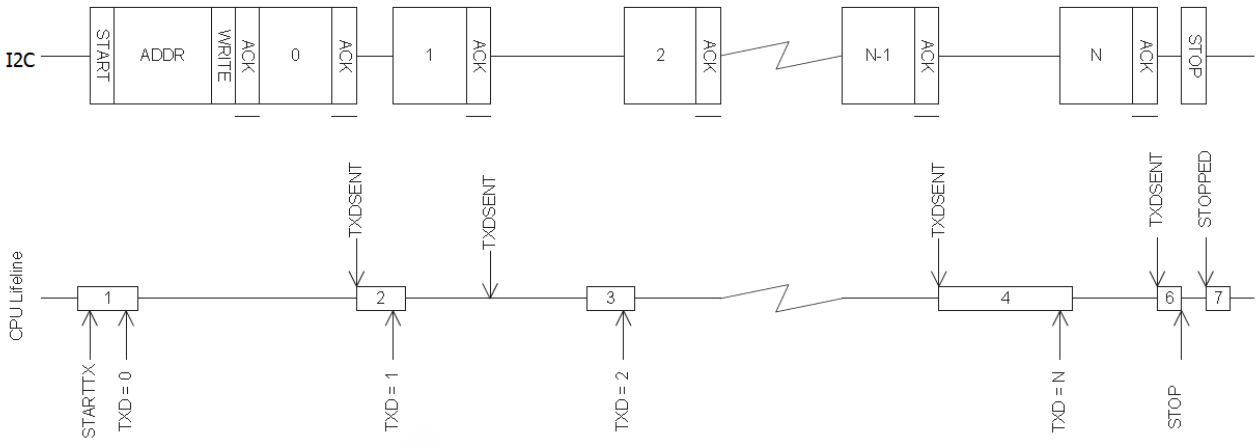


Figure 18: The I2C master writing data to a slave

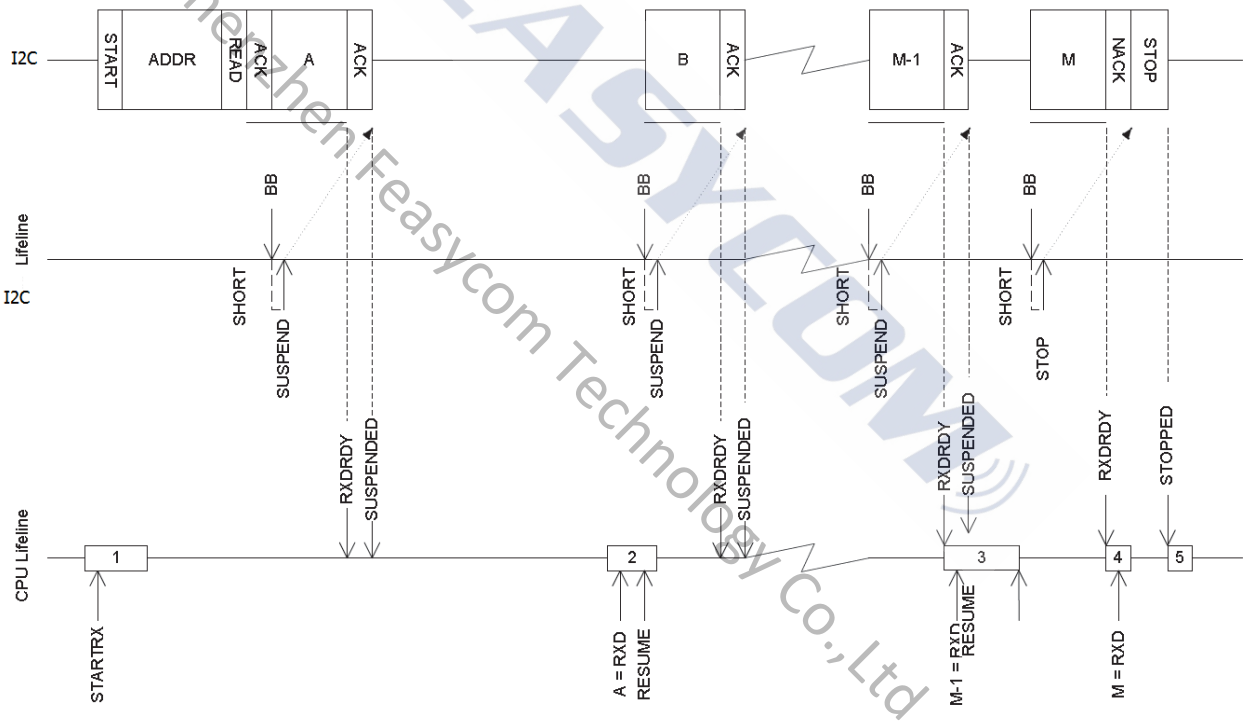


Figure 19: The I2C master reading data from a slave

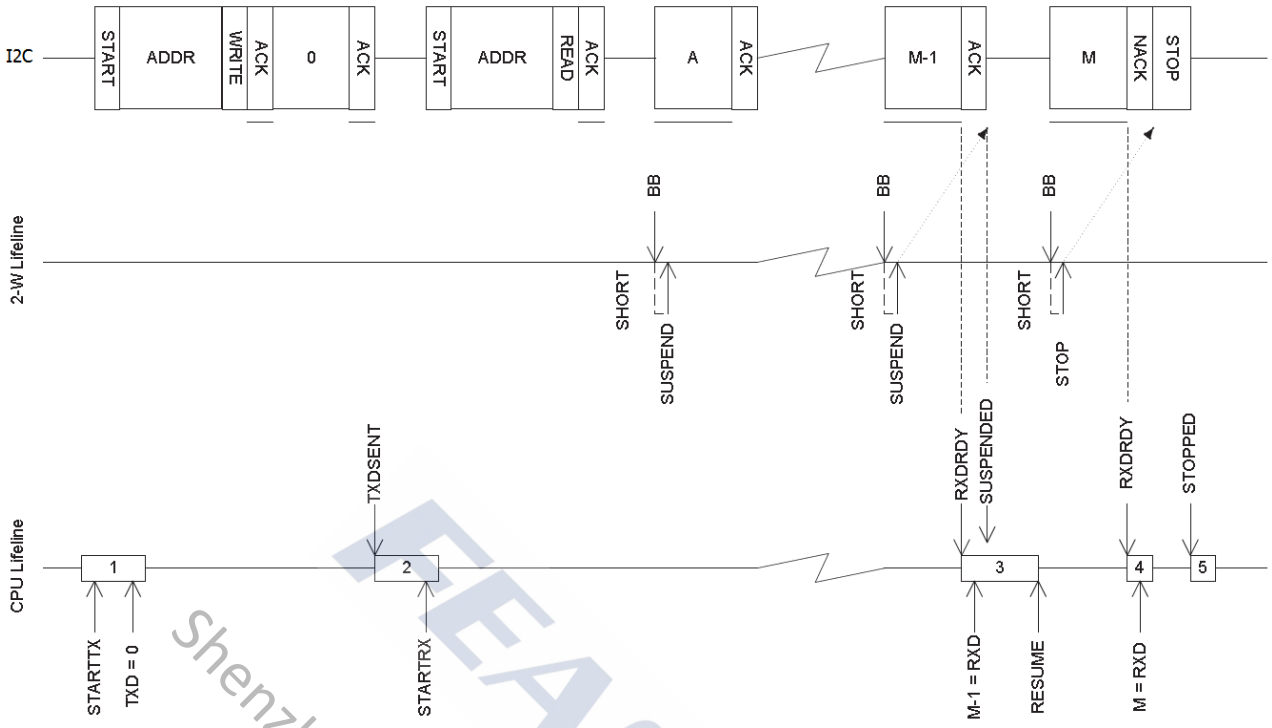


Figure 20: A repeated start sequence, where the I2C master writes one byte, followed by reading M bytes from the slave without performing a stop in-between

4.9 Pulse width modulation (PWM)

The PWM module enables the generation of pulse width modulated signals on GPIO. The module implements an up or up-and-down counter with four PWM channels that drive assigned GPIOs.

Three PWM modules can provide up to 12 PWM channels with individual frequency control in groups of up to four channels. Furthermore, a built-in decoder and EasyDMA capabilities make it possible to manipulate the PWM duty cycles without CPU intervention. Arbitrary duty-cycle sequences are read from Data RAM and can be chained to implement ping-pong buffering or repeated into complex loops.

Listed here are the main features of one PWM module:

- Fixed PWM base frequency with programmable clock divider
- Up to four PWM channels with individual polarity and duty-cycle values
- Edge or center-aligned pulses across PWM channels
- Multiple duty-cycle arrays (sequences) defined in Data RAM
- Autonomous and glitch-free update of duty cycle values directly from memory through EasyDMA
- Change of polarity, duty-cycle, and base frequency possibly on every PWM period
- Data RAM sequences can be repeated or connected into loops

4.10 Pulse density modulation interface (PDM)

The pulse density modulation (PDM) module enables input of pulse density modulated signals from external audio frontends, for example, digital microphones. The PDM module generates the PDM clock and supports single-channel or dual-channel (Left and Right) data input. Data is transferred directly to RAM buffers using EasyDMA.

Listed here are the main features for PDM:

- Up to two PDM microphones configured as a Left/Right pair using the same data input
- 16 kHz output sample rate, 16-bit samples
- EasyDMA support for sample buffering
- HW decimation filters
- The PDM module illustrated

The PDM module illustrated is interfacing up to two digital microphones with the PDM interface. It implements EasyDMA, which relieves real-time requirements associated with controlling the PDM slave from a low priority CPU execution context. It also includes all the necessary digital filter elements to produce PCM samples. The PDM module allows continuous audio streaming.

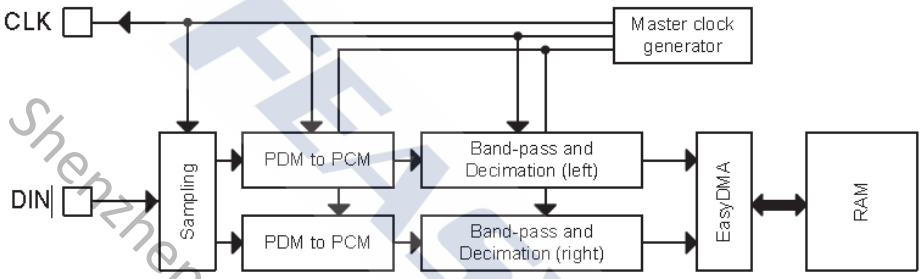


Figure 21: PDM module

4.10.1 Hardware example

Connect the microphone clock to CLK, and data to DIN.

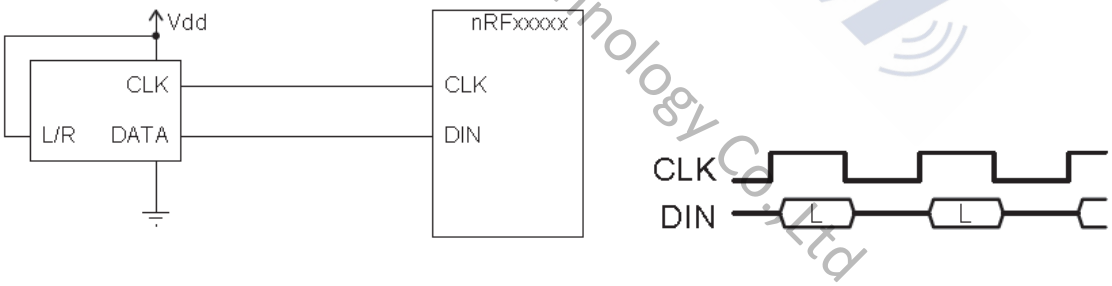


Figure 22: Example of a single PDM microphone, wired as left

Figure 23: Example of a single PDM microphone, wired as right

Note that in a single-microphone (mono) configuration, depending on the microphone's implementation, either the left or the right channel (sampled at falling or rising CLK edge respectively) will contain reliable data. If two microphones are used, one of them has to be set as left, the other as right (L/R pin tied high or to GND on the respective microphone). It is strongly recommended to use two microphones of exactly the same brand and type so that their timings in left and right operation match.

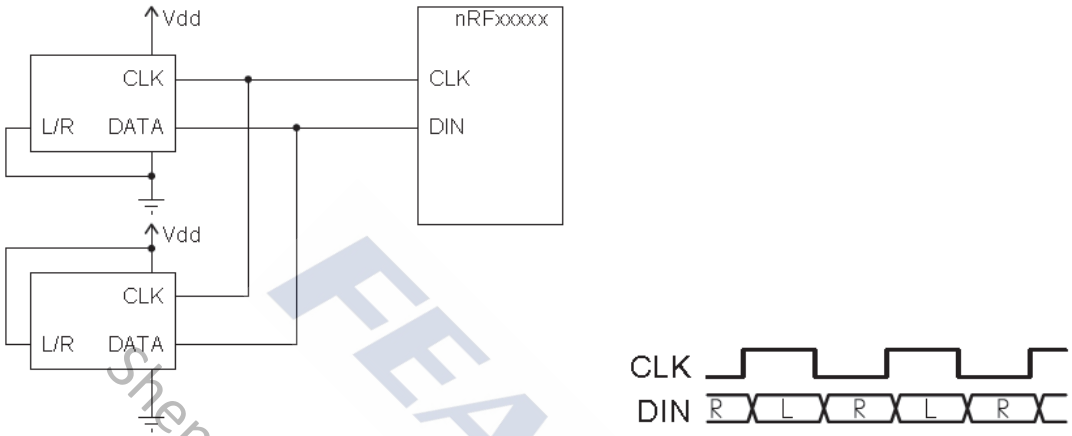


Figure 24: Example of two PDM microphones

4.11 Near field communication tag (NFC)

The NFC peripheral (referred to as the 'NFC peripheral' from now on) supports communication signal interface type A and 106 kbps bit rate from the NFC Forum.

With appropriate software, the NFC peripheral can be used to emulate the listening device NFC-A as specified by the NFC Forum.

Listed here are the main features for the NFC peripheral:

- NFC-A listen mode operation
  - 13.56 MHz input frequency
  - Bit rate 106 kbps
- Wake-on-field low power field detection (SENSE) mode
- Frame assemble and disassemble for the NFC-A frames specified by the NFC Forum
- Programmable frame timing controller
- Integrated automatic collision resolution, CRC and parity functions

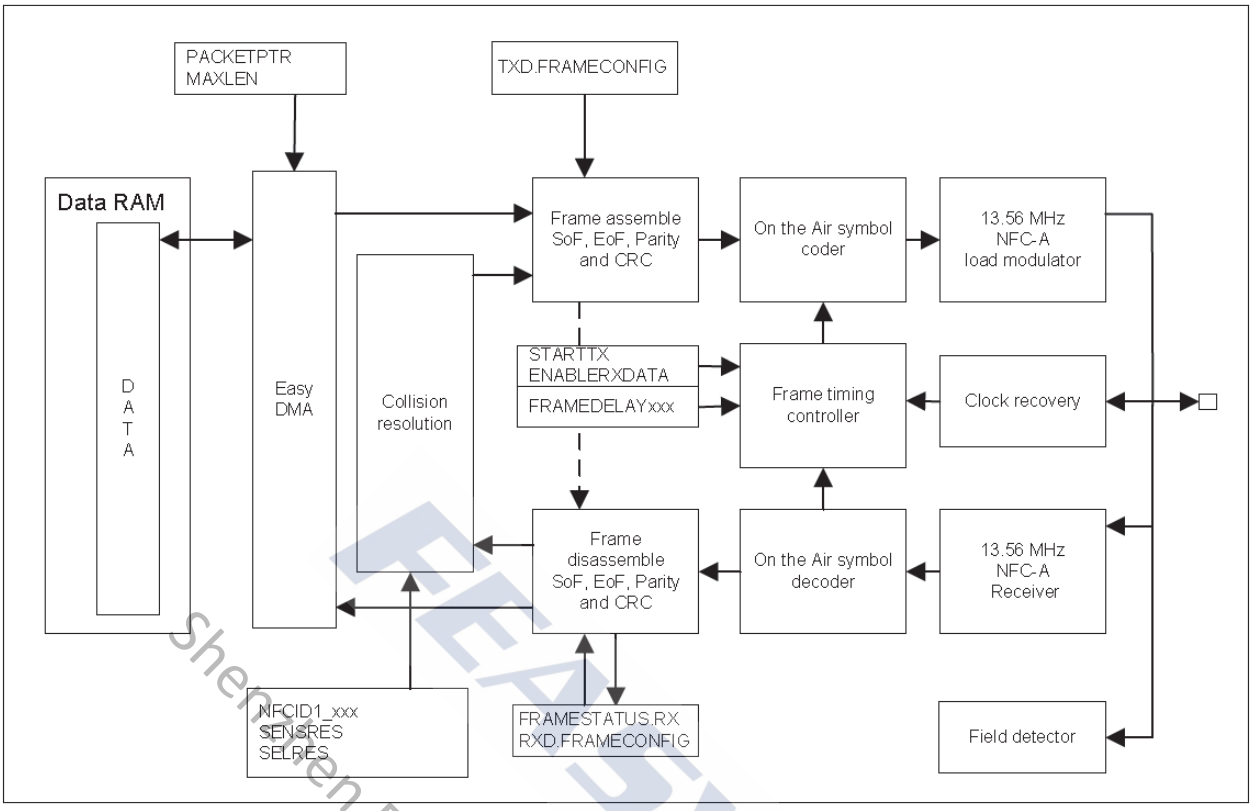


Figure 25: NFC block diagram

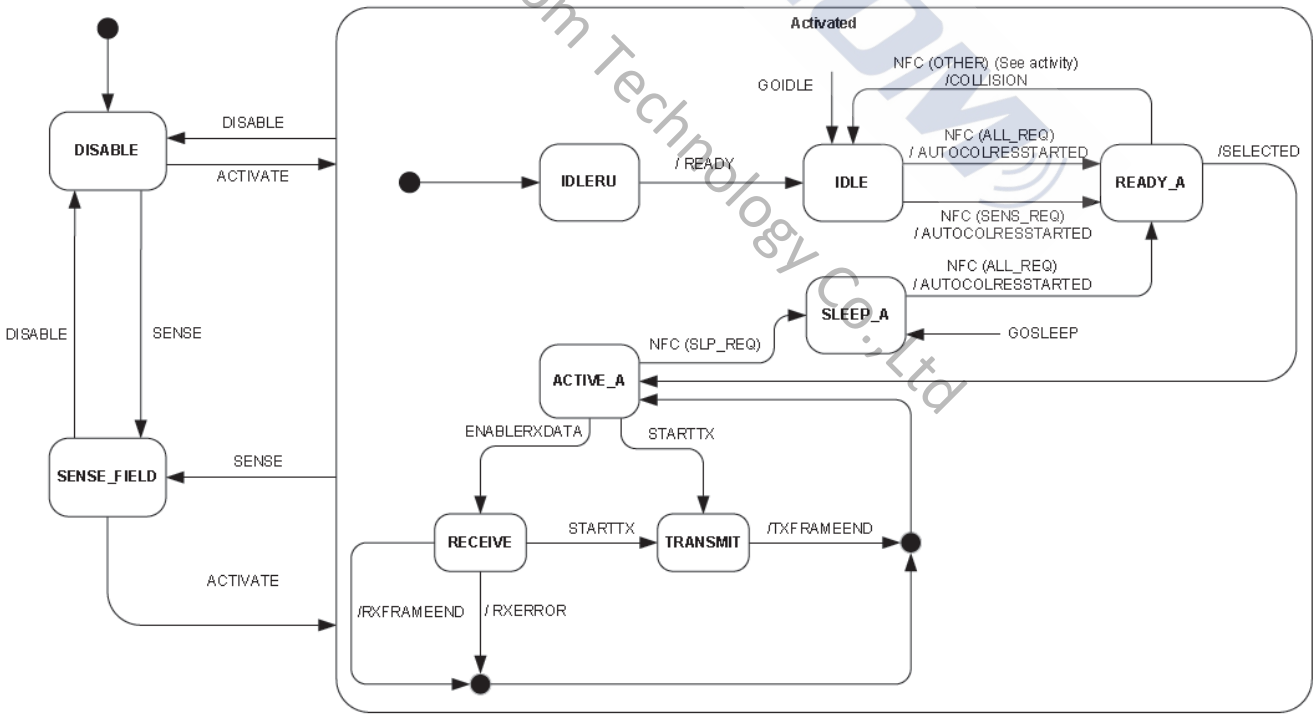


Figure 26: NFC state diagram

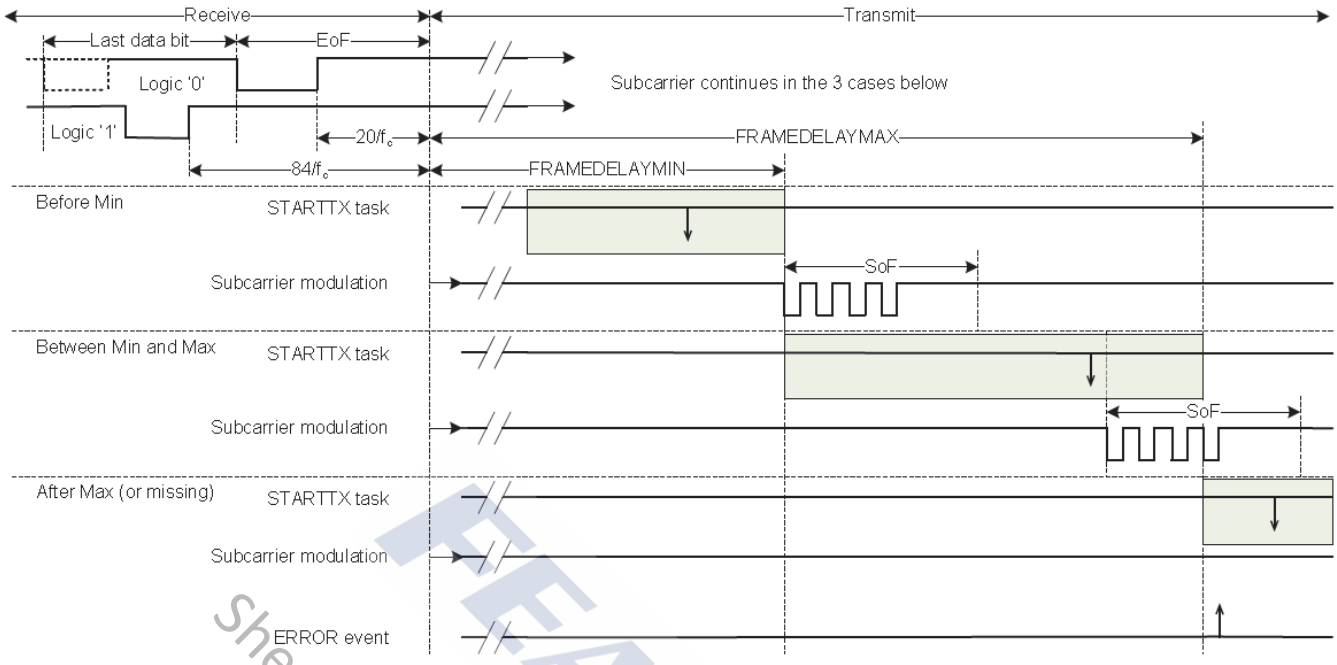


Figure 27: Frame timing controller (FRAMEDELAYMODE=Window)

4.11.1 Antenna interface

In ACTIVATED state, an amplitude regulator will adjust the voltage swing on the antenna pins to a value that is within the V_{swing} limit.

4.11.2 NFCT antenna recommendations

The NFCT antenna coil must be connected differential between NFC1 and NFC2 pins of the device.

Two external capacitors should be used to tune the resonance of the antenna circuit to 13.56MHz.

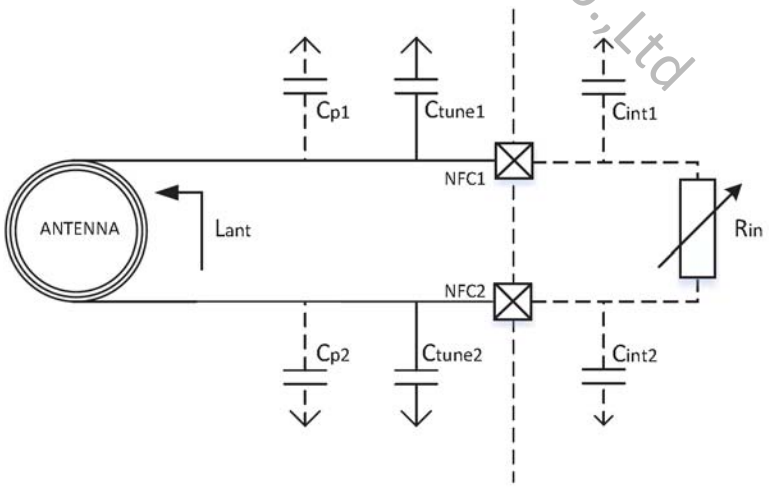


Figure 28: NFC antenna recommendations

The required tuning capacitor value is given by the below equations:

$$C'_{tune} = \frac{1}{(2\pi \cdot 13.56\ MHz)^2 \cdot L_{ant}} \quad where\ C'_{tune} = \frac{1}{2} \cdot (C_p + C_{\text{int}} + C_{tune})$$

$$and\ C_{tune1} = C_{tune2} = C_{tune} \qquad C_{p1} = C_{p2} = C_p \qquad C_{\text{int1}} = C_{\text{int2}} = C_{\text{int}}$$

$$C_{tune} = \frac{2}{(2\pi \cdot 13.56\ MHz)^2 \cdot L_{ant}} - C_p - C_{\text{int}}$$

An antenna inductance of L_{ant} = 2 µH will give tuning capacitors in the range of 130pF on each pin. For good performance, match the total capacitance on NFC1 and NFC2.

4.11.3 Battery protection

If the antenna is exposed to a strong NFC field, current may flow in the opposite direction on the supply due to parasitic diodes and ESD structures.

If the battery used does not tolerate return current, a series diode must be placed between the battery and the device in order to protect the battery.

4.11.4 References

NFC Forum, NFC Analog Specification version 1.0, www.nfc-forum.org

NFC Forum, NFC Digital Protocol Technical Specification version 1.1, www.nfc-forum.org

NFC Forum, NFC Activity Technical Specification version 1.1, www.nfc-forum.org

5. ELECTRICAL CHARACTERISTICS

5.1 Absolute Maximum Ratings

Absolute maximum ratings for supply voltage and voltages on digital and analogue pins of the module are listed below. Exceeding these values causes permanent damage.

The average PIO pin output current is defined as the average current value flowing through any one of the corresponding pins for a 100mS period. The total average PIO pin output current is defined as the average current value flowing through all of the corresponding pins for a 100mS period. The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

Table 5: Absolute Maximum Rating

Parameter	Min	Max	Unit
Supply voltages			
VDD	-0.3	+3.9V	V
VSS		0V	V
I/O pin voltage			
$V_{I/O}$, VDD ≤3.6 V	-0.3	VDD+0.3	V
$V_{I/O}$, VDD >3.6 V	-0.3	3.9V	V
NFC antenna pin current			
$I_{NFC1/2}$		80	mA
Radio			
RF input level		10	dBm
Environmental			
Storage temperature	-40	+125	℃

5.2 Recommended Operating Conditions

Table 6: Recommended Operating Conditions

Parameter	Min	Type	Max	Unit
V_{DD} - Supply voltage, independent of DCDC enable	1.7	3.0	3.6	V
t_{R_VDD} - Supply rise time (0 V to 1.7 V)			60	mS
T_A - Operating Temperature	-40	25	+85	℃

Important:

The on-chip power-on reset circuitry may not function properly for rise times longer than the specified maximum.

5.3 Input/output Terminal Characteristics

Table 7: GPIO Electrical Specification

Parameter	Min	Type	Max	Unit
V_{IH} - Input High Voltage	0.7xVDD	-	VDD	V
V_{IL} - Input Low Voltage	VSS	-	0.3xVDD	V
$V_{OH,HDH}$ - Output high voltage, standard drive, 0.5 mA, VDD ≥1.7	VDD-0.4	-	VDD	V
$V_{OH,HDH}$ - Output high voltage, high drive, 5 mA, VDD >= 2.7 V	VDD-0.4	-	VDD	V
$V_{OH,HDL}$ - Output high voltage, high drive, 3 mA, VDD >= 1.7 V	VDD-0.4	-	VDD	V
$V_{OL,SD}$ - Output low voltage, standard drive, 0.5 mA, VDD ≥1.7	VSS	-	VSS+0.4	V
$V_{OL,HDH}$ - Output low voltage, high drive, 5 mA, VDD >= 2.7 V	VSS	-	VSS+0.4	V
$V_{OL,HDL}$ - Output low voltage, high drive, 3 mA, VDD >= 1.7 V	VSS	-	VSS+0.4	V
$I_{OL,SD}$ - Current at VSS+0.4 V, output set low, standard drive, VDD ≥1.7	1	2	4	mA
$I_{OL,HDH}$ - Current at VSS+0.4 V, output set low, high drive, VDD >= 2.7 V	6	10	15	mA

$I_{OL,HDL}$ - Current at VSS+0.4 V, output set low, high drive, VDD >= 1.7 V	3	-	-	mA
$I_{OH,SD}$ - Current at VDD-0.4 V, output set high, standard drive, VDD ≥1.7	1	2	4	mA
$I_{OH,HDH}$ - Current at VDD-0.4 V, output set high, high drive, VDD >= 2.7 V	6	9	14	mA
$I_{OH,HDL}$ - Current at VDD-0.4 V, output set high, high drive, VDD >= 1.7 V	3	-	-	mA
$t_{RF,15pF}$ - Rise/fall time, low drive mode, 10-90%, 15 pF load1	-	9	-	nS
$t_{RF,25pF}$ - Rise/fall time, low drive mode, 10-90%, 25 pF load1	-	13	-	nS
$t_{RF,50pF}$ - Rise/fall time, low drive mode, 10-90%, 50 pF load1	-	25	-	nS
$t_{HRF,15pF}$ - Rise/Fall time, high drive mode, 10-90%, 15 pF load1	-	4	-	nS
$t_{HRF,25pF}$ - Rise/Fall time, high drive mode, 10-90%, 25 pF load1	-	5	-	nS
$t_{HRF,50pF}$ - Rise/Fall time, high drive mode, 10-90%, 50 pF load1	-	8	-	nS
R_{PU} - Pull-up resistance	11	13	16	KΩ
R_{PD} - Pull-down resistance	11	13	16	KΩ
C_{PAD} - Pad capacitance	-	3	-	pF
C_{PAD_NFC} - Pad capacitance on NFC pads	-	4	-	pF
I_{NFC_LEAK} - Leakage current between NFC pads when driven to different states	-	2	10	uA

The current drawn from the battery when GPIO is active as an output is calculated as follows:

$I_{GPIO}=V_{DD}\ C_{load}\ f$

C_{load} being the load capacitance and "f" is the switching frequency.

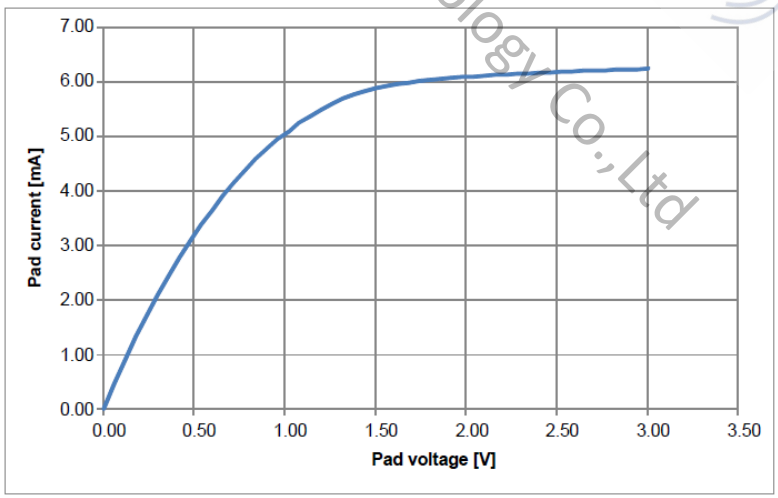


Figure 29: GPIO drive strength vs Voltage, standard drive, VDD = 3.0 V

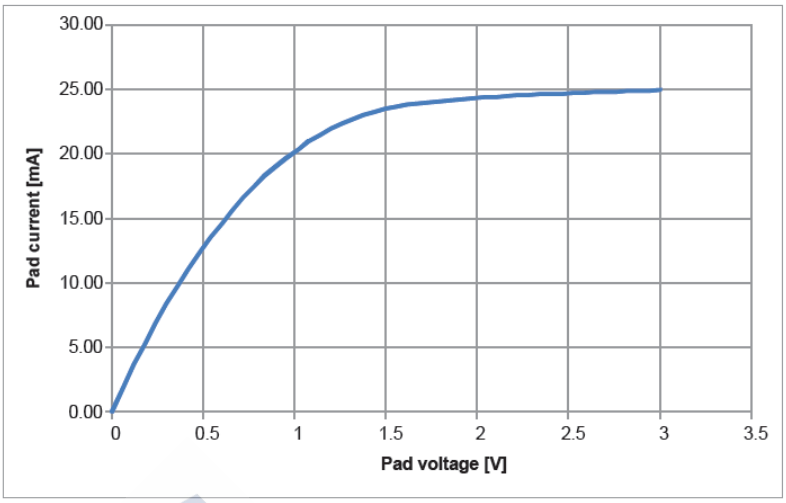


Figure 30: GPIO drive strength vs Voltage, high drive, VDD = 3.0 V

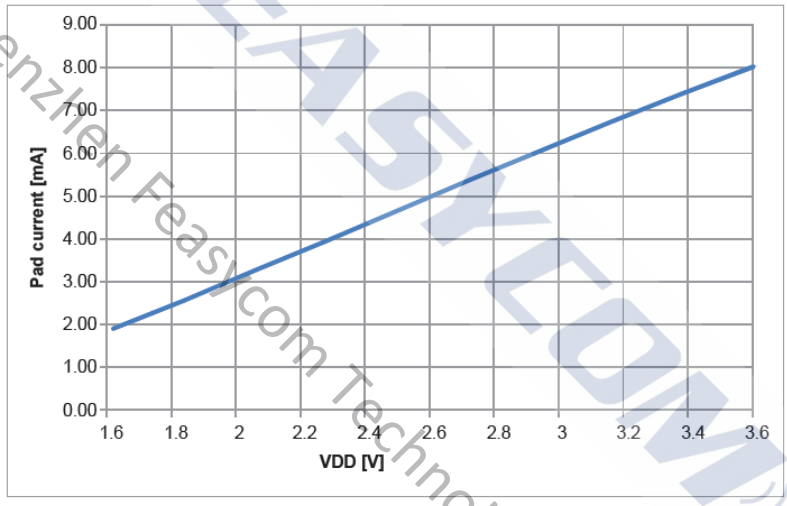


Figure 31: Max sink current vs Voltage, standard drive

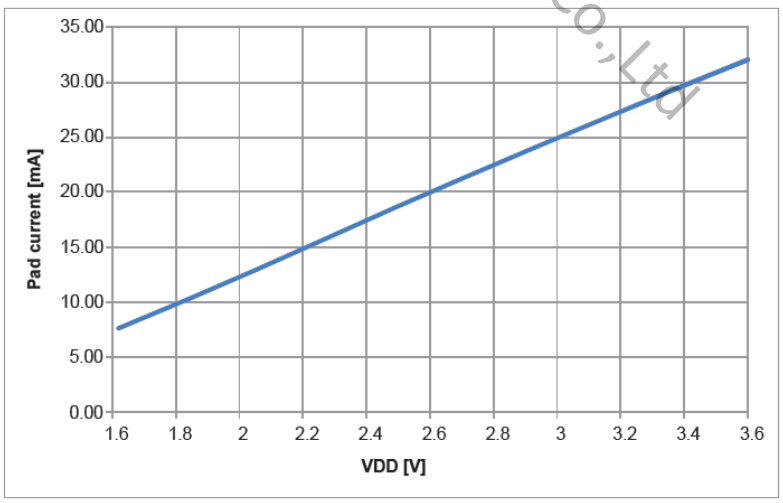


Figure 32: Max sink current vs Voltage, high drive

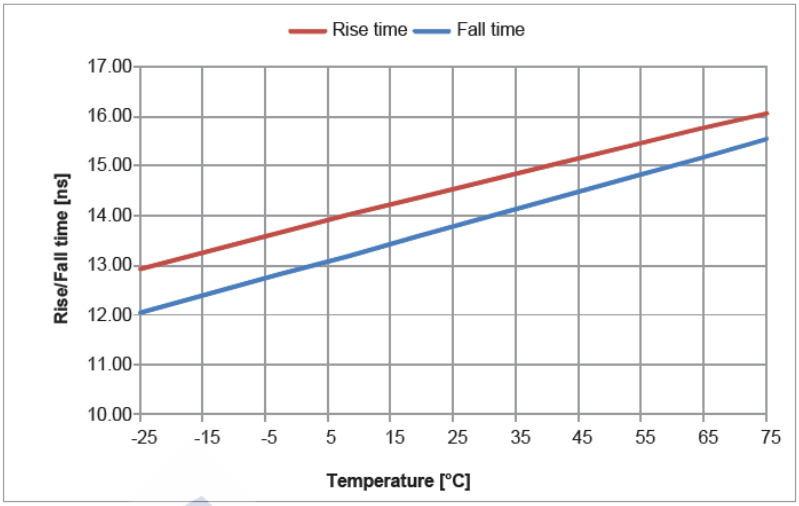


Figure 33: Rise and fall time vs Temperature, 10%-90%, 25pF load capacitance, VDD = 3.0 V

5.4 Analog Characteristics

5.4.1 ADC Electrical Specification

Table 8: ADC characteristics

Parameter	Min	Typ	Max	Unit
DNL - Differential non-linearity, 10-bit resolution	-0.95	<1	-	LSB
INL - Integral non-linearity, 10-bit resolution	-	1	-	LSB
V_{OS} - Differential offset error (calibrated), 10-bit resolution [a]	-	+-2	-	LSB
C_{EG} - Gain error temperature coefficient	-	0.02	-	%/°C
f_{SAMPLE} - Maximum sampling rate	-	-	200	kHz
$t_{ACQ,10k}$ - Acquisition time (configurable), source Resistance <= 10kOhm	-	3	-	µs
$t_{ACQ,40k}$ - Acquisition time (configurable), source Resistance <= 40kOhm	-	5	-	µs
$t_{ACQ,100k}$ - Acquisition time (configurable), source Resistance <= 100kOhm	-	10	-	µs
tACQ,200k - Acquisition time (configurable), source Resistance<=200kOhm	-	15	-	µs
$t_{ACQ,400k}$ - Acquisition time (configurable), source Resistance <= 400kOhm	-	20	-	µs
$t_{ACQ,800k}$ - Acquisition time (configurable), source Resistance <= 800kOhm	-	40	-	µs
t_{CONV} - Conversion time	-	<2	-	µs
$I_{ADC,CONV}$ - ADC current during ACQuisition and CONVersion	-	700	-	µA
$I_{ADC,IDLE}$ - Idle current, when not sampling, excluding clock sources and regulator base currents[33]	-	<5	-	µA
$E_{G1/6}$ - Errorb for Gain = 1/6	-3	-	3	%
$E_{G1/4}$ - Errorb for Gain = 1/4	-3	-	3	%
$E_{G1/2}$ - Errorb for Gain = 1/2	-3	-	4	%
E_{G1} - Errorb for Gain = 1	-3	-	4	%
C_{SAMPLE} - Sample and hold capacitance at maximum gain	-	2.5	-	pF
R_{INPUT} - Input resistance	-	>1	-	MΩ
E_{NOB} - Effective number of bits, differential mode, 12-bit resolution,	-	9	-	Bit

1/1 gain, 3 µs acquisition time, crystal HFCLK, 200 ksps				
S_{NDR} - Peak signal to noise and distortion ratio, differential mode, 12-bit resolution, 1/1 gain, 3 µs acquisition time, crystal HFCLK, 200ksps	-	56	-	dB
S_{FDR} - Spurious free dynamic range, differential mode, 12-bit resolution, 1/1 gain, 3 µs acquisition time, crystal HFCLK, 200ksps	-	70	-	dBc
R_{LADDER} - Ladder resistance	-	160	-	kΩ

a :Digital output code at zero volt differential input.

33 :When t_{ACQ} is 10us or longer, and if DC/DC is active, it will be allowed to work in refresh mode if no other resource is requiring a high quality power supply from 1V3. If t_{ACQ} is smaller than 10us and DC/DC is active,

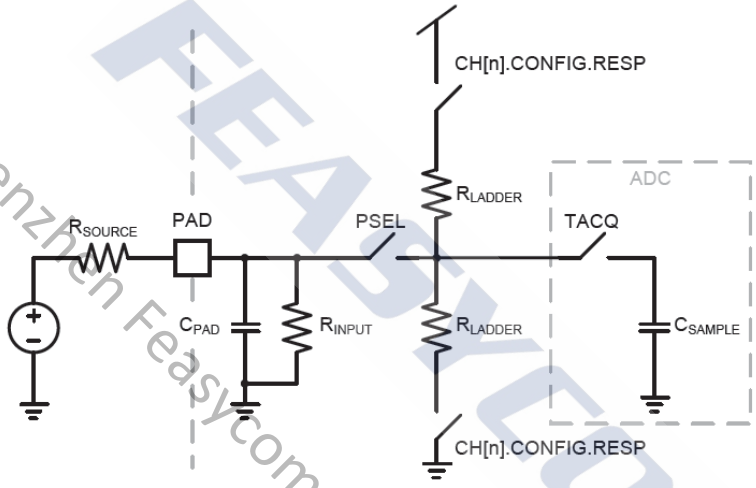


Figure 34: Model of SAADC input (one channel)

Note: SAADC average current calculation for a given application is based on the sample period, conversion and acquisition time (tconv and tACQ) and conversion and idle current (IADC,CONV and IADC,IDLE). For example,sampling at 4kHz gives a sample period of 250µs. The average current consumption would then be:

$$I_{AVERAGE} = \left(\frac{\left(t_{CONV} + t_{ACQ}\right)}{250}\right)\left(I_{ADC,CONV}\right) + \left(\frac{250 - \left(t_{CONV} + t_{ACQ}\right)}{250}\right)\left(I_{ADC,IDLE}\right)$$

Figure 35： Typical connection diagram using the ADC

5.5 SPI Electrical specification

5.5.1 SPI master interface

Table 9: SPI master interface electrical specifications

Parameter	Min	Typ	Max	Unit
f_{SPI} - Bit rates for SPI[a]	-	-	8[b]	Mbps
$I_{SPI,2Mbps}$ - Run current for SPI, 2 Mbps	-	-	50	µA
$I_{SPI,8Mbps}$ - Run current for SPI, 8 Mbps	-	-	50	µA
$I_{SPI,IDLE\ Idle}$ - current for SPI (STARTed, no CSN activity)	-	<1	-	µA
$t_{SPI,START,LP}$ - Time from writing TXD register to transmission started, low power mode	-	$t_{SPI,START,CL}$ + t_{START_HFINT}	-	µS
$t_{SPI,START,CL}$ - Time from writing TXD register to transmission started, constant latency mode	-	1	-	uS

a:Higher bit rates may require GPIOs to be set as High Drive, see GPIO chapter for more details.
b:The actual maximum data rate depends on the slave's CLK to MISO and MOSI setup and hold timings.

Table 10: Serial Peripheral Interface (SPI) Master timing specifications

Parameter	Min	Typ	Max	Unit
$t_{SPI,CSCK,8Mbps}$ - SCK period at 8Mbps	-	125	-	nS
$t_{SPI,CSCK,4Mbps}$ - SCK period at 4Mbps	-	250	-	nS
$t_{SPI,CSCK,2Mbps}$ - SCK period at 2Mbps	-	500	-	nS
$t_{SPI,RSCK,LD}$ - SCK rise time, low drive[a]	-	-	$t_{RF,25pF}$	
$t_{SPI,RSCK,HD}$ - SCK rise time, high drive[a]	-	-	$t_{HRF,25pF}$	
$t_{SPI,FSCK,LD}$ - SCK fall time, low drive[a]	-	-	$t_{RF,25pF}$	
$t_{SPI,FSCK,HD}$ - SCK fall time, high drive[a]	-	-	$t_{HRF,25pF}$	
tSPI,WHSCK - SCK high time[a]	(0.5*tCSCK) – tRSCK			
$t_{SPI,WLSCK}$ - SCK low time[a]	(0.5*tCSCK) – tFSCK			
$t_{SPI,SUMI}$ - MISO to CLK edge setup time	19			ns
$t_{SPI,HMI}$ - CLK edge to MISO hold time	18			ns
$t_{SPI,VMO}$ - CLK edge to MOSI valid			59	ns
$t_{SPI,HMO}$ - MOSI hold time after CLK edge	20			ns

a: At 25pF load, including GPIO capacitance, see GPIO spec.

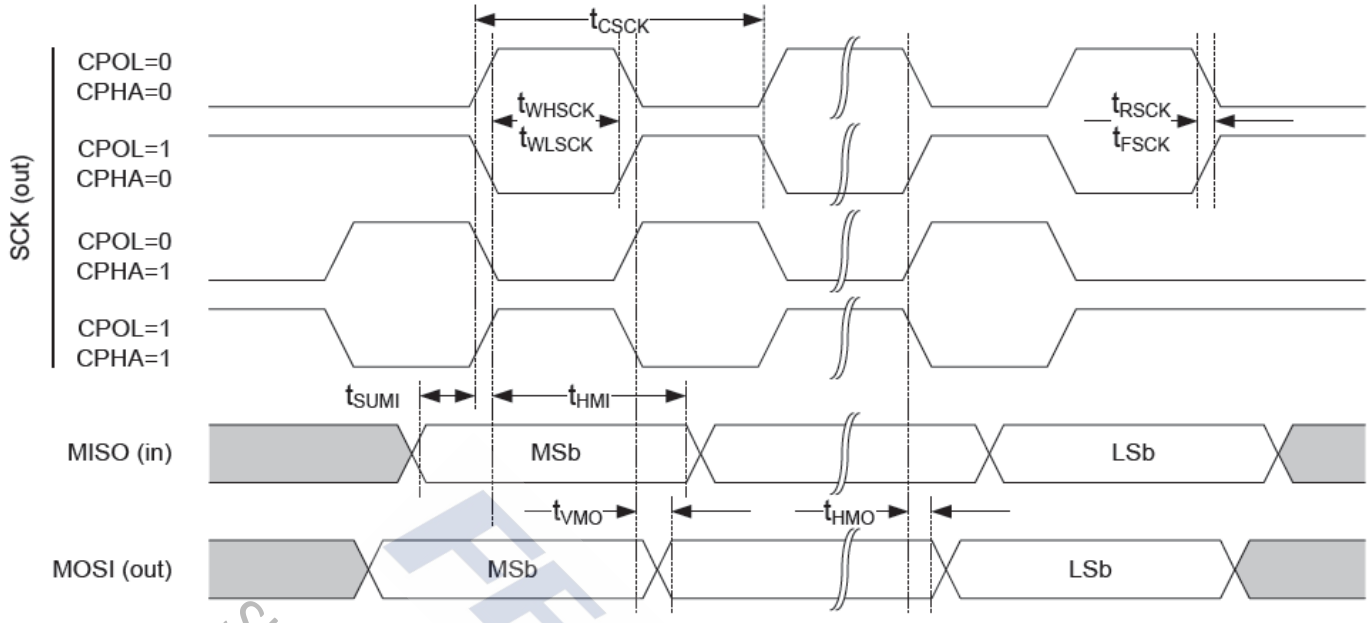


Figure 36: SPI master timing diagram

5.5.2 SPI slave interface electrical specifications

Table 11: SPI slave interface electrical specifications

Parameter	Min	Typ	Max	Unit
f_{SPI} - Bit rates for SPI[a]	-	-	8[b]	Mbps
$I_{SPI,2Mbps}$ - Run current for SPI, 2 Mbps	-	45	-	µA
$I_{SPI,8Mbps}$ - Run current for SPI, 8 Mbps	-	45	-	µA
$I_{SPI,IDLE\ Idle}$ - current for SPI (STARTed, no CSN activity)	-	1	-	µA
$t_{SPIS,LP,START}$ - Time from RELEASE task to ready to receive/transmit (CSN active), Low power mode	-	$t_{SPIS,CL,START}$ + t_{START_HFINT}	-	µS
$t_{SPIS,CL,START}$ - Time from RELEASE task to receive/transmit (CSN active), Constant latency mode	-	0.125	-	uS

a:Higher bit rates may require GPIOs to be set as High Drive, see GPIO chapter for more details.
b:The actual maximum data rate depends on the slave's CLK to MISO and MOSI setup and hold timings.

Table 12: Serial Peripheral Interface Slave (SPIS) timing specifications

Parameter	Min	Typ	Max	Unit
$t_{SPI,CSCK,8Mbps}$ - SCK period at 8Mbps	-	125	-	nS
$t_{SPI,CSCK,4Mbps}$ - SCK period at 4Mbps	-	250	-	nS
$t_{SPI,CSCK,2Mbps}$ - SCK period at 2Mbps	-	500	-	nS
$t_{SPIS,RFSCKIN}$ - SCK input rise/fall time			30	nS
$t_{SPIS,WHSCKIN}$ - SCK input high time		30		nS

$t_{SPIS,WLSCKIN}$ - SCK input low time	30		nS
$t_{SPIS,SUCSN,LP}$ - CSN to CLK setup time, Low power mode	tSPIS,SUCSN,CL + tSTART_HFINT		nS
$t_{SPIS,SUCSN,CL}$ - CSN to CLK setup time, Constant latency mode	1000		nS
$t_{SPIS,HCSN}$ - CLK to CSN hold time	2000		nS
$t_{SPIS,ASO}$ - CSN to MISO driven[a]		1000	nS
$t_{SPIS,DISSO}$ - CSN to MISO disabled[a]		68	nS
$t_{SPIS,CWH}$ - CSN inactive time	300		nS
$t_{SPIS,VSO}$ - CLK edge to MISO valid		19	nS
$t_{SPIS,HSO}$ - MISO hold time after CLK edge	18[b]		nS
$t_{SPIS,SUSI}$ - MOSI to CLK edge setup time	59		nS
$t_{SPIS,HSI}$ - CLK edge to MOSI hold time	20		nS

a: At 25pF load, including GPIO capacitance, see GPIO spec.

b: This is to ensure compatibility to SPI masters sampling MISO on the same edge as MOSI is output

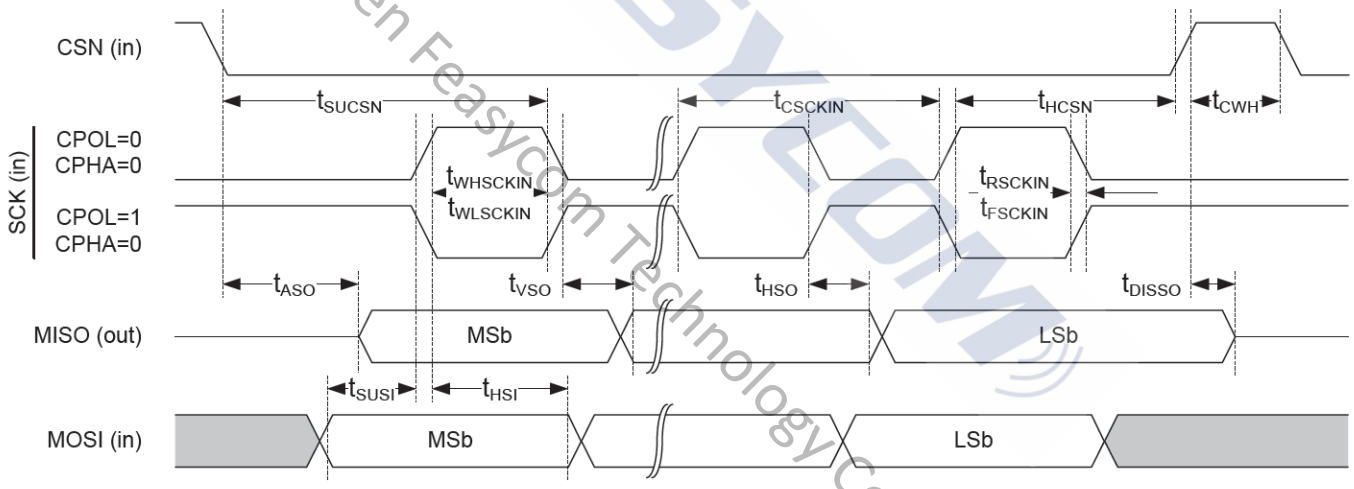


Figure 37: SPI timing diagram(Slave)

5.6 I2C Dynamic Characteristics

5.6.1 I2C Master interface electrical specifications

Table 13: I2C interface electrical specifications(Master)

Parameter	Min	Typ	Max	Unit
f_{I2C} - Bit rates for I2C[a]	100	-	400	Kbps
$I_{I2C,100kbps}$ - Run current for I2C, 100 kbps	-	50	-	μA
$I_{I2C,400kbps}$ - Run current for I2C, 400 kbps	-	50	-	μA
$t_{I2C,START,LP}$ - Time from STARTRX/STARTTX task to transmission started, Low power mode	-	$T_{I2C,START,CL}$ +	-	μS

		t_{START_HFINT}		
$t_{I2C,START,CL}$ - Time from STARTRX/STARTTX task to transmission started, Constant latency mode	-	1.5	-	µS

a: Higher bit rates or stronger pull-ups may require GPIOs to be set as High Drive, see GPIO chapter for more details.

Table 14: Two Wire Interface (I2C) timing specifications(Master)

Parameter	Min	Typ	Max	Unit
$f_{I2C,SCL,100kbps}$ - SCL clock frequency, 100 kbps	-	100		KHz
$f_{I2C,SCL,250kbps}$ - SCL clock frequency, 250 kbps	-	250	-	KHz
$f_{I2C,SCL,400kbps}$ - SCL clock frequency, 400 kbps	-	400	-	KHz
t_{I2C,SU_DAT} - Data setup time before positive edge on SCL – all modes	300	-	-	nS
t_{I2C,HD_DAT} - Data hold time after negative edge on SCL – all modes	500	-	-	nS
$t_{I2C,HD\_STA,100kbps}$ - I2C master hold time for START and repeated START condition, 100 kbps	10000	-	-	nS
$t_{I2C,HD\_STA,250kbps}$ - I2C master hold time for START and repeated START condition, 250kbps	4000	-	-	nS
$t_{I2C,HD\_STA,400kbps}$- I2C master hold time for START and repeated START condition,400 kbps	2500	-	-	nS
$t_{I2C,SU\_STO,100kbps}$ - I2C master setup time from SCL high to STOP condition, 100kbps	5000	-	-	nS
$t_{I2C,SU\_STO,250kbps}$ - I2C master setup time from SCL high to STOP condition, 250kbps	2000	-	-	nS
$t_{I2C,SU\_STO,400kbps}$ - I2C master setup time from SCL high to STOP condition, 400kbps	1250	-	-	nS
$t_{I2C,BUF,100kbps}$ - I2C master bus free time between STOP and START conditions,100 kbps	5800	-	-	nS
$t_{I2C,BUF,250kbps}$ - I2C master bus free time between STOP and START conditions,250 kbps	2700	-	-	nS
$t_{I2C,BUF,400kbps}$ - I2C master bus free time between STOP and START conditions,400 kbps	2100	-	-	nS

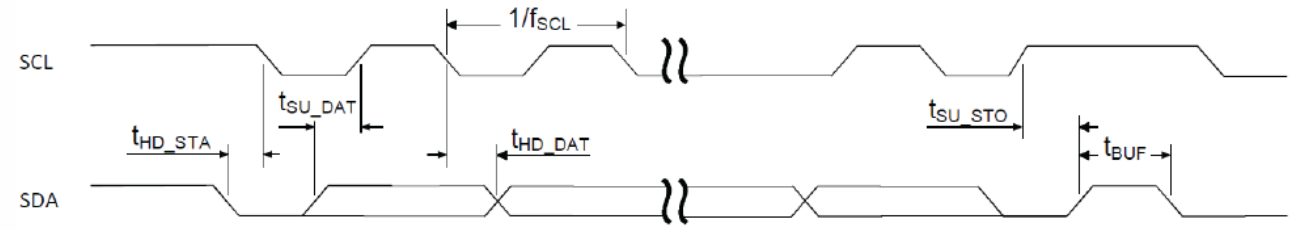


Figure 38: I2C timing diagram, 1 byte transaction

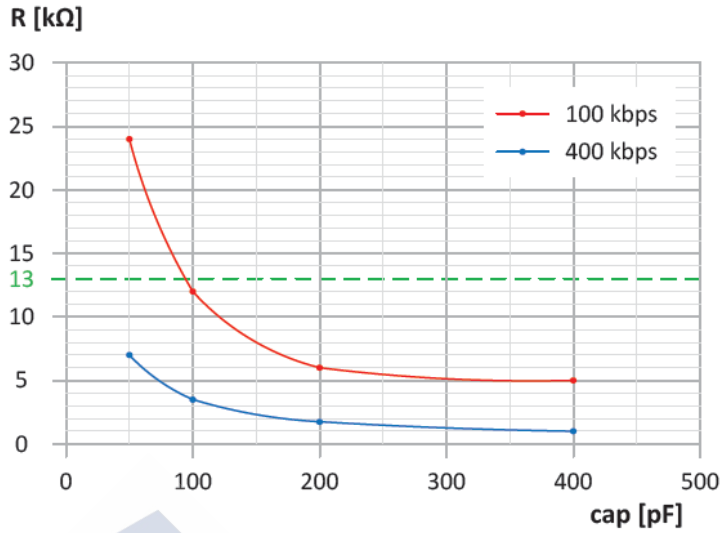


Figure 39: Recommended TWIM pullup value vs. line capacitance

- The I2C specification allows a line capacitance of 400 pF at most.
- FSC-BT630 internal pullup has a fixed value of typ. 13 kOhm, see RPU in the GPIO chapter.

5.6.2 I2C slave interface electrical specifications

Table 15: I2C interface electrical specifications(Slave)

Parameter	Min	Typ	Max	Unit
f_{I2C} - Bit rates for I2C[a]	100	-	400	Kbps
$I_{I2C,100kbps}$ - Run current for I2C, 100 kbps	-	45	-	µA
$I_{I2C,400kbps}$ - Run current for I2C, 400 kbps	-	45	-	µA
$I_{I2C,IDLE}$- Idle current for I2C	-	1	-	uA
$t_{I2C,START,LP}$ - Time from PREPARERX/PREPARETX task to transmission started, Low power mode	-	$T_{I2C,START,CL}$ + t_{START_HFINT}	-	µS
$t_{I2C,START,CL}$ - Time from PREPARERX/PREPARETX task to transmission started, Constant latency mode	-	1.5	-	µS

a: Higher bit rates or stronger pull-ups may require GPIOs to be set as High Drive, see GPIO chapter for more details.

Table 16: Two Wire Interface (I2C) timing specifications(Master)

Parameter	Min	Typ	Max	Unit
$f_{I2C,SCL,400kbps}$ - SCL clock frequency, 400 kbps	-	400	-	KHz
t_{I2C,SU_DAT} - Data setup time before positive edge on SCL – all modes	300	-	-	nS
t_{I2C,HD_DAT} - Data hold time after negative edge on SCL – all modes	500	-	-	nS
$t_{I2C,HD\_STA,100kbps}$ - I2C slave hold time from for START condition (SDA low to SCL	5200	-	-	nS

low), 100 kbps				
$t_{I2C,HD\_STA,400kbps}$- I2C slave hold time from for START condition (SDA low to SCL low), 400 kbps	1300	-	-	nS
$t_{I2C,SU\_STO,100kbps}$ - I2C slave setup time from SCL high to STOP condition, 100 kbps	5200	-	-	nS
$t_{I2C,SU\_STO,400kbps}$ - I2C slave setup time from SCL high to STOP condition, 400 kbps	1300	-	-	nS
$t_{I2C,BUF,100kbps}$ - I2C slave bus free time between STOP and START conditions, 100 kbps	-	4700	-	nS
$t_{I2C,BUF,400kbps}$ - I2C slave bus free time between STOP and START conditions, 400 kbps	-	1300	-	nS

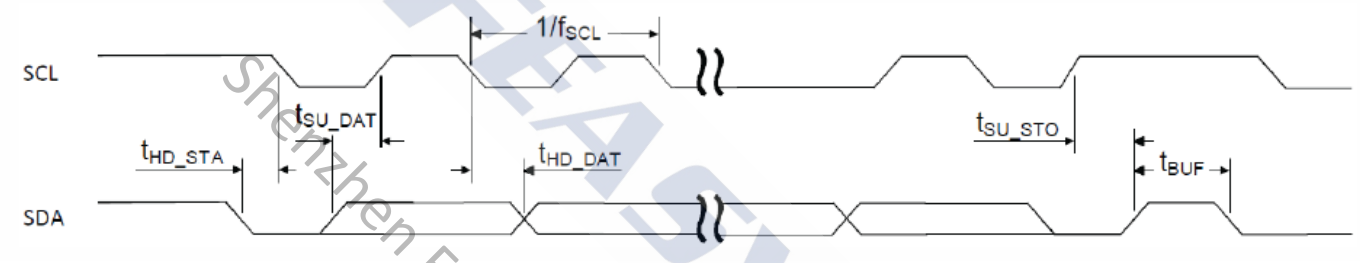


Figure 40: I2C timing diagram, 1 byte transaction

5.7 I2S Electrical specification

Table 17: I2S Dynamic Characteristics

Parameter	Min	Typ	Max	Unit
t_{S_SDIN} - SDIN setup time before SCK rising	20	-	400	nS
t_{H_SDIN} - SDIN hold time after SCK rising	15	50	-	nS
t_{S_SDOUT} - SDOUT setup time after SCK falling	40	50	-	nS
t_{H_SDOUT} - SDOUT hold time before SCK falling	6	-	-	nS
t_{SCK_LRCK} - SCLK falling to LRCK edge	-5	0	5	nS
f_{MCK} - MCK frequency	-	-	4000	KHz
f_{LRCK} - LRCK frequency	-	-	48	KHz
f_{SCK} - SCK frequency	-	-	2000	KHz
DC_{CK} - Clock duty cycle (MCK, LRCK, SCK)	45	-	55	%

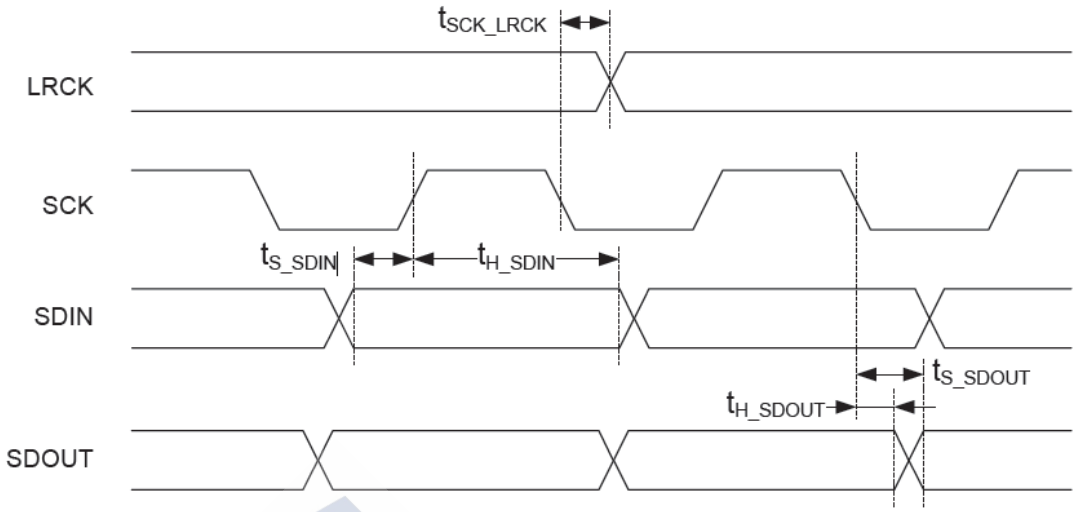


Figure 41: I2S timing diagram

5.8 PWM Characteristics

Table 18: PWM Electrical Specification

Parameter	Min	Typ	Max	Unit
$I_{PWM,16MHz}$ - PWM run current, Prescaler set to DIV_1 (16 MHz), excluding DMA and GPIO	-	200	-	uA
$I_{PWM,8MHz}$- PWM run current, Prescaler set to DIV_2 (8 MHz), excluding DMA and GPIO	-	150	-	uA
$I_{PWM,125kHz}$ - PWM run current, Prescaler set to DIV_128 (125 kHz), excluding DMA and GPIO	-	150	-	uA

5.9 PDM Characteristics

Table 19: PDM Electrical Specification

Parameter	Min	Typ	Max	Unit
$I_{PDM,stereo}$ - PDM module active current, stereo operation[a]	-	1.4	-	mA
$f_{PDM,CLK}$ - PDM clock speed	-	1.032	-	MHz
$t_{PDM,JITTER}$ - Jitter in PDM clock output	-	-	20	nS
$T_{dPDM,CLK}$ - PDM clock duty cycle	40	50	60	%
$t_{PDM,DATA}$ - Decimation filter delay	-	-	5	ms
$t_{PDM,cv}$ - Allowed clock edge to data valid	-	-	125	nS
$t_{PDM,ci}$ - Allowed (other) clock edge to data invalid	0	-	-	nS
$t_{PDM,s}$ - Data setup time at $f_{PDM,CLK}$=1.024 MHz	65	-	-	nS
$t_{PDM,h}$ - Data hold time at $f_{PDM,CLK}$=1.024 MHz	0	-	-	nS
$G_{PDM,default}$ - Default (reset) absolute gain of the PDM module	-	3.2	-	dB

a: Average current including PDM and DMA transfers, excluding clock and power supply base currents

5.10 UART Electrical Specification

Table 20: UART Electrical Specification

Parameter	Min	Typ	Max	Unit
f_{UART} - Baud rate for UART[a]	-	-	1000	Kbps
I_{UART1M} - Run current at max baud rate.	-	55	-	uA
$I_{UART115k}$ - Run current at 115200 bps.	-	55	-	uA
$I_{UART1k2}$- Run current at 1200 bps.	-	55	-	uA
$I_{UART,IDLE}$ - Idle current for UART	-	1	-	uA
$t_{UART,CTSH}$ - CTS high time	1	-	-	uS
$t_{UART,START,LP}$ - Time from STARTRX/STARTTX task to transmission started, low power mode	-	$t_{UART,START}$ + t_{START_HFINT}	-	uS
$t_{UART,START,CL}$ - Time from STARTRX/STARTTX task to transmission started, constant latency mode	-	1	-	uS

a: Higher baud rates may require GPIOs to be set as High Drive, see GPIO chapter for more details.

5.11 NFC Electrical Specification

Table 21: NFC Electrical Specification

Parameter	Min	Typ	Max	Unit
f_c - Frequency of operation	-	13.56	-	MHz
C_{MI} - Carrier modulation index	95	-	-	%
DR - Data Rate	-	106	-	kbps
f_s - Modulation sub-carrier frequency	-	fc/16	-	MHz
V_{swing} Peak differential Input voltage swing on NFC1 and NFC2	-	-	VDD	Vp
V_{sense} - Peak differential Field detect threshold level on NFC1-NFC2[a]	-	1.0	-	Vp
I_{sense} - Current in SENSE STATE	-	100	-	nA
$I_{activated}$ - Current in ACTIVATED STATE	-	480	-	uA
R_{in_min} - Minimum input resistance when regulating voltage swing	-	-	40	Ω
R_{in_max} - Maximum input resistance when regulating voltage swing	1.0	-	-	kΩ
$R_{in\_loadmod}$ - Input resistance when load modulating	8	-	22	Ω
I_{max} - Maximum input current on NFC pins	-	-	80	mA

a: Input is high impedance in sense mode

Table 22: NFCT Timing Parameters

Parameter	Min	Typ	Max	Unit
$t_{activate}$ - Time from task_ACTIVATE in SENSE or DISABLE state to ACTIVATE_A or IDLE stateb	-	-	500	uS
t_{sense} - Time from remote field is present in SENSE mode to FIELDDETECTED event is asserted	-	-	20	uS

b: Does not account for voltage supply and oscillator startup times

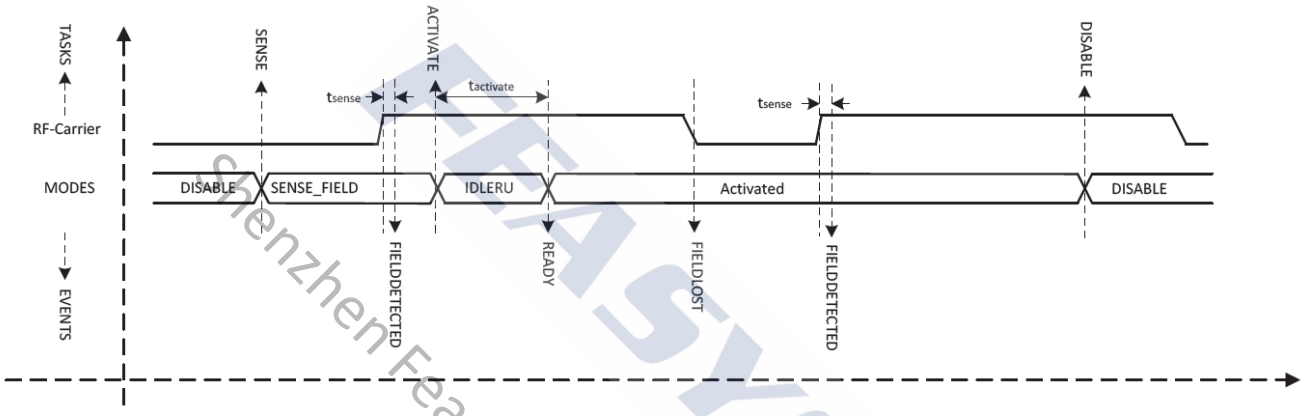


Figure 42: NFCT timing parameters (Shortcuts for FIELDDETECTED and FIELDLOST are disabled)

5.12 Power consumptions

Table 23: Power consumptions **(TBD)**

Parameter	Test Conditions	Type	Unit
TX & RX	peak current in TX (0 dBm)	~5.3	mA
	peak current in TX (4 dBm)	~6.6	
	paeak current in RX	~5.4	
NFC antenna pin current	INFC1/2	80	mA
Current consumption, sleep			
I_{OFF} - System OFF current, no RAM retention		0.3	uA
I_{ON} - System ON base current, no RAM retention		1.2	uA
I_{RAM} - Additional RAM retention current per 4 KB RAM section		20	nA
Power fail comparator			
I_{POF} - Current consumption when enabled		<4	uA

6. MSL & ESD

Table 24: MSL and ESD

Parameter	Value
MSL (moisture sensitivity level)	MSL 1
ESD grade:	ESD HBM (human body model): 2KV ESD HBM (human body model): 500V

7. RECOMMENDED TEMPERATURE REFLOW PROFILE

Prior to any reflow, it is important to ensure the modules were packaged to prevent moisture absorption. New packages contain desiccate (to absorb moisture) and a humidity indicator card to display the level maintained during storage and shipment. If directed to bake units on the card, please check the below **Table 25** and follow instructions specified by IPC/JEDEC J-STD-033.

Note: The shipping tray cannot be heated above 65°C. If baking is required at the higher temperatures displayed in the below **Table 25**, the modules must be removed from the shipping tray.

Any modules not manufactured before exceeding their floor life should be re-packaged with fresh desiccate and a new humidity indicator card. Floor life for MSL (Moisture Sensitivity Level) 3 devices is 168 hours in ambient environment 30°C/60%RH.

Table 25: Recommended baking times and temperatures

MSL	125°C Baking Temp.		90°C/≤ 5%RH Baking Temp.		40°C/ ≤ 5%RH Baking Temp.	
	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%
3	9 hours	7 hours	33 hours	23 hours	13 days	9 days

Feasycom surface mount modules are designed to be easily manufactured, including reflow soldering to a PCB. Ultimately it is the responsibility of the customer to choose the appropriate solder paste and to ensure oven temperatures during reflow meet the requirements of the solder paste. Feasycom surface mount modules conform to J-STD-020D1 standards for reflow temperatures.

The soldering profile depends on various parameters necessitating a set up for each application. The data here is given only for guidance on solder reflow.

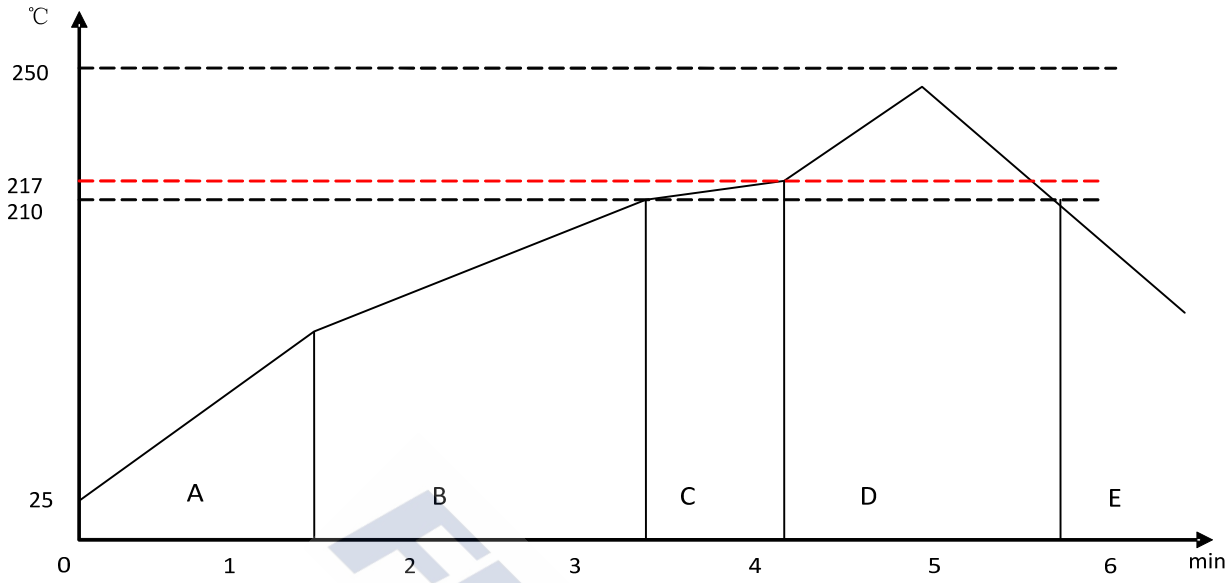


Figure 43: Typical Lead-free Re-flow

Pre-heat zone (A) — This zone raises the temperature at a controlled rate, **typically 0.5 – 2 °C/s**. The purpose of this zone is to preheat the PCB board and components to 120 ~ 150 °C. This stage is required to distribute the heat uniformly to the PCB board and completely remove solvent to reduce the heat shock to components.

Equilibrium Zone 1 (B) — In this stage the flux becomes soft and uniformly encapsulates solder particles and spread over PCB board, preventing them from being re-oxidized. Also with elevation of temperature and liquefaction of flux, each activator and rosin get activated and start eliminating oxide film formed on the surface of each solder particle and PCB board. **The temperature is recommended to be 150° to 210° for 60 to 120 second for this zone.**

Equilibrium Zone 2 (C) (optional) — In order to resolve the upright component issue, it is recommended to keep the temperature in 210 – 217 ° for about 20 to 30 second.

Reflow Zone (D) — The profile in the figure is designed for Sn/Ag3.0/Cu0.5. It can be a reference for other lead-free solder. The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint. The recommended peak temperature (Tp) is 230 ~ 250 °C. The soldering time should be 30 to 90 second when the temperature is above 217 °C.

Cooling Zone (E) — The cooling ate should be fast, to keep the solder grains small which will give a longer-lasting joint. **Typical cooling rate should be 4 °C.**

8. MECHANICAL DETAILS

8.1 Mechanical Details

- Dimension: 10mm(W) x 11.9mm(L) x 1.7mm(H) Tolerance: ±0.1mm
- Module size: 10mm X 11.9mm Tolerance: ±0.1mm
- Pad size: 0.9mmX0.6mm Tolerance: ±0.1mm
- Pad pitch: 1.1mm Tolerance: ±0.1mm

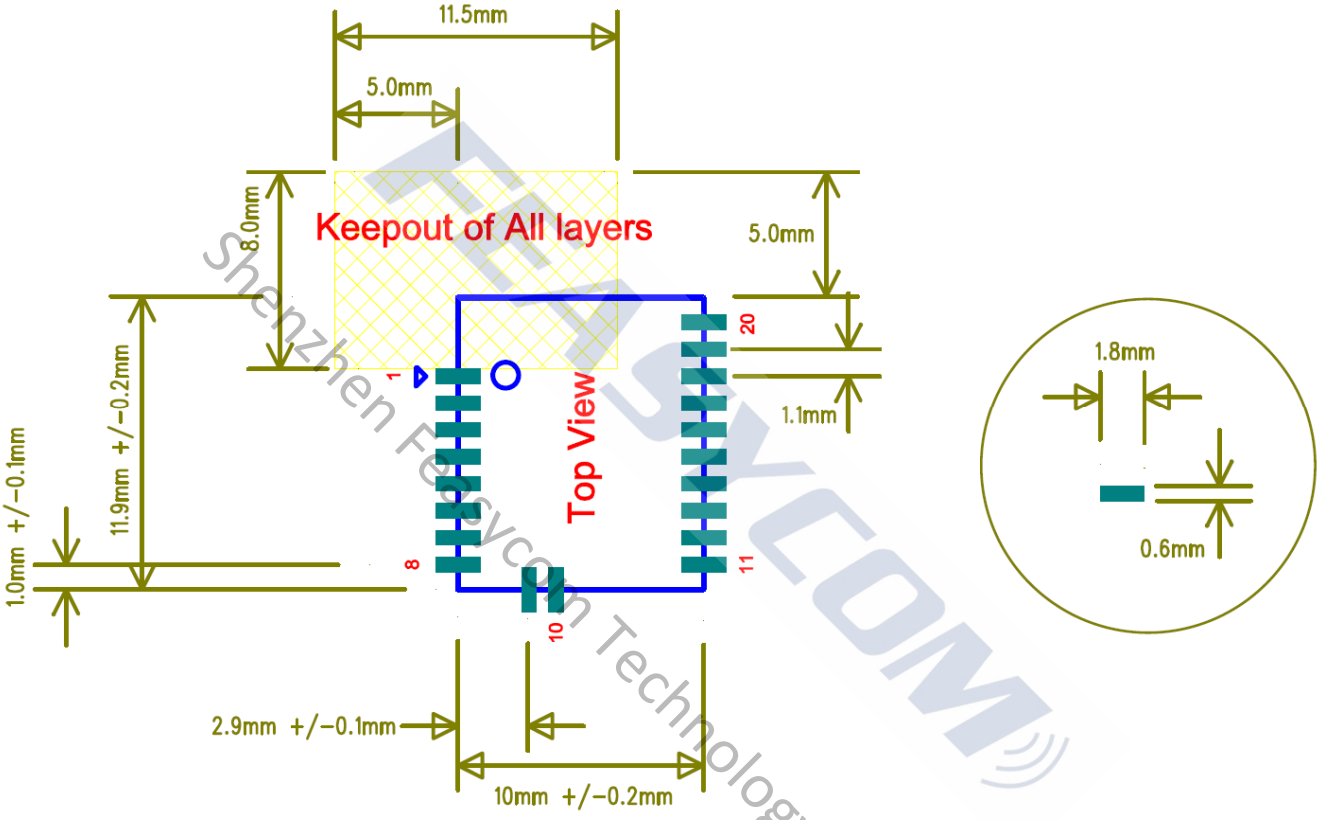


Figure 44: FSC-BT630 footprint

9. HARDWARE INTEGRATION SUGGESTIONS

9.1 Soldering Recommendations

FSC-BT630 is compatible with industrial standard reflow profile for Pb-free solders. The reflow profile used is dependent on the thermal mass of the entire populated PCB, heat transfer efficiency of the oven and particular type of solder paste used. Consult the datasheet of particular solder paste for profile configurations.

Feasycom will give following recommendations for soldering the module to ensure reliable solder joint and operation of the module after soldering. Since the profile used is process and layout dependent, the optimum profile should be studied case by case. Thus following recommendation should be taken as a starting point guide.

9.2 Layout Guidelines(Internal Antenna)

It is strongly recommended to use good layout practices to ensure proper operation of the module. Placing copper or any metal near antenna deteriorates its operation by having effect on the matching properties. Metal shield around the antenna will prevent the radiation and thus metal case should not be used with the module. Use grounding vias separated max 3 mm apart at the edge of grounding areas to prevent RF penetrating inside the PCB and causing an unintentional resonator. Use GND vias all around the PCB edges.

The mother board should have no bare conductors or vias in this restricted area, because it is not covered by stop mask print. Also no copper (planes, traces or vias) are allowed in this area, because of mismatching the on-board antenna.

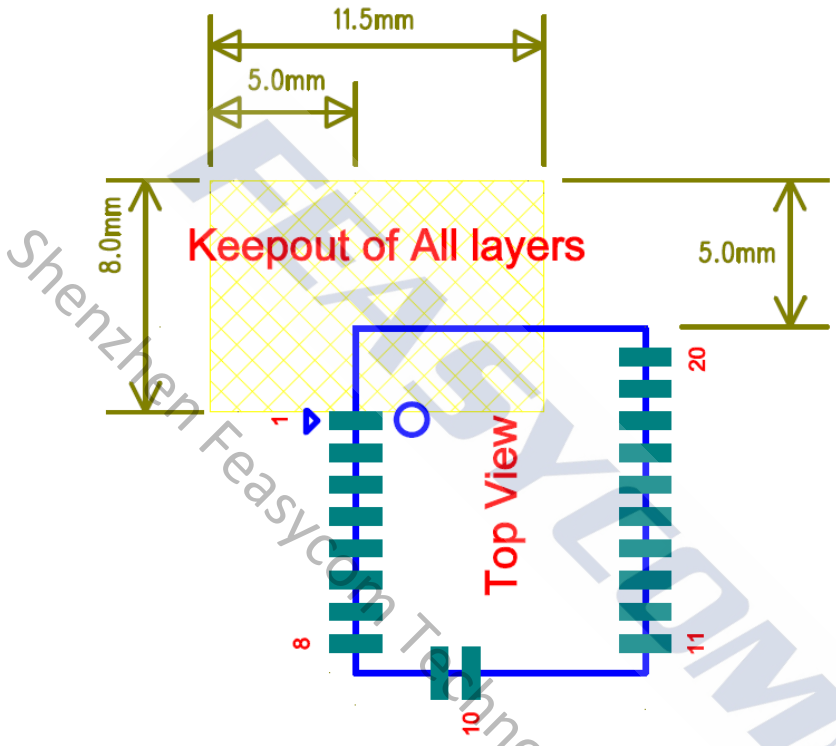


Figure 45: FSC-BT630 Restricted Area (keepout of all layers)

Following recommendations helps to avoid EMC problems arising in the design. Note that each design is unique and the following list do not consider all basic design rules such as avoiding capacitive coupling between signal lines. Following list is aimed to avoid EMC problems caused by RF part of the module. Use good consideration to avoid problems arising from digital signals in the design.

Ensure that signal lines have return paths as short as possible. For example if a signal goes to an inner layer through a via, always use ground vias around it. Locate them tightly and symmetrically around the signal vias. Routing of any sensitive signals should be done in the inner layers of the PCB. Sensitive traces should have a ground area above and under the line. If this is not possible, make sure that the return path is short by other means (for example using a ground line next to the signal line).

9.3 Layout Guidelines(External Antenna)

Placement and PCB layout are critical to optimize the performances of a module without on-board antenna designs. The trace from the antenna port of the module to an external antenna should be 50Ω and must be as short as possible to avoid any interference into the transceiver of the module. The location of the external antenna and RF-IN port of the module should be kept away from any noise sources and digital traces. A matching network might be needed in between the external antenna and RF-IN port to better match the impedance to minimize the return loss.

As indicated in **Figure 46** below, RF critical circuits of the module should be clearly separated from any digital circuits on the system board. All RF circuits in the module are close to the antenna port. The module, then, should be placed in this way that module digital part towards your digital section of the system PCB.

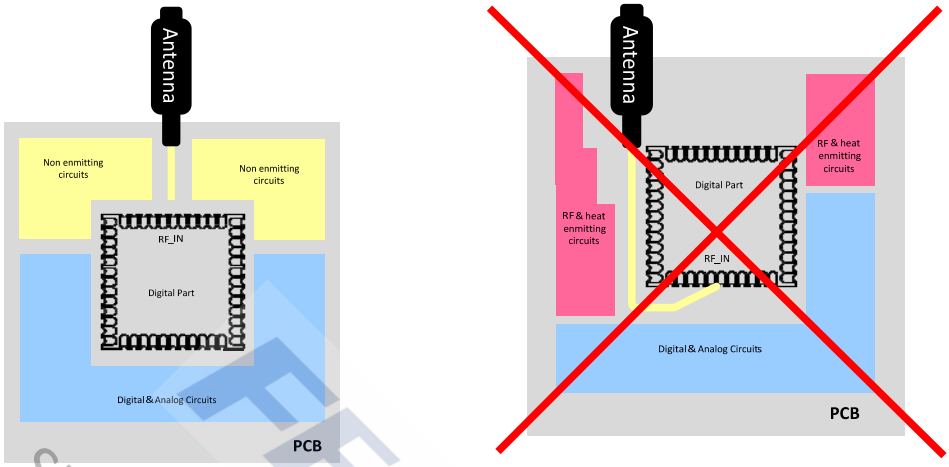


Figure 46: Placement the Module on a System Board

9.3.1 Antenna Connection and Grounding Plane Design

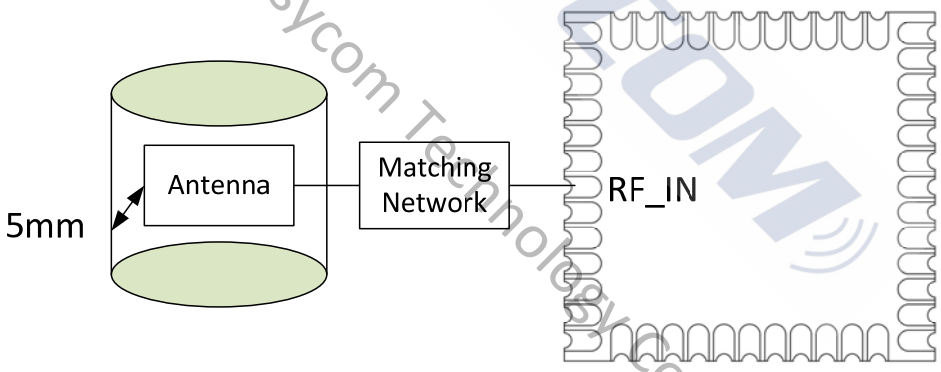


Figure 47: Leave 5mm Clearance Space from the Antenna

General design recommendations are:

- The length of the trace or connection line should be kept as short as possible.
- Distance between connection and ground area on the top layer should at least be as large as the dielectric thickness.
- Routing the RF close to digital sections of the system board should be avoided.
- To reduce signal reflections, sharp angles in the routing of the micro strip line should be avoided. Chamfers or fillets are preferred for rectangular routing; 45-degree routing is preferred over Manhattan style 90-degree routing.

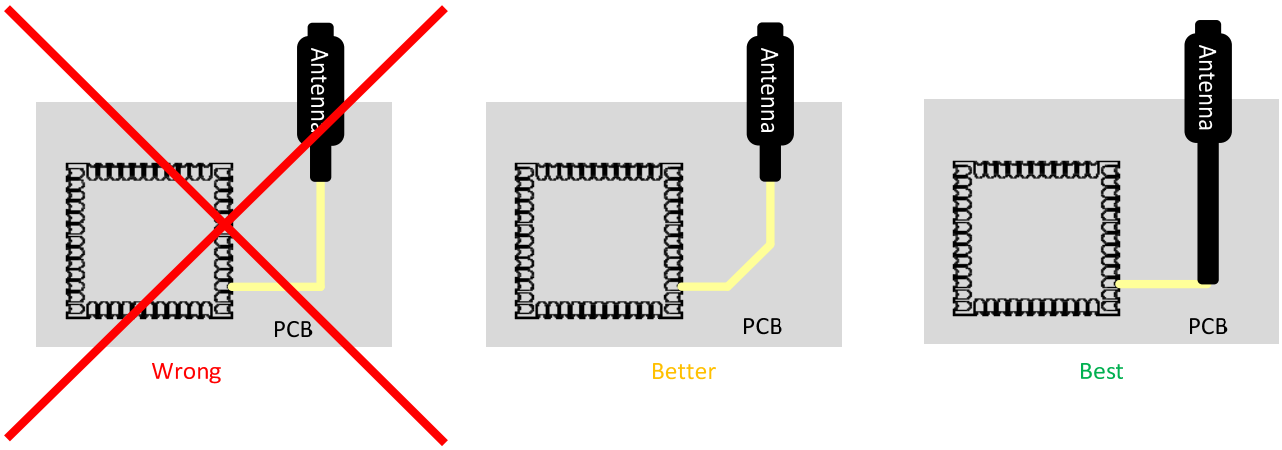


Figure 48: Recommended Trace Connects Antenna and the Module

- Routing of the RF-connection underneath the module should be avoided. The distance of the micro strip line to the ground plane on the bottom side of the receiver is very small and has huge tolerances. Therefore, the impedance of this part of the trace cannot be controlled.
- Use as many vias as possible to connect the ground planes.

10. PRODUCT PACKAGING INFORMATION

10.1 Default Packing

a, Tray vacuum

b, Tray Dimension: 180mm * 195mm

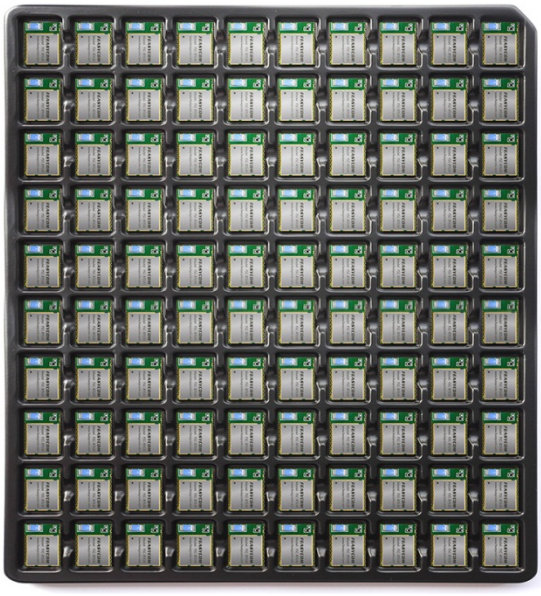


Figure 49: Tray vacuum (Image for reference only, subject to actual product)

11. APPLICATION SCHEMATIC