DLC Display Co., Limited

德爾西顯示器有限公司

MODEL No: DLC0150CNOG-W

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Record of Revision

Date	Revision No.	Summary
2013-10-21	1.0	Rev 1.0 was issued
2020-03-09	1.1	Modify Chromaticity page 13

1. Scope

This data sheet is to introduce the specification of DLC0150CNOG-W, passive matrix OLED module. It is composed of an OLED panel, driver ICs and FPC. The1.50″ display area contains 128 x 128 pixels.

2. Application

Digital equipments which need display, instrumentation, remote control, electronic product.
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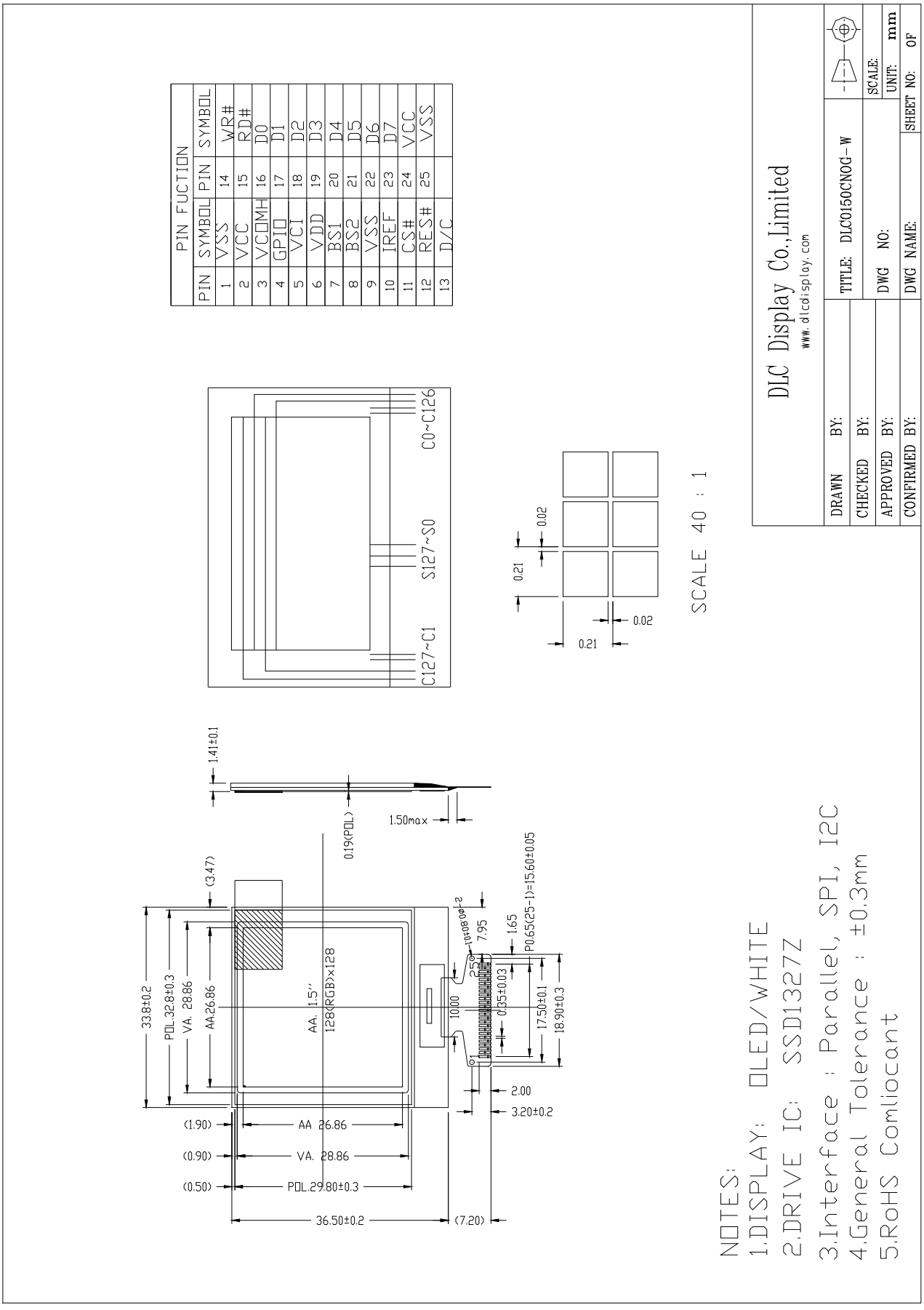
3. General Information

Item	Contents	Unit
Size	1.50	inch
Resolution	128(RGB)×128	/
Display Color	White	
Interface	8-bit 8080,8-bit 6800,SPI,I²C	
Dot Size	0.19 (W) x 0.19 (H)	mm
Pixel pitch	0.21 (W) x 0.21 (H)	mm
Outline Dimension	33.8 (W) x 36.5 (H) x 1.41 (T)	mm
Active Area	26.86(W)x26.86(H)	mm
Driver IC	SSD1327	
Drive Duty	1/128 Duty	/
Operating Temperature	-40℃~+70℃	
Storage Temperature	-40℃~＋85℃	

4. Outline Drawing



5. Interface signals

PIN NO.	PIN NAME	DESCRIPTION
1	VSS	Ground
2	VCC	Power supply for analog circuit.
3	VCOMH	Com Voltage Output. A capacitor should be connected between this pin and VSS.
4	GPIO	General I/O port.
5	VCI	Power supply for logic circuit.
6	VDD	A capacitor should be connected between this pin and VSS.
7	BS1	MCU bus interface selection pins.
8	BS2	
9	VSS	Ground pin. It must be connected to external ground.
10	IREF	Reference current input pin. A resistor should be connected between this pin and VSS.
11	CS#	Chip select input.
12	RES#	Reset signal input. When it's low, initialization of SSD1327 is executed.
13	D/C#	Data / Command control. Pull high for write/read display data. Pull low for write command or read status.
14	W/R#	MCU interface input. Data write operation is initiated when it's pull low.
15	RD#	MCU interface input. Data read operation is initiated when it's pull low.
16~23	D0-D7	Data bus(for parallel interface)
24	VCC	Power supply for analog circuit.
25	VSS	Ground

6. Environment Conditions

6.1 Electrical Absolute max. ratings

Parameter	Symbol	MIN	MAX	Unit	Remark
Supply voltage	VCC	8	19	V	IC maximum rating
	VCI	-0.3	4.0	V	IC maximum rating

Note (1): All of the voltages are on the basis of "VSS = 0V".

6.2 Environment Conditions

Item	Symbol	MIN	MAX	Unit	Remark
Operating Temperature	TOPR	-40	70	℃	
Storage Temperature	TSTG	-40	85	℃	

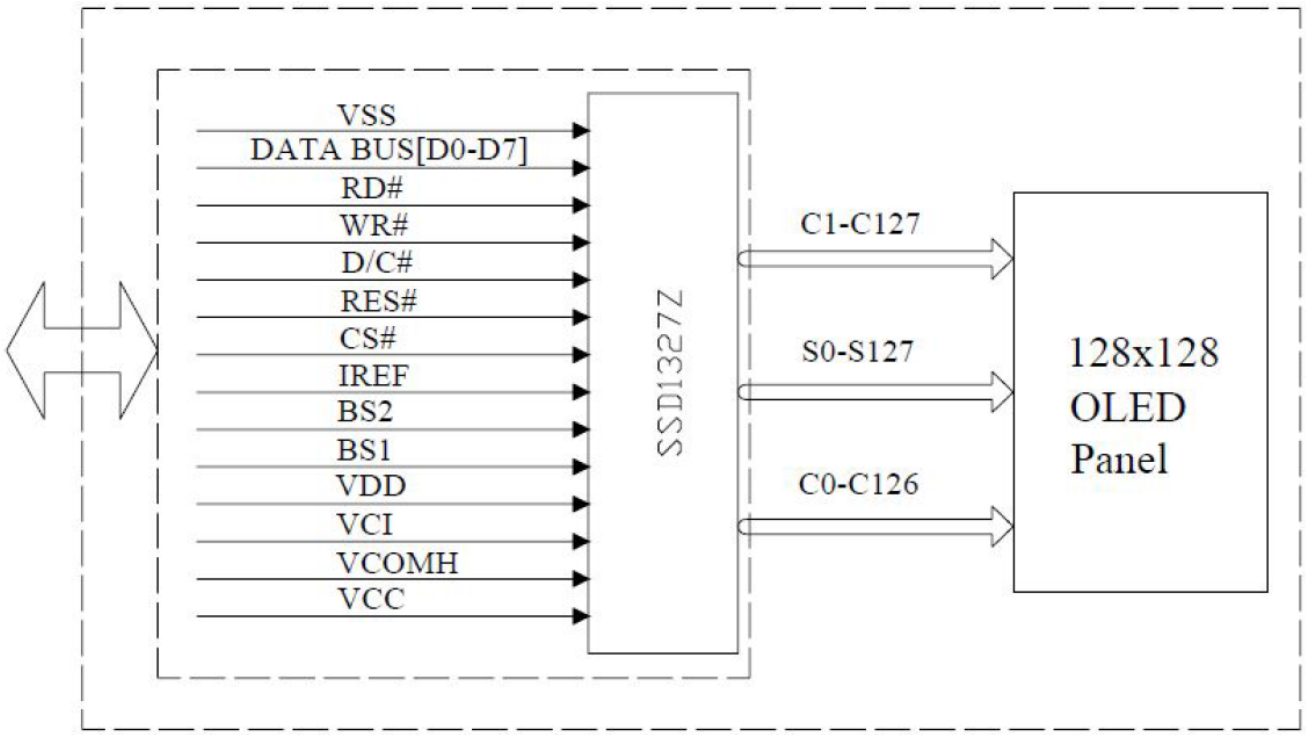
7. Electrical Specifications

7.1 Electrical characteristics

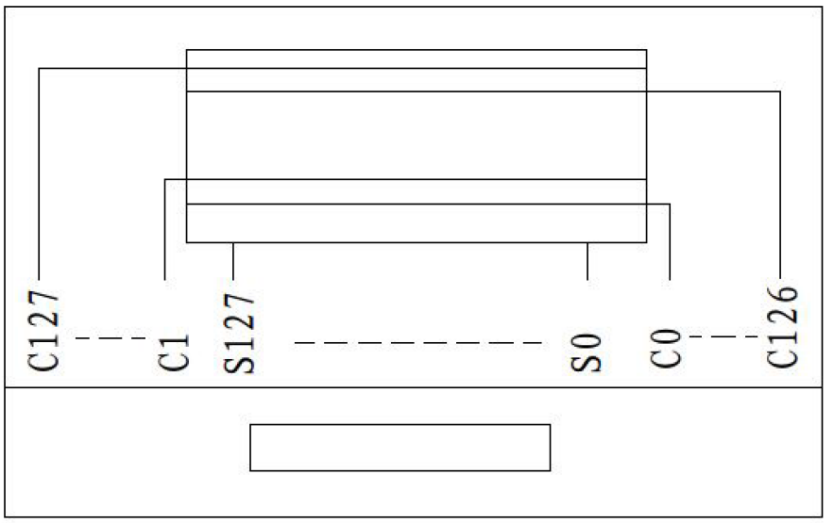
Item	Symbol	MIN	TYP	MAX	Unit	Remark
OLED Driver Supply Voltage	VCC	14.5	15	15.5	V	
MCU interface logic level & Low voltage power supply	VCI	2.6	--	3.5	V	
High-level Input Voltage	VIH	0.8×VCI	-	VCI	V	
Low-level Input Voltage	VIL	0	-	0.2×VCI	V	
High-level Output Voltage	VOH	0.9×VCI	-	VCI	V	
Low-level Output Voltage	VOL	0	-	0.1×VCI	V	

7.2 Function Block Diagram

7.1 Function Block Diagram



7.2 Panel Layout Diagram



COM&SEG LAYOUT

8. Command/AC Timing

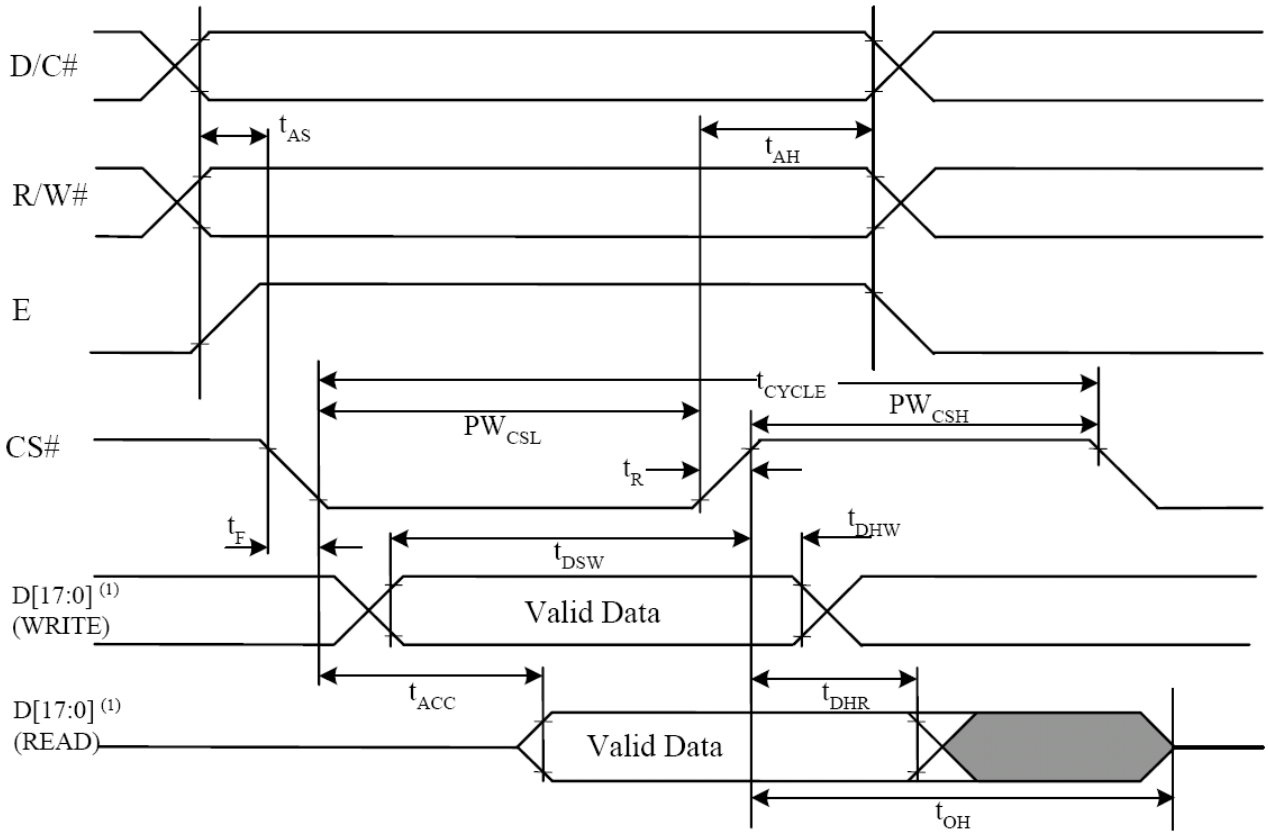
8.1 AC Electrical Characteristics

8.1.1 6800-Series MPU Parallel Interface Timing Characteristics

(VCI-VSS =1.65V to 3.5V, TA = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{CYCLE}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Table: 6800-series MCU parallel interface characteristics

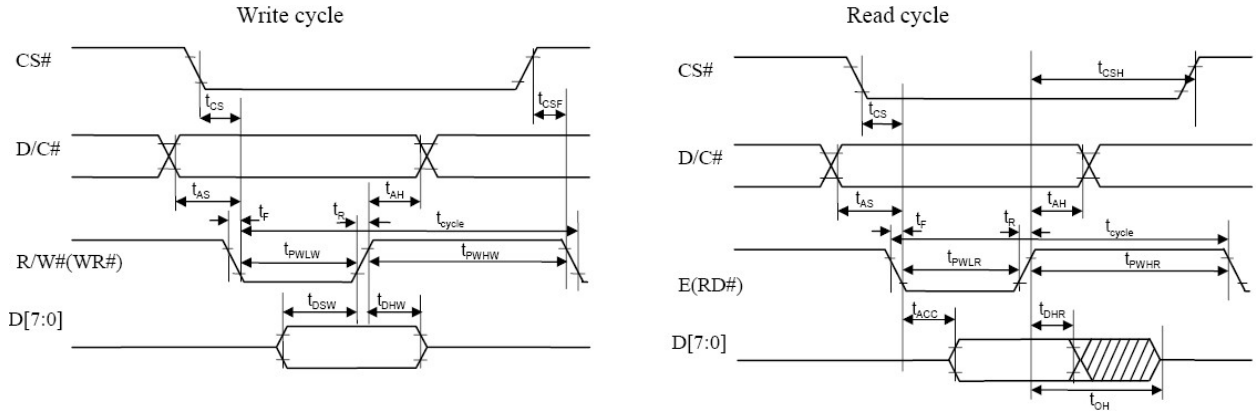


8.1.2 8080-Series MPU Parallel Interface Timing Characteristics

(VCI-VSS =1.65V to 3.5V, TA = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{CYCLE}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
t_{PWLR}	Read Low Time	150	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHR}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns

Table: 8800-series MCU parallel interface characteristics

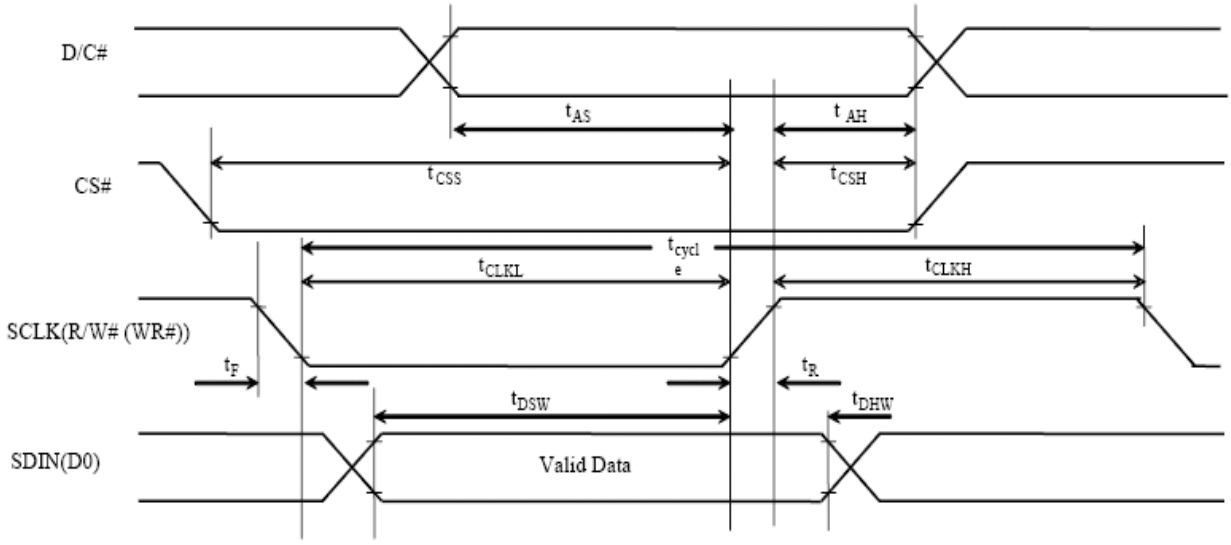


8.1.3 Serial Interface Timing Characteristics(4-wire SPI)

(VCI-VSS =1.65V to 3.5V, TA = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	50	-	-	ns
t_{AS}	Address Setup Time	15	-	-	ns
t_{AH}	Address Hold Time	15	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	20	-	-	ns
t_{CLKH}	Clock High Time	20	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Table: Serial interface characteristics(4-wire SPI)

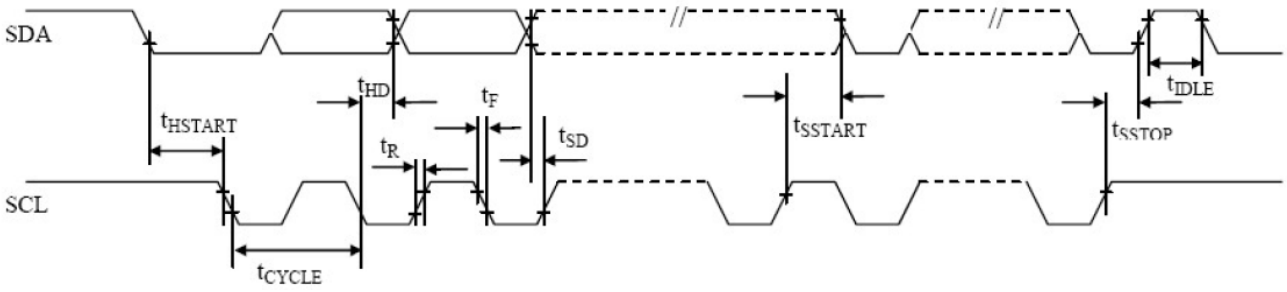


8.1.4 I²C Interface Timing Characteristics

(VCI-VSS =1.65V to 3.5V, TA = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	-	us
t_{HSTART}	Start condition Hold Time	0.6	-	-	us
t_{HD}	Data Hold Time (for "SDA_{OUT}" pin)	0	-	-	ns
	Data Hold Time (for "SDA_{IN}" pin)	300	-	-	ns
t_{SD}	Data Setup Time	100	-	-	ns
t_{SSTART}	Start condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	-	us
t_{SSTOP}	Stop condition Setup Time	0.6	-	-	us
t_R	Rise Time for data and clock pin	-	-	300	ns
t_F	Fall Time for data and clock pin	-	-	300	ns
t_{IDLE}	Idle Time before a new transmission can start	1.3	-	-	us

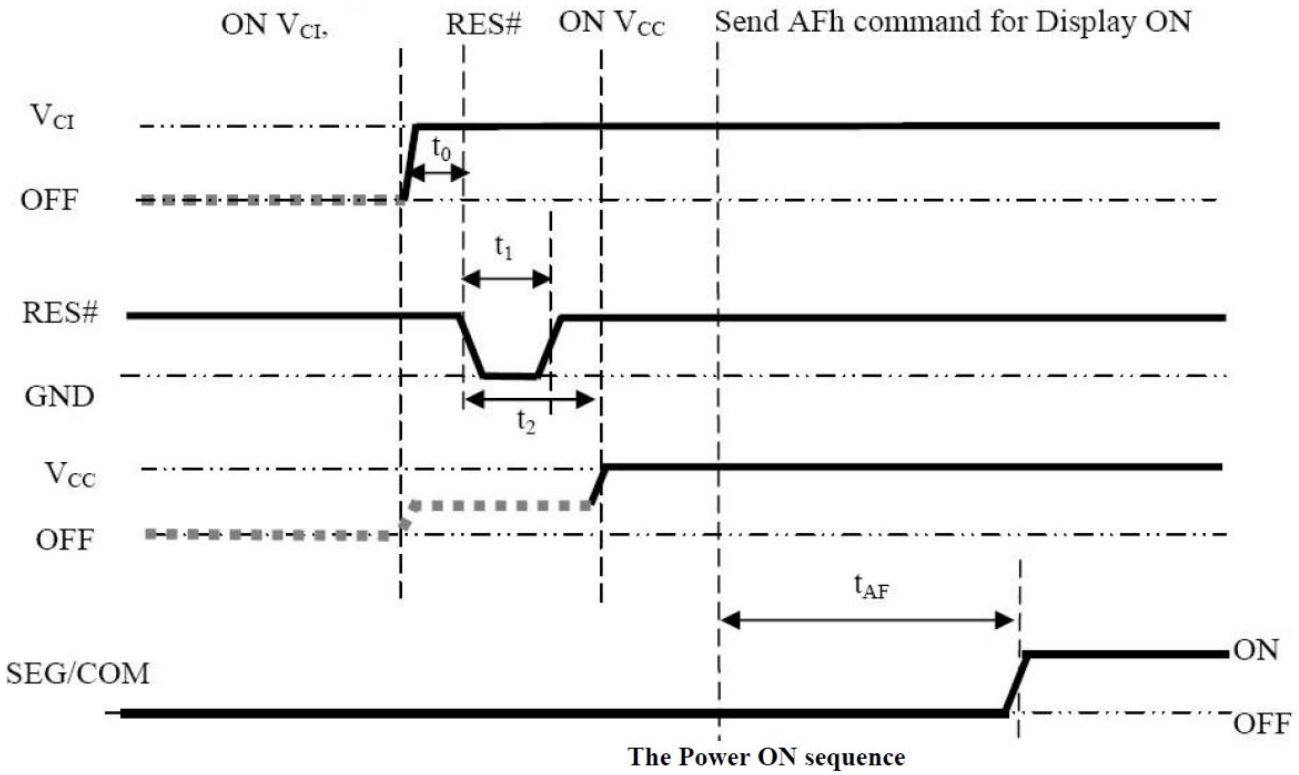
Table: I²C Interface Timing characteristics



8.2 Functional Specification and Application Circuit

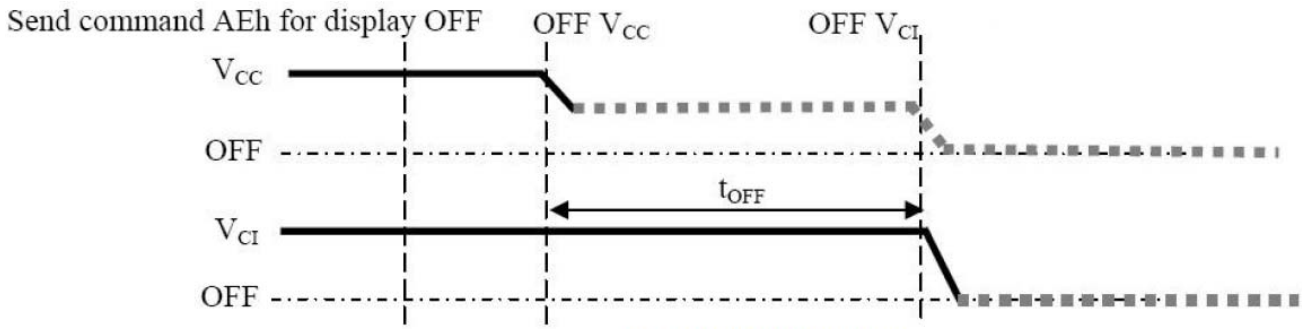
8.2.1 Power ON and Power OFF Sequence

1. Power ON VCI.
2. After VCI becomes stable, set wait time at least 1ms(t0)for internal VDD become stable. Then set RES# pin LOW(logic low),for at least 100us(t1)(4)and then HIGH(logic high).
3. After set RES# pin LOW(logic low),wait for least 100us(t2).Then Power ON VCC.(1)
4. After VCC become stable, send command AFh for display ON.SEG/COM will be ON after200ms(tAF).



The Power ON sequence

1. Send command Aeh for display OFF.
2. Power OFF VCC.(1),(2),(3)
3. Wait fo Toff. Power OFF VCI(where Minimum Toff=0ms(5),Typical tOFF=100ms)



The Power OFF sequence

Notes:

(1) Since an ESD protection circuit is connected between VCI and VCC, VCC becomes lower than VCI whenever VCI is ON and VCC is OFF as shown in the dotted line of VCC in above figures.

(2) VCC should be kept float (disabled) when it is OFF.

(3) Power pins(VCI, VCC)can never be pulled to ground under any circumstance.

(4) The register values are reset after t1.

(5) VCI should not be Power OFF before VCC Power OFF.

8.2.2 Application Circuit

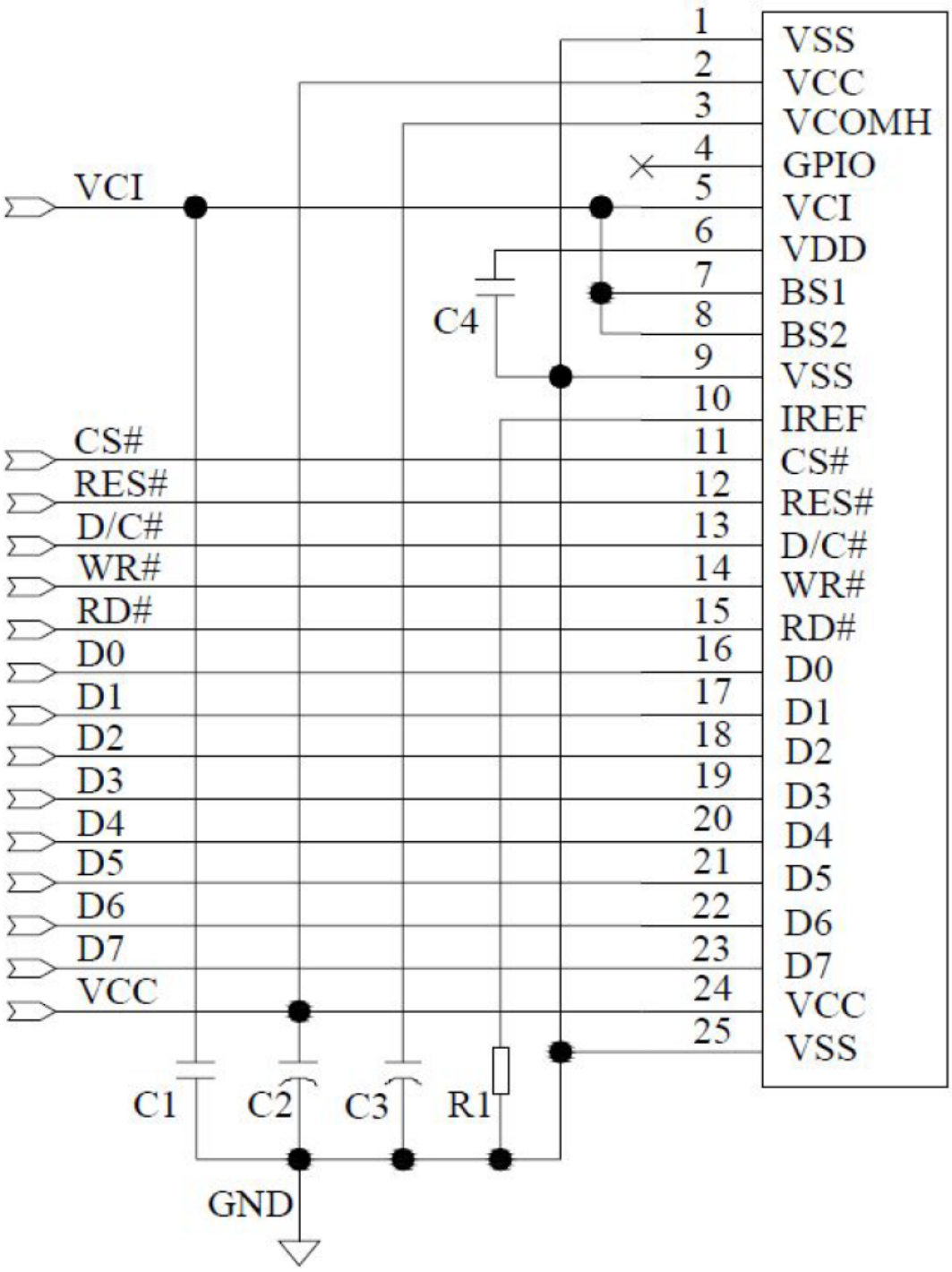
The configuration for 8-bit 8080-parallel interface mode, external VCC is shown in the following diagram:

The double byte command for 0xAB is used to enable or disable the VDD regulator.

No matter VDD is supplied by external source or internal regulated ; VCI must always be set equivalent to or higher than VDD.

VDD can be supplied regulated internally from VCI when A[0] is set to 1b.

(VCI must be > 2.6V)



Pin connected to MCU interface: D[7:0],RD#,WR#,D/C#,RES#,CS#

Recommended components

C1,C4: 4.7uF/35V(Tantalum type) or VISHAY (572D475X0025A2T)

C2,C3: 1uF/16V(0603)

R1: 2M ohm (0603) 1%

9. Optical Specification

Item		Symbol	Condition	Min	Typ.	Max.	Unit	Remark
Contrast Ratio		CR	θ=0°	≥2000:1		-		
View Angles		ΘT	--	≥160		-	Degree	
Response Time		Tr	25℃	-	10	-	us	
		Tf						
Chromaticity	White	x	Brightness is on	0.24	0.28	0.32		
		y		0.28	0.32	0.36		
Normal Mode Brightness		L	All pixels ON(1)	70	90	-	cd/m^2	
Standby Mode Brightness			Standby Mode 10% pixels ON(2)	-	20	-	cd/m^2	
Normal Mode Power Consumption		P	All pixels ON(1)	-	480	510	mW	
Standby Mode Power Consumption			Standby Mode 10% pixels ON(2)	-	45	60	mW	

Normal mode condition :

- Driving Voltage : 15V
- Contrast setting : 0x77
- Frame rate : 105Hz
- Duty setting : 1/128

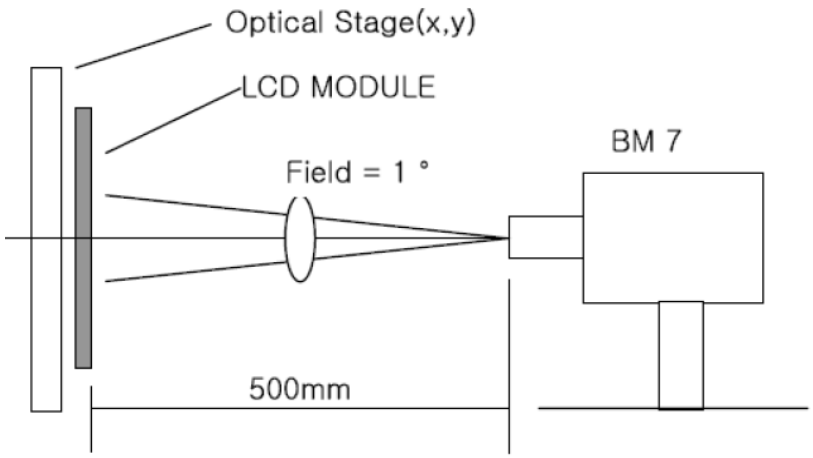
Standby mode condition :

- Driving Voltage : 15V
- Contrast setting : 0x14
- Frame rate : 105Hz
- Duty setting : 1/128

Note 1: Definition of optical measurement system.

Temperature = 25℃(±3℃)

LED back-light: ON, Environment brightness < 150 lx

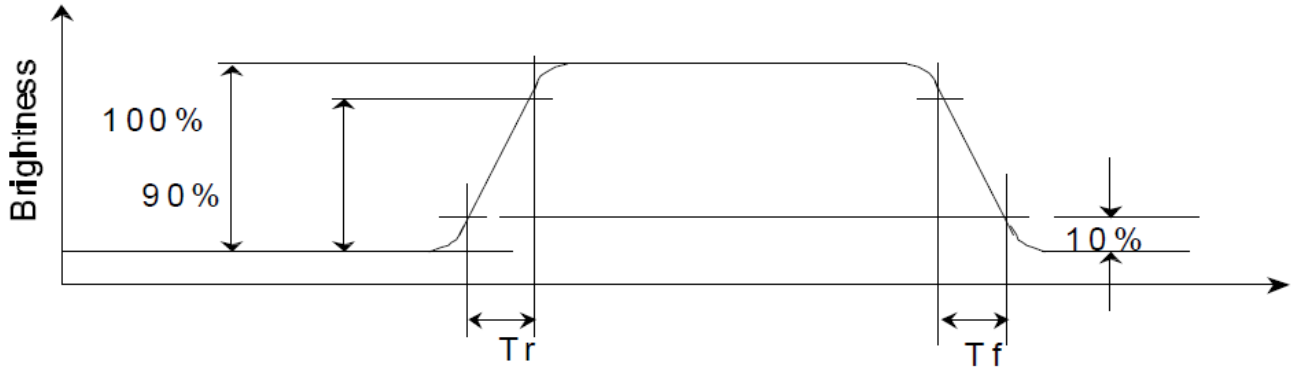


Note 2: Contrast ratio is defined as follow:

$$\text{Contrast Ratio} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

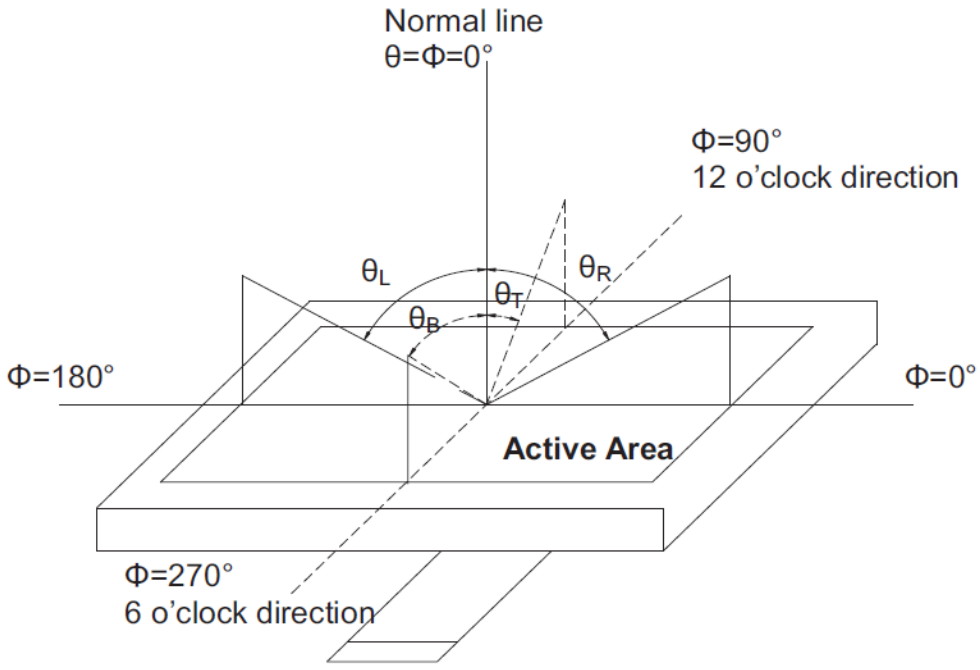
Note 3: Response time is defined as follow:

The definition of turn-on response time Tr is the time interval between a pixel reaching 10% of steady state luminance and 90% of steady state luminance.
The definition of turn-off response time Tf is the time interval between a pixel reaching 90% of steady state luminance and 10% of steady state luminance.



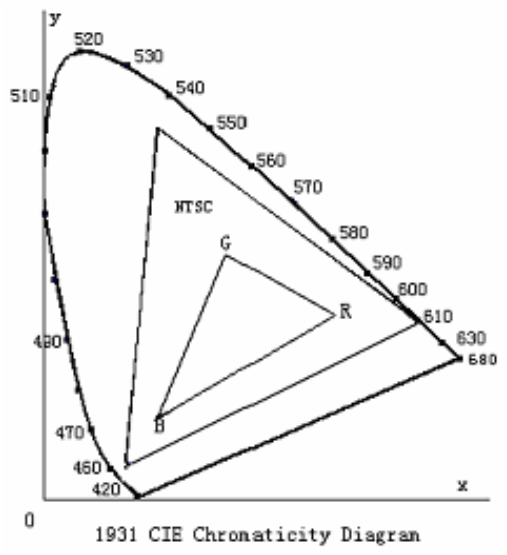
Note 4: Viewing angle range is defined as follow:

Viewing angle is measured at the center point of the LCD.



Note 5: Color chromaticity is defined as follow: (CIE1931)

Color coordinates measured at center point of LCD.



$$S = \frac{\text{area of RGB triangle}}{\text{area of NTSC triangle}} \times 100\%$$

Note 6: Luminance is defined as follow:

Luminance is defined as the brightness of all pixels “White” at the center of display area on optimum contrast.

10. Environmental / Reliability Tests

No	Test Item	Condition	Judgment criteria
1	High Temp Operation	Ta= +70℃, 120hrs	Per table in below
2	Low Temp Operation	Ta= -40℃, 120hrs	Per table in below
3	High Temp Storage	Ta= +85℃, 240hrs	Per table in below
4	Low Temp Storage	Ta= -40℃, 120hrs	Per table in below
5	High Temp & High Humidity Storage	Ta=+60℃, 90% RH, 120 hours	Per table in below (polarizer discoloration is excluded)
6	Thermal Shock (Non-operation)	-40℃ 30 min~+85℃ 30 min, Change time:5min, 10 Cycles	Per table in below
7	ESD (Operation)	Air discharge model, ±8kV, 10 times	Per table in below
8	Vibration (Non-operation)	Frequency : 5~50HZ, 0.5G Scan rate : 1 oct/min Time : 2 hrs/axis Test axis : X, Y, Z	Per table in below
9	Shock (Non-operation)	-40°C ~85°C (-40°C /30min; transit /3min; 85°C /30min; transit /3min) 1cycle: 66min, 100 cycles	Per table in below
10	Package Drop Test	Height: 120cm Sequence : 1 angle 3 edges and 6 faces Cycles: 1	Per table in below

INSPECTION	CRITERION(after test)
Appearance	No Crack on the FPC, on the OLED Panel
Alignment of OLED Panel	No Bubbles in the OLED Panel No other Defects of Alignment in Active area
Electrical current	Within device specifications
Function / Display	No Broken Circuit, No Short Circuit or No Black line No Other Defects of Display

11. Precautions for Use of OLED Modules

11.1 Safety

The liquid crystal in the OLED is poisonous. Do not put it in your mouth. If the liquid crystal touches your skin or clothes, wash it off immediately using soap and water.

11.2 Handling

A. The OLED and touch panel is made of plate glass. Do not subject the panel to mechanical shock or to excessive force on its surface.
B. Do not handle the product by holding the flexible pattern portion in order to assure the reliability
C. Transparency is an important factor for the touch panel. Please wear clear finger sacks, gloves and mask to protect the touch panel from finger print or stain and also hold the portion outside the view area when handling the touch panel.
D. Provide a space so that the panel does not come into contact with other components.
E. To protect the product from external force, put a covering lens (acrylic board or similar board) and keep an appropriate gap between them.
F. Transparent electrodes may be disconnected if the panel is used under environmental conditions where dew condensation occurs.
G. Property of semiconductor devices may be affected when they are exposed to light, possibly resulting in IC malfunctions.
H. To prevent such IC malfunctions, your design and mounting layout shall be done in the way that the IC is not exposed to light in actual use.

11.3 Static Electricity

A. Ground soldering iron tips, tools and testers when they are in operation.
B. Ground your body when handling the products.
C. Power on the OLED module before applying the voltage to the input terminals.
D. Do not apply voltage which exceeds the absolute maximum rating.
E. Store the products in an anti-electrostatic bag or container.

11.4Storage

A. Store the products in a dark place at +25℃±10℃ with low humidity (40% RH to 60% RH). Don't expose to sunlight or fluorescent light.
B. Storage in a clean environment, free from dust, active gas, and solvent.

11.5 Cleaning

A. Do not wipe the touch panel with dry cloth, as it may cause scratch.
B. Wipe off the stain on the product by using soft cloth moistened with ethanol. Do not allow ethanol to get in between the upper film and the bottom glass. It may cause peeling issue or defective operation. Do not use any organic solvent or detergent other than ethanol.

11.6 Cautions for installing and assembling

A. Bezel edge must be positioned in the area between the Active area and View area. The bezel may press the touch screen and cause activation if the edge touches the active area. A gap of approximately 0.5mm is needed between the bezel and the top electrode. It may cause unexpected activation if the gap is too narrow. There is a tolerance of 0.2 to 0.3mm for the outside dimensions of the touch panel and tail. A gap must be made to absorb the tolerance in the case and connector.
B. In order to make the display assembly stable and firm, DLC recommends to design some supporting at the display backside, especially for the display with tape-attached touch panel, such supporting is important and essential, or else, the display may drop-off from front after some period of time.
C. Do not display the fixed pattern for a long time because it may develop image sticking due to the LCD structure. If the screen is displayed with fixed pattern, use a screen saver.