# DLC Display Co., Limited

# 德爾西顯示器有限公司

MODEL No: DLC0139BQOG

TEL: 86-755-86029824

FAX: 86-755-86029827

E-MAIL: sales@dlcdisplay.com

WEB: www.dlcdisplay.com

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# Record of Revision

| Date | Revision No. | Summary |
|---|---|---|
| 2018-04-28 | 1.0 | Rev 1.0 was issued |
| 2018-05-29 | 1.1 | Add 8.4 Power IC Application Circuit<br>8.5 Display Initial Setting |
| | | |

## 1. Scope

This data sheet is to introduce the specification of DLC0139BQOG, AMOLED display module. It is composed of an AMOLED panel, driver IC and FPC. The 1.39″ display area contains 400 (RGB) x 400 pixels.

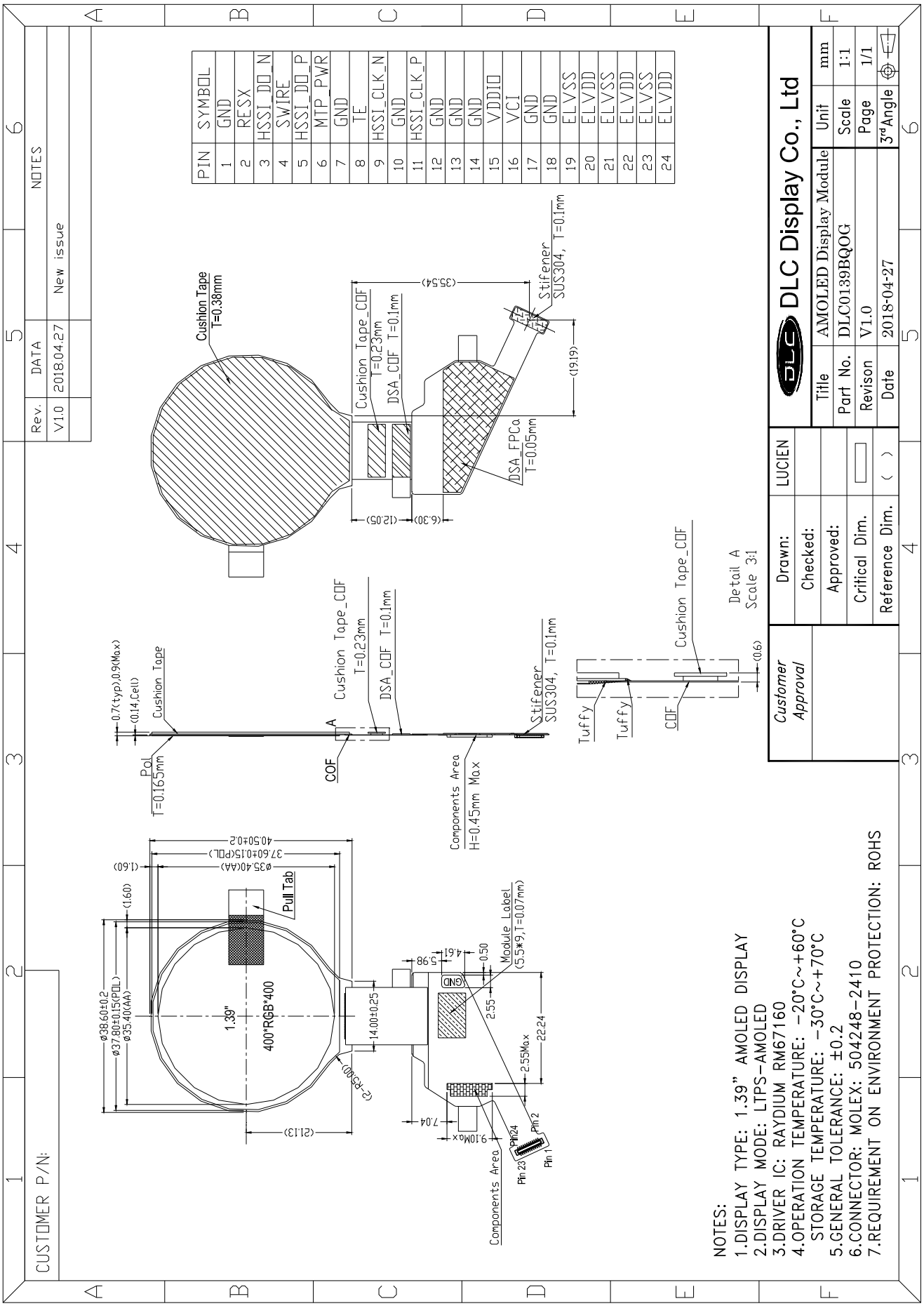
## 2. Application

Digital equipments which need display, instrumentation, remote control, electronic product.

## 3. General Information

| Item | Contents | Unit |
|---|---|---|
| Size | 1.39 | inch |
| Display Technology | AMOLED | / |
| Resolution | 400(RGB)×400 | / |
| Display Color | 16.7M | / |
| Interface | MIPI | / |
| Outline Dimension | 38.6 x 40.5 x 0.7 | mm |
| Active Area | Φ35.4 | mm |
| Driver IC | RAYDIUM RM67160 | / |
| Operating Temperature | -20℃ ~ +60℃ | / |
| Storage Temperature | -30℃ ~ +70℃ | / |

# 4. Outline Drawing



## 5. Interface signals

| PIN NO. | PIN NAME | DESCRIPTION |
|---|---|---|
| 1 | GND | Power ground |
| 2 | RESX | Device reset signal (0: Enable; 1: Disable) |
| 3 | HSSI_D0_N | MIPI data negative signal |
| 4 | SWIRE | SWIRE signal for PWR IC control |
| 5 | HSSI_D0_P | MIPI data positive signal |
| 6 | MTP_PWR | MTP (need to indicate to connect GND or NC) |
| 7 | GND | Power ground |
| 8 | TE | Vsync(vertical sync) signal output from panel to avoid tearing effect |
| 9 | HSSI_CLK_N | MIPI negative clock signal |
| 10 | GND | Power ground |
| 11 | HSSI_CLK_P | MIPI positive clock signal |
| 12 | GND | Power ground |
| 13 | GND | Power ground |
| 14 | GND | Power ground |
| 15 | VDDIO | Power supply for interface system |
| 16 | VCI | Power supply for analog |
| 17 | GND | Power ground |
| 18 | GND | Power ground |
| 19 | ELVSS | AMOLED power negative |
| 20 | ELVDD | AMOLED power positive |
| 21 | ELVSS | AMOLED power negative |
| 22 | ELVDD | AMOLED power positive |
| 23 | ELVSS | AMOLED power negative |
| 24 | ELVDD | AMOLED power positive |

FPCA recommended connector: 504248-2410 (Molex)
Main board recommended connector: 504208-2410 (Molex)

# 6. Environment Conditions

## 6.1 Electrical Absolute max. ratings

| Parameter | Symbol | MIN | MAX | Unit | Remark |
|---|---|---|---|---|---|
| Supply voltage | VCI | -0.3 | 5.5 | V | Power for digital circuit |
| | VDDIO | -0.3 | 5.5 | V | Power for interface circuit |
| | ELVDD | - | 5.0 | V | Power for OLED |
| | ELVSS | -5.0 | - | V | Power for OLED |

Note1: All of the voltages listed above are with respective to GND= 0V.
Note2: Device is subject to be damaged permanently if stresses beyond those absolute maximum ratings listed above.

## 6.2 Environment Conditions

| Item | Symbol | MIN | MAX | Unit | Remark |
|---|---|---|---|---|---|
| Operating Temperature | TOPR | -20 | 60 | ℃ | |
| Storage Temperature | TSTG | -30 | 70 | ℃ | |

# 7. Electrical Specifications

## 7.1 Electrical characteristics

| Item | | Symbol | MIN | TYP | MAX | Unit | Remark |
|---|---|---|---|---|---|---|---|
| Supply voltage | | VCI | 2.7 | 2.8 | 3.6 | V | |
| | | VDDIO | 1.65 | 1.8 | 3.3 | V | |
| | | ELVDD | 4.55 | 4.60 | 4.65 | V | |
| | | ELVSS | -2.35 | -2.4 | -2.45 | V | |
| Input voltage | "H" level | VIH | 0.8*VDDIO | - | VDDIO | V | VDDIO= 1.65V~3.3V |
| | "L" level | VIL | 0 | - | 0.2*VDDIO | V | |
| Output voltage | "H" level | VOH | 0.8*VDDIO | - | VDDIO | V | |
| | "L" level | VOL | 0 | - | 0.2*VDDIO | V | |

Note: The operation is guaranteed under the recommended operating conditions only. The operation is not guaranteed if a quick voltage change occurs during the operation. To prevent the noise, a bypass capacitor must be inserted into the line closed to the power pin.

## 7.2 Power Consumption

| Display Mode | Item | Symbol | Typ | Max |
|---|---|---|---|---|
| | | | Current(mA) | Current(mA) |
| 100% Pixel On (Normal mode) | Current of VDDIO | $I_{VDDIO}$ | 3.0 | - |
| | Current of VCI | $I_{VCI}$ | 6.1 | - |
| | Current of ELVSS | $I_{ELVSS}$ | 20.5 | - |
| 50% Pixel On (Normal mode) | Current of VDDIO | $I_{VDDIO}$ | 3.0 | - |
| | Current of VCI | $I_{VCI}$ | 6.1 | - |
| | Current of ELVSS | $I_{ELVSS}$ | 10.3 | - |
| ALL Pixel Off (Normal mode) | Current of VDDIO | $I_{VDDIO}$ | 3.0 | - |
| | Current of VCI | $I_{VCI}$ | 6.0 | - |
| | Current of ELVSS | $I_{ELVSS}$ | 0.0 | - |
| ALL Pixel Off (Standby mode) | Current of VDDIO | $I_{VDDIO}$ | - | 0.0 |
| | Current of VCI | $I_{VCI}$ | - | <2uA |
| | Current of ELVSS | $I_{ELVSS}$ | - | 0 |

Note1: Power supply: VDDIO=1.8V , VCI=2.8V.
Note2: Frame frequency: Frame=60Hz@25degC, Brightness 300nits MIPI CMD mode.

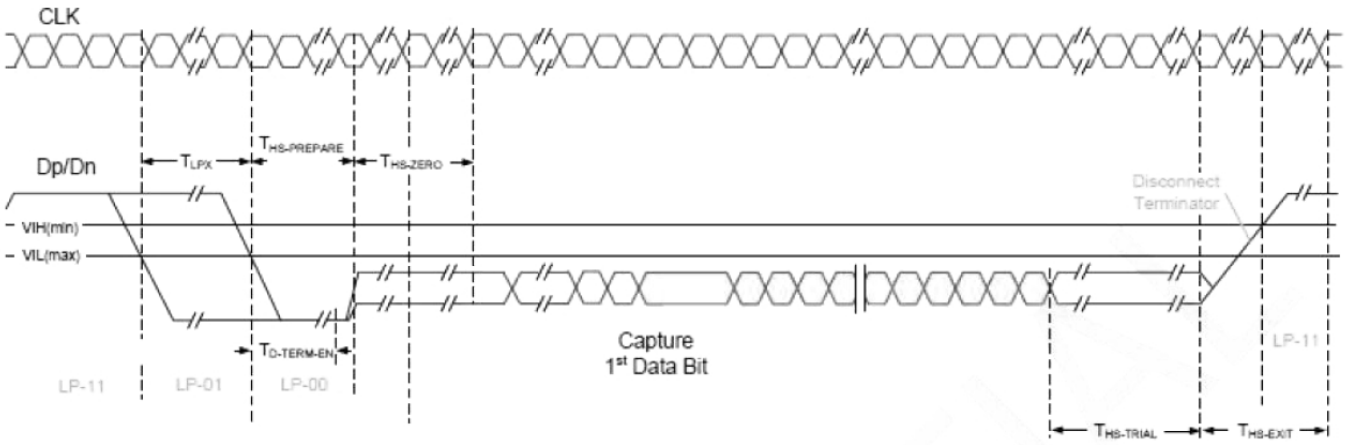
| Display Mode | Item | Symbol | Typ | Max |
|---|---|---|---|---|
| | | | Current(mA) | Current(mA) |
| 10% Pixel On (Idle mode) | Current of VDDIO | $I_{VDDIO}$ | 0.6 | - |
| | Current of VCI | $I_{VCI}$ | 2.6 | - |
| | Current of ELVSS | $I_{ELVSS}$ | 0.2 | - |

Note1: Power supply: VDDIO=1.8V , VCI=2.8V.
Note2: Frame frequency: Frame=15Hz@25degC, Brightness 30nits MIPI CMD mode.

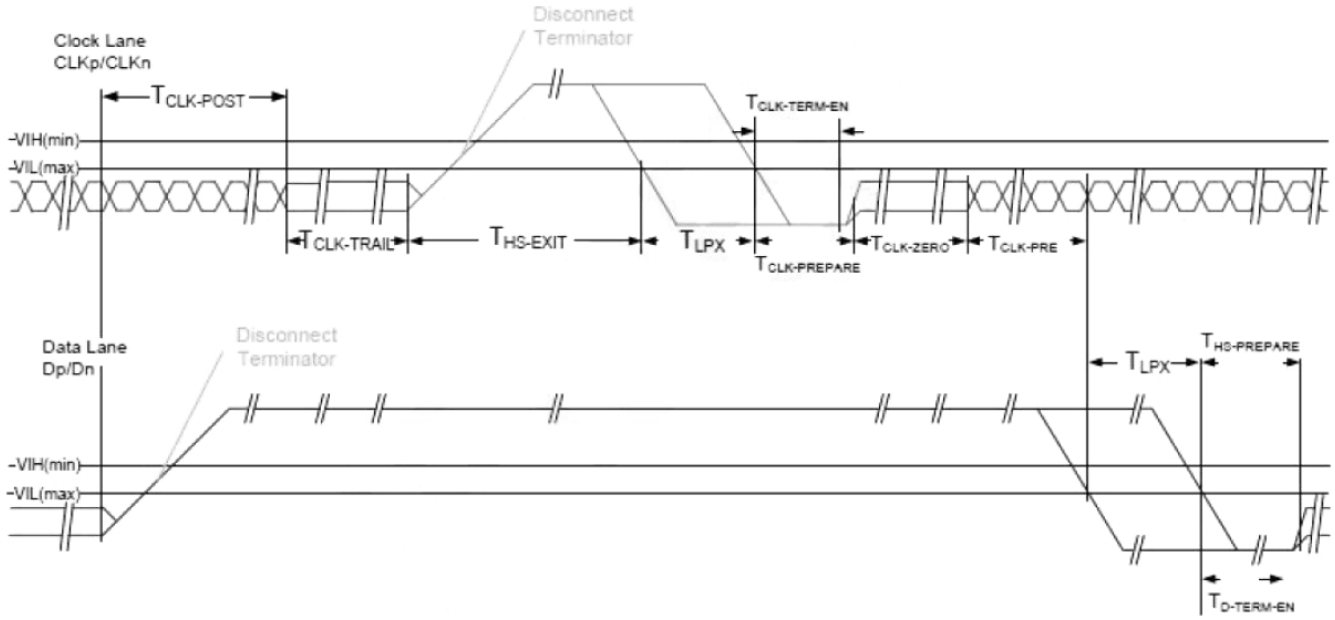
# 8. Command/AC Timing

## 8.1.MIPI Interface Characteristics

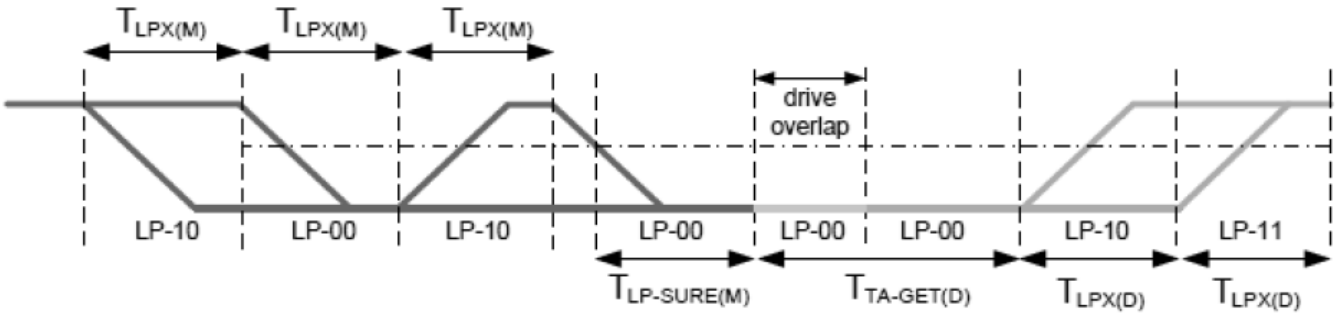
HS Data Transmission Burst




➢ HS clock transmission

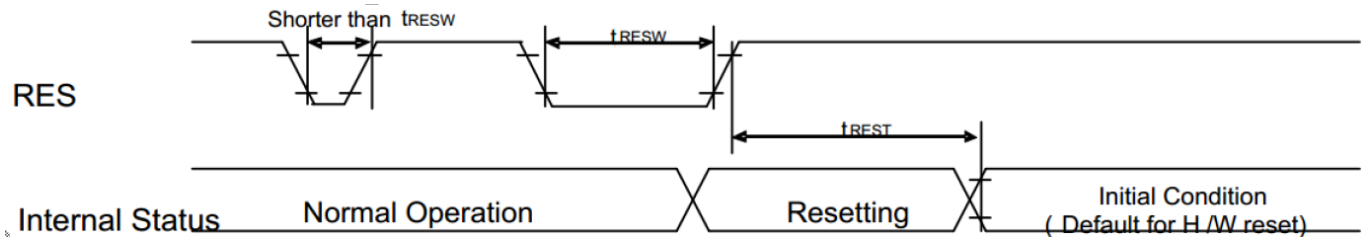



Turnaround Procedure



| Timing Parameters: Parameter | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| TCLK-POST | Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of THS-TRAIL to the beginning of TCLK-TRAIL . | 60ns + 52*UI | - | - | ns |
| TCLK-TRAIL | Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst. | 60 | - | - | ns |
| THS-EXIT | Time that the transmitter drives LP-11 following a HS burst. | 300 | - | - | ns |
| TCLK-TERM-EN | Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses VIL,MAX . | Time for Dn to reach VTERM-EN | - | 38 | ns |
| TCLK-PREPARE | Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission. | 38 | - | 95 | ns |
| TCLK-PRE | Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode. | 8 | - | - | UI |
| TCLK-PREPARE + TCLK-ZERO | TCLK-PREPARE + time that the transmitter drives the HS-0 state prior to starting the Clock. | 300 | - | - | ns |
| TD-TERM-EN | Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses VIL,MAX . | Time for Dn to reach VTERM-EN | - | 35 ns +4*UI | ns |
| THS-PREPARE | Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission | 40ns + 4*UI | - | 60 ns + 6*UI | ns |
| THS-PREPARE + THS-ZERO | THS-PREPARE + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence. | 145ns + 10*UI | - | - | ns |
| THS-TRAIL | Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst | 60ns+4*UI | - | - | ns |
| TLPX(M) | Transmitted length of any Low-Power state period of MCU to display module | 50 | - | 150 | ns |
| TTA-SURE(M) | Time that the display module waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround. | TLPX(M) | - | 2*TLPX(M) | ns |
| TLPX(D) | Transmitted length of any Low-Power state period of display module to MCU | 50 | - | 150 | ns |
| TTA-GET(D) | Time that the display module drives the Bridge state (LP-00) after accepting control during a Link Turnaround. | 5*TLPX(D) | - | - | ns |
| TTA-GO(D) | Time that the display module drives the Bridge state (LP-00) before releasing control during a Link Turnaround. | 4*TLPX(D) | - | - | ns |
| TTA-SURE(D) | Time that the MPU waits after the LP- 10 state before transmitting the Bridge state (LP-00) during a Link Turnaround. | TLPX(D) | - | 2*TLPX(D) | ns |

8.2 Reset Timing




IOVDD=1.65 to 1.95V, VDD=2.8 to 3.1V, AGND=DGND=0V, Ta=-40 to 85℃

| Item | Symbol | Related Pins | MIN | TYP | MAX | Unit | Remark |
|---|---|---|---|---|---|---|---|
| Reset low pulse width | tRESW | RESX | 10 | - | - | us | |
| Reset complete time | tREST | | - | - | 5 | ms | When reset applied during Sleep in mod |
| | | | | | 120 | ms | When reset applied during Sleep out mode |

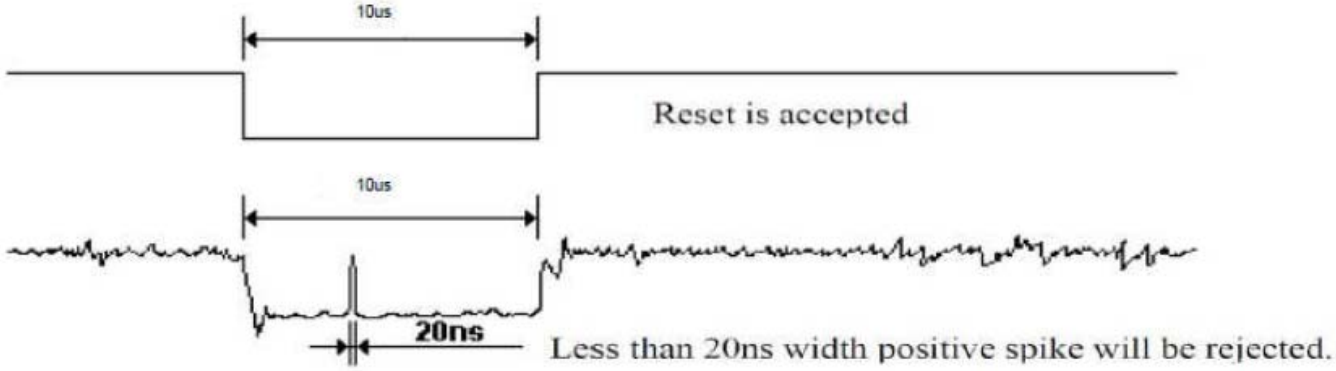
Note 1: Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

| RESX Pulse | Action |
|---|---|
| Shorter than 5s | Reset Rejected |
| Longer than 10s | Reset |
| Between 5s and 15s | Reset starts<br>(It depends on voltage and temperature condition) |

Note 2: During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then return to Default condition for H/W reset.

Note 3: During Reset Complete Time, data in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of RESX.

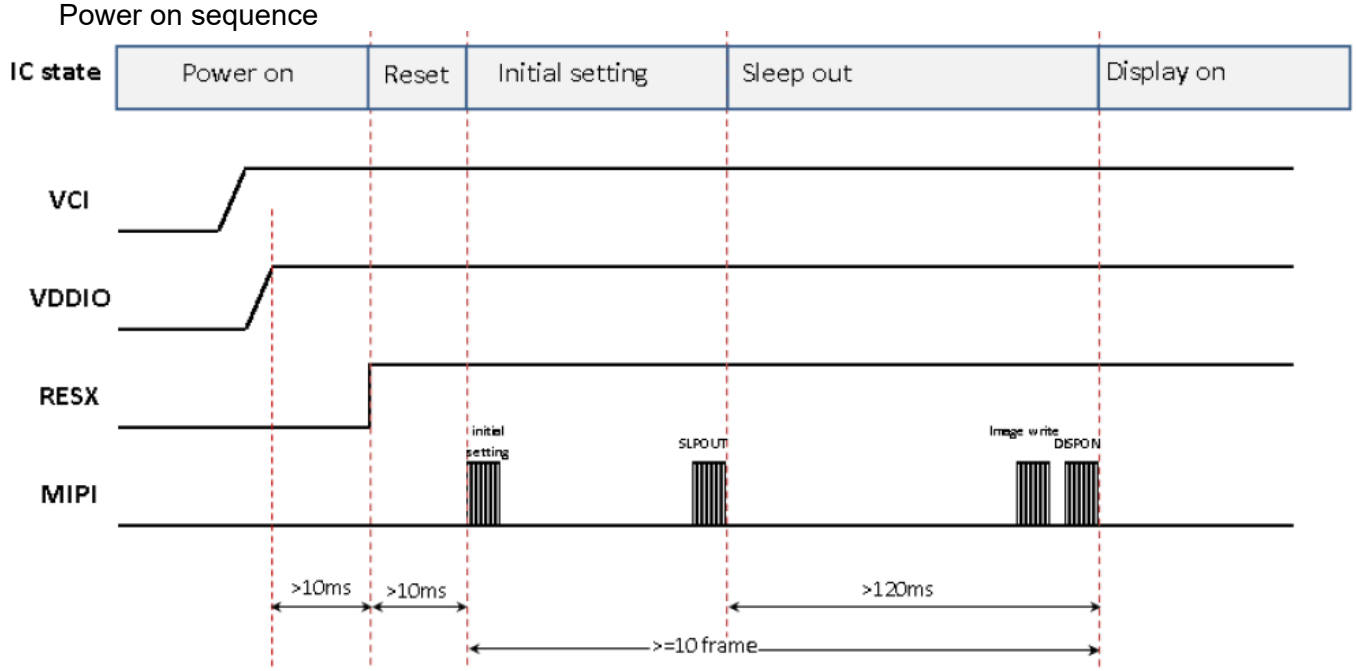
Note 4: Spike Rejection also applies during a valid reset pulse as shown below:



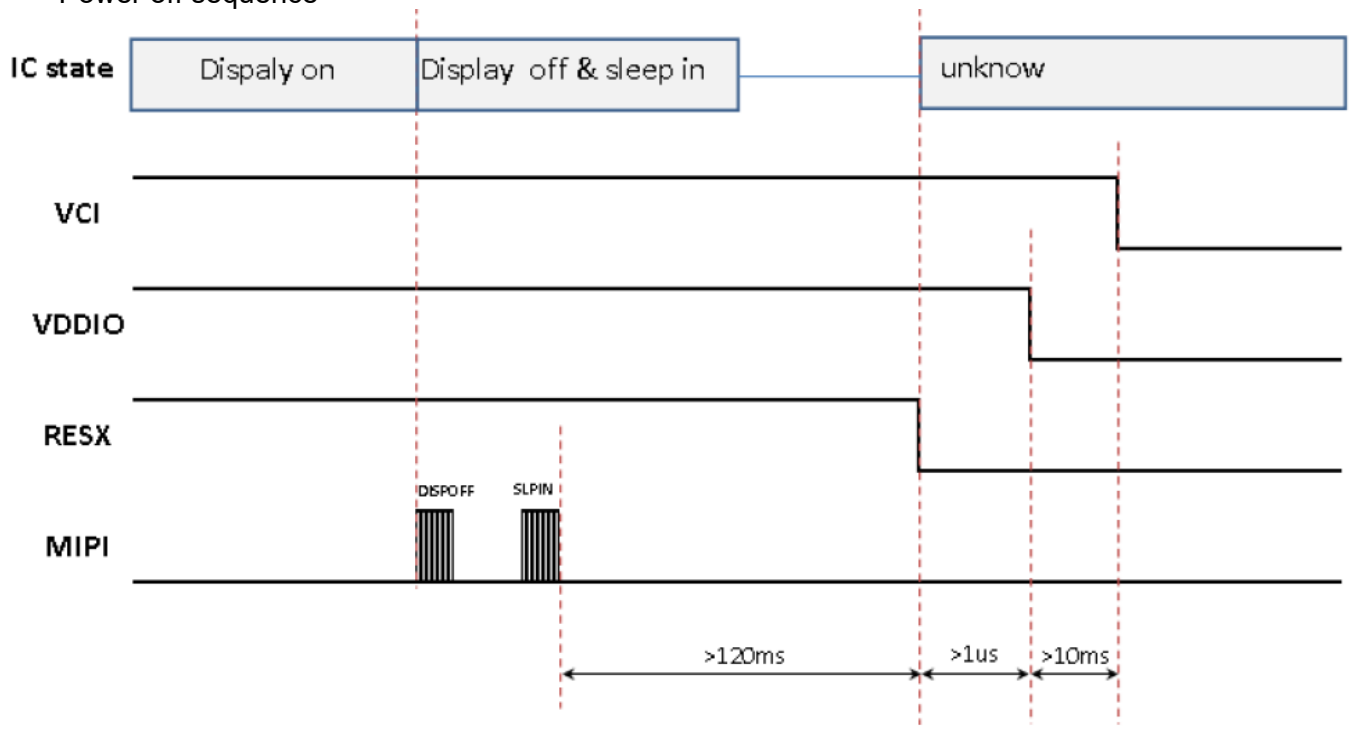

Note 5: It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

## 8.3 Operating Power Sequence

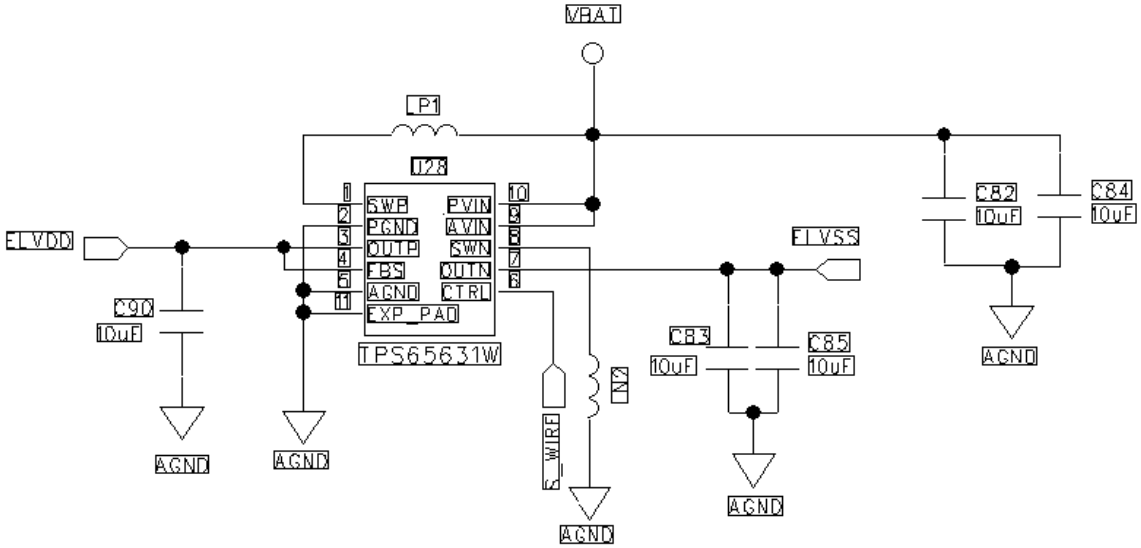
Power on sequence




Power off sequence



## 8.4 Power IC Application Circuit




Note: OLED Power IC: TPS65631W
Input: VBAT (2.9v ~ 4.4v)
Output: ELVDD, ELVSS

## 8.5 Display Initial Setting

| Recommended power on initial sequence | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Step | Instruction | Delay time | R/W | MIPI Data Type | Address | | Data hex. | Description |
| | | | | | MIPI | Others | | |
| 1 | Turn on VCI | | | | | | | VCI=2.8v |
| 2 | Turn on VDDIO | | | | | | | VDDIO=1.8v |
| 3 | Delay | No limit | | | | | | |
| 4 | REST pin low | 20us | | | | | | |
| 5 | REST pin high | | | | | | | |
| 6 | Delay | 5ms | | | | | | |
| 7 | | | W | 0x15 | FE | FE00 | 00 | |
| 8 | | | W | 0x15 | 35 | 3500 | 01 | |
| 9 | Sleep out | | W | 0x05 | 11 | 1100 | 00 | |
| 10 | Delay | 300ms | | | | | | |
| 11 | Display on | | W | 0x05 | 29 | 2900 | 00 | |

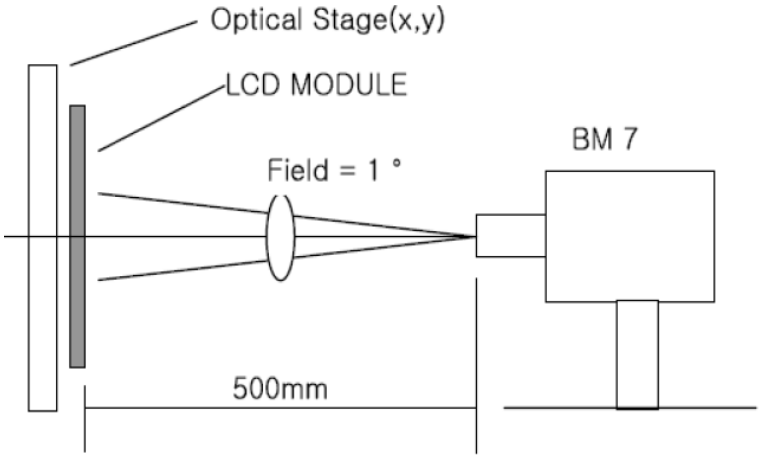
## 9. Optical Specification

| Item | | Symbol | Condition | Min | Typ. | Max. | Unit | Remark |
|---|---|---|---|---|---|---|---|---|
| Contrast Ratio | | CR | θ=0° | - | 10,000 | - | | Note1 Note2 |
| View Angles | | ΘT | Cr≥10 | 80 | - | - | Degree | Note 4 |
| | | ΘB | | 80 | - | - | | |
| | | ΘL | | 80 | - | - | | |
| | | ΘR | | 80 | - | - | | |
| Optical Switching Time | | (Tr+Tf)/2 | 25℃ | - | <4 | - | ms | Note1 Note3 |
| Chromaticity | White | x | Brightness is on | 0.27 | 0.30 | 0.33 | | Note5, Note1 |
| | | y | | 0.28 | 0.31 | 0.34 | | |
| | Red | x | | 0.64 | 0.67 | 0.70 | | |
| | | y | | 0.30 | 0.33 | 0.36 | | |
| | Green | x | | 0.19 | 0.24 | 0.29 | | |
| | | y | | 0.65 | 0.70 | 0.75 | | |
| | Blue | x | | 0.09 | 0.13 | 0.17 | | |
| | | y | | 0.025 | 0.065 | 0.105 | | |
| Luminance | | L | | 250 | 300 | - | cd/m2 | Note1 Note6 |
| Luminance Uniformity | | - | - | 80 | - | - | % | Note7 |
| NTSC | | - | - | 85 | 100 | - | % | |
| Gamma | | - | - | 1.9 | 2.2 | 2.5 | | |

Note 1: Definition of optical measurement system.

Temperature = 25℃(±3℃)

LED back-light: ON, Environment brightness < 150 lx

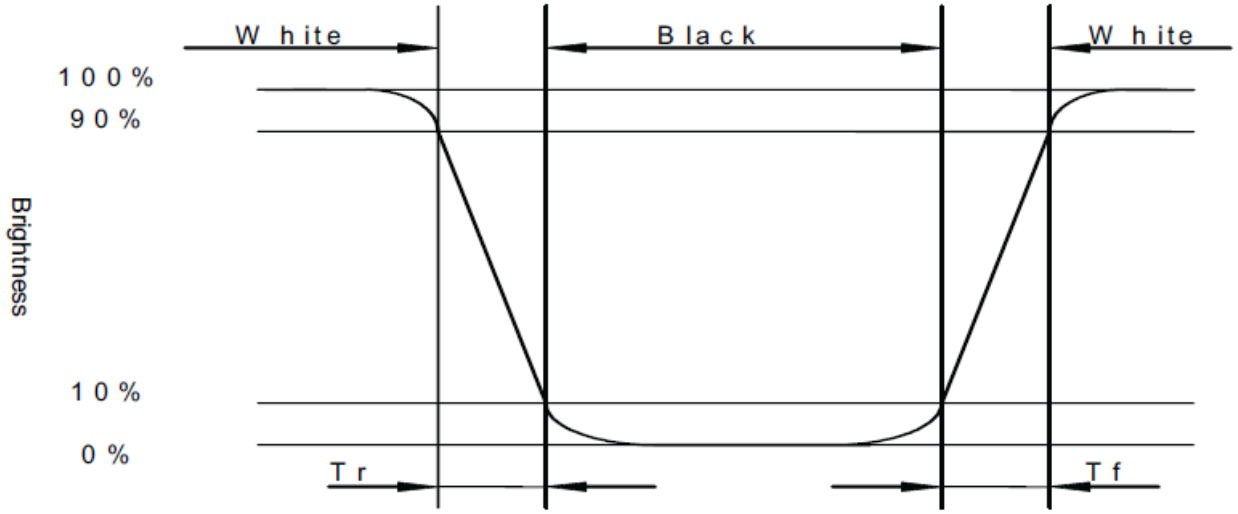


Note 2: Contrast ratio is defined as follow:

$$\text{Contrast Ratio} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

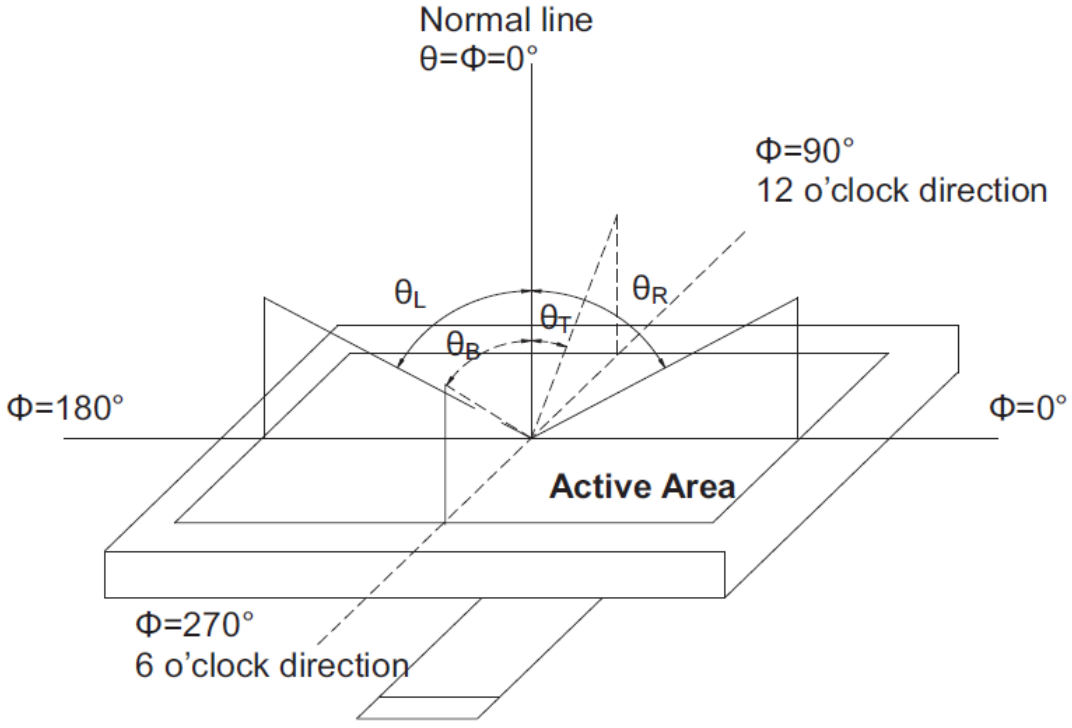
Note 3: Response time is defined as follow:

Response time is the time required for the display to transition from black to white (Rise Time, Tr) and from white to black(Decay Time, Tf).



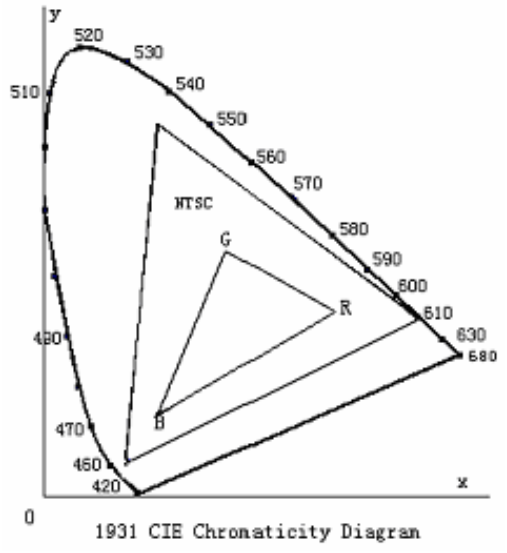

Note 4: Viewing angle range is defined as follow:

Viewing angle is measured at the center point of the LCD.



## Note 5: Color chromaticity is defined as follow: (CIE1931)

Color coordinates measured at center point of LCD.




$$S = \frac{\text{area of RGB triangle}}{\text{area of NTSC triangle}} \times 100\%$$

## Note 6: Luminance is defined as follow:

Luminance is defined as the brightness of all pixels “White” at the center of display area on optimum contrast.

## Note 7: Luminance Uniformity

- Measurement equipment: CS2000 or similar equipment.
- Measuring surroundings: Dark room.
- Measuring temperature: Ta=25℃.
- The data are measured after OLEDs are lighted on for more than 5 minutes and all pixels are fully white.
- The Luminance Uniformity is calculated by using following formula:

WHITE = Lp (Min.) / Lp (Max.)×100 (%)
Lp (Min.) = Minimum Luminance with all white pixels (P1, P2, P3, P4, P5)
Lp (Max.) = Maximum Luminance with all white pixels (P1, P2, P3, P4, P5)

## 10. Environmental / Reliability Tests

| No | Test Item | Condition | Judgment criteria |
|---|---|---|---|
| 1 | High Temp Operation | Ts=+60℃, 120hrs | Per table in below |
| 2 | Low Temp Operation | Ta=-20℃, 120hrs | Per table in below |
| 3 | High Temp Storage | Ta=+70℃, 120hrs | Per table in below |
| 4 | Low Temp Storage | Ta=-30℃, 120hrs | Per table in below |
| 5 | High Temp & High Humidity Storage | Ta=+60℃, 90% RH<br>120 hours | Per table in below<br>(polarizer discoloration is excluded) |
| 6 | Thermal Shock (Non-operation) | -30°C ~70°C，Dwell for 30 min. 100 cycles | Per table in below |
| 7 | ESD (Operation) | Voltage:±8KV, R: 330Ω, C: 150pF<br>Air discharge, 10time | Per table in below |
| 8 | Vibration | Frequency ： 10Hz~55Hz~10Hz<br>Amplitude：1.5mm,<br>X，Y，Z direction for total 3hours<br>(Packing condition) | Per table in below |
| 9 | Package<br>Drop Test | Drop to the ground from 75cm height, one time, every side of carton. (Packing condition) | Per table in below |

| INSPECTION | CRITERION(after test) |
|---|---|
| Appearance | No Crack on the FPC, on the OLED Panel |
| Alignment of OLED Panel | No Bubbles in the OLED Panel<br>No other Defects of Alignment in Active area |
| Electrical current | Within device specifications<br>Current consumption: within · 50% of initial value. |
| Function / Display | No Broken Circuit, No Short Circuit or No Black line<br>No Other Defects of Display |

# 11. Precautions for Use of OLED Modules

## 11.1 Safety

The liquid crystal in the OLED is poisonous. Do not put it in your mouth. If the liquid crystal touches your skin or clothes, wash it off immediately using soap and water.

## 11.2 Handling

A. The OLED and touch panel is made of plate glass. Do not subject the panel to mechanical shock or to excessive force on its surface.
B. Do not handle the product by holding the flexible pattern portion in order to assure the reliability
C. Transparency is an important factor for the touch panel. Please wear clear finger sacks, gloves and mask to protect the touch panel from finger print or stain and also hold the portion outside the view area when handling the touch panel.
D. Provide a space so that the panel does not come into contact with other components.
E. To protect the product from external force, put a covering lens (acrylic board or similar board) and keep an appropriate gap between them.
F. Transparent electrodes may be disconnected if the panel is used under environmental conditions where dew condensation occurs.
G. Property of semiconductor devices may be affected when they are exposed to light, possibly resulting in IC malfunctions.
H. To prevent such IC malfunctions, your design and mounting layout shall be done in the way that the IC is not exposed to light in actual use.

## 11.3 Static Electricity

A. Ground soldering iron tips, tools and testers when they are in operation.
B. Ground your body when handling the products.
C. Power on the OLED module before applying the voltage to the input terminals.
D. Do not apply voltage which exceeds the absolute maximum rating.
E. Store the products in an anti-electrostatic bag or container.

## 11.4Storage

A. Store the products in a dark place at +25℃±10℃ with low humidity (40% RH to 60% RH).
Don't expose to sunlight or fluorescent light.
B. Storage in a clean environment, free from dust, active gas, and solvent.

## 11.5 Cleaning

A. Do not wipe the touch panel with dry cloth, as it may cause scratch.
B. Wipe off the stain on the product by using soft cloth moistened with ethanol. Do not allow ethanol to get in between the upper film and the bottom glass. It may cause peeling issue or defective operation. Do not use any organic solvent or detergent other than ethanol.

## 11.6 Cautions for installing and assembling

A. Bezel edge must be positioned in the area between the Active area and View area. The bezel may press the touch screen and cause activation if the edge touches the active area. A gap of approximately 0.5mm is needed between the bezel and the top electrode. It may cause unexpected activation if the gap is too narrow. There is a tolerance of 0.2 to 0.3mm for the outside dimensions of the touch panel and tail. A gap must be made to absorb the tolerance in the case and connector.
B. In order to make the display assembly stable and firm, DLC recommends to design some supporting at the display backside, especially for the display with tape-attached touch panel, such supporting is important and essential, or else, the display may drop-off from front after some period of time.
C. Do not display the fixed pattern for a long time because it may develop image sticking due to the LCD structure. If the screen is displayed with fixed pattern, use a screen saver.