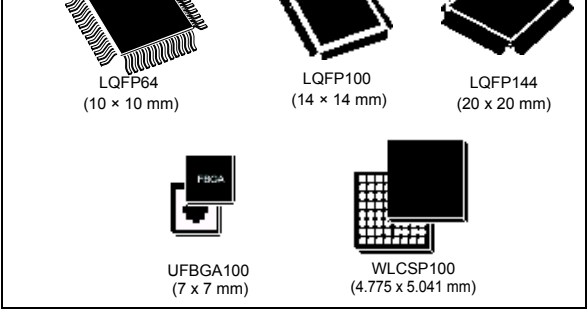


ARM<sup>®</sup> Cortex<sup>®</sup>-M4 32b MCU+FPU, up to 512KB Flash, 64KB SRAM, FSMC, 2 ADCs, 1 DAC ch., 4 comp, 2 Op-Amp, 2.0-3.6 V

Datasheet - production data

## Features

- Core: ARM<sup>®</sup> Cortex<sup>®</sup>-M4 32-bit CPU with 72 MHz FPU, single-cycle multiplication and HW division, DSP instruction and MPU (memory protection unit)
  - Operating conditions:
    - $V_{DD}$ ,  $V_{DDA}$  voltage range: 2.0 V to 3.6 V
  - Memories
    - Up to 512 Kbytes of Flash memory
    - 64 Kbytes of SRAM, with HW parity check implemented on the first 32 Kbytes.
    - Flexible memory controller (FSMC) for static memories, with four Chip Select
  - CRC calculation unit
  - Reset and supply management
    - Power-on/Power-down reset (POR/PDR)
    - Programmable voltage detector (PVD)
    - Low-power modes: Sleep, Stop and Standby
    - $V_{BAT}$  supply for RTC and backup registers
  - Clock management
    - 4 to 32 MHz crystal oscillator
    - 32 kHz oscillator for RTC with calibration
    - Internal 8 MHz RC with x 16 PLL option
    - Internal 40 kHz oscillator
  - Up to 115 fast I/Os
    - All mappable on external interrupt vectors
    - Several 5 V-tolerant
  - Interconnect matrix
  - 12-channel DMA controller
  - Two ADCs 0.20  $\mu$ s (up to 18 channels) with selectable resolution of 12/10/8/6 bits, 0 to 3.6 V conversion range, separate analog supply from 2.0 to 3.6 V
  - One 12-bit DAC channels with analog supply from 2.4 to 3.6 V
- 
- Four ultra-fast rail-to-rail analog comparators with analog supply from 2.0 to 3.6 V
  - Two operational amplifiers that can be used in PGA mode, all terminals accessible with analog supply from 2.4 to 3.6 V
  - Up to 24 capacitive sensing channels supporting touchkey, linear and rotary touch sensors
  - Up to 11 timers:
    - One 32-bit timer and two 16-bit timers with up to four IC/OC/PWM or pulse counter and quadrature (incremental) encoder input
    - One 16-bit 6-channel advanced-control timers, with up to six PWM channels, deadtime generation and emergency stop
    - One 16-bit timer with two IC/OCs, one OCN/PWM, deadtime generation and emergency stop
    - Two 16-bit timers with IC/OC/OCN/PWM, deadtime generation and emergency stop
    - Two watchdog timers (independent, window)
    - One SysTick timer: 24-bit downcounter
    - One 16-bit basic timers to drive the DAC
  - Calendar RTC with Alarm, periodic wakeup from Stop/Standby
  - Communication interfaces
    - CAN interface (2.0B Active)

- Three I<sup>2</sup>C Fast mode plus (1 Mbit/s) with 20 mA current sink, SMBus/PMBus, wakeup from STOP
- Up to five USART/UARTs (ISO 7816 interface, LIN, IrDA, modem control)
- Up to four SPIs, 4 to 16 programmable bit frames, two with multiplexed half/full duplex I<sup>2</sup>S interface
- USB 2.0 full-speed interface with LPM support
- Infrared transmitter
- SWD, Cortex<sup>®</sup>-M4 with FPU ETM, JTAG
- 96-bit unique ID

**Table 1. Device summary**

| Reference   | Part number                            |
|-------------|--|
| STM32F302xD | STM32F302RD, STM32F302VD, STM32F302ZD. |
| STM32F302xE | STM32F302RE, STM32F302VE, STM32F302ZE. |

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# 1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F302xD/E microcontrollers.

This STM32F302xD/E datasheet should be read in conjunction with the reference manual of STM32F302xB/C/D/E, STM32F302x6/8 devices (RM0365) available on STMicroelectronics website at [www.st.com](http://www.st.com).

For information on the ARM® Cortex®-M4 core with FPU, refer to the following documents:

- *Cortex® -M4 with FPU Technical Reference Manual*, available from the [www.arm.com](http://www.arm.com) website
- *STM32F3 and STM32F4 Series Cortex® -M4 programming manual* (PM0214) available on STMicroelectronics website at [www.st.com](http://www.st.com).



## 2 Description

The STM32F302xD/E family is based on the high-performance ARM® Cortex®-M4 32-bit RISC core with FPU operating at a frequency of 72 MHz, and embedding a floating point unit (FPU), a memory protection unit (MPU) and an embedded trace macrocell (ETM). The family incorporates high-speed embedded memories (512-Kbyte Flash memory, 64-Kbyte SRAM), a flexible memory controller (FSMC) for static memories (SRAM, PSRAM, NOR and NAND), and an extensive range of enhanced I/Os and peripherals connected to an AHB and two APB buses.

The devices offer two fast 12-bit ADCs (5 Msps), four comparators, two operational amplifiers, one DAC channel, a low-power RTC, up to two general-purpose 16-bit timers, one general-purpose 32-bit timer, and one timer dedicated to motor control. They also feature standard and advanced communication interfaces: up to three I<sup>2</sup>Cs, up to four SPIs (two SPIs are with multiplexed full-duplex I<sup>2</sup>Ss), three USARTs, up to two UARTs, CAN and USB. To achieve audio class accuracy, the I<sup>2</sup>S peripherals can be clocked via an external PLL.

The STM32F302xD/E family operates in the -40 to +85°C and -40 to +105°C temperature ranges from a 2.0 to 3.6 V power supply. A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F302xD/E family offers devices in different packages ranging from 64 to 144 pins.

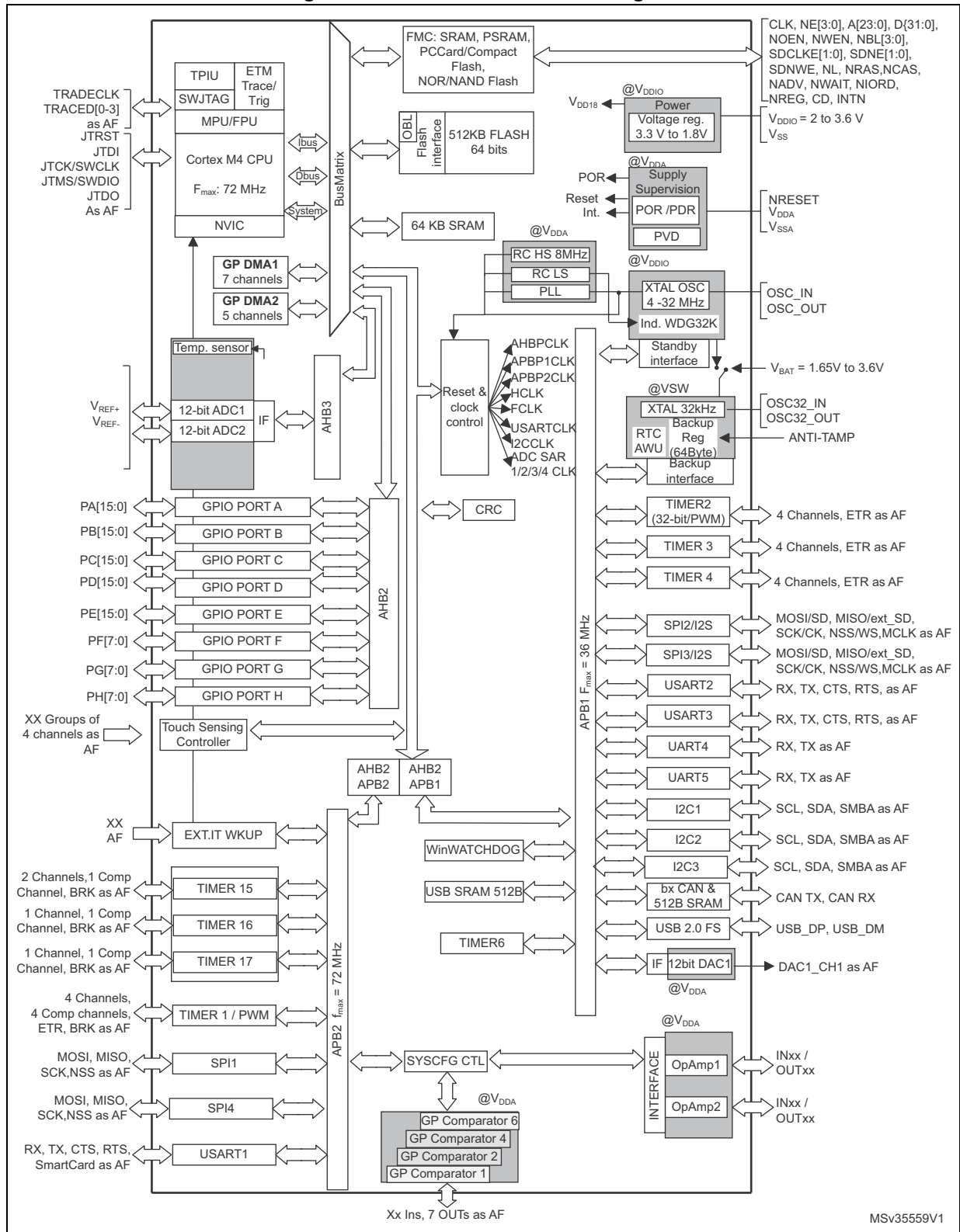
Depending on the device chosen, different sets of peripherals are included.

**Table 2. STM32F302xD/E family device features and peripheral counts**

| Peripheral                       |                                       | STM32F302Rx   |  | STM32F302Vx |     | STM32F302Zx      |     |
|----------------------------------|---------------------------------------|---|--|-------------|-----|------------------|-----|
| Flash (Kbytes)                   |                                       | 384   | 512  | 384         | 512 | 384              | 512 |
| SRAM (Kbytes) on data bus        |                                       | 64  |  |             |     |                  |     |
| FMC (flexible memory controller) |                                       | NO  |  | YES         |     |                  |     |
| Timers                           | Advanced control                      | 1 (16-bit)  |  |             |     |                  |     |
|                                  | General purpose                       | 5 (16-bit)<br>1 (32-bit)  |  |             |     |                  |     |
|                                  | Basic                                 | 1 (16-bit)  |  |             |     |                  |     |
|                                  | PWM channels (all) <sup>(1)</sup>     | 26  |  |             |     |                  |     |
|                                  | PWM channels (except complementary)   | 20  |  |             |     |                  |     |
| Communication interfaces         | SPI (I <sup>2</sup> S) <sup>(2)</sup> | 4(2)  |  |             |     |                  |     |
|                                  | I <sup>2</sup> C                      | 3   |  |             |     |                  |     |
|                                  | USART                                 | 3   |  |             |     |                  |     |
|                                  | UART                                  | 2   |  |             |     |                  |     |
|                                  | CAN                                   | 1   |  |             |     |                  |     |
|                                  | USB                                   | 1   |  |             |     |                  |     |
| GPIOs                            | Normal I/Os (TC, TTa)                 | 26  | 37 in WLCSP100,44 in LQFP100 and UFBGA100    |             |     | 45               |     |
|                                  | 5-volt tolerant I/Os (FT, FTf)        | 25  | 42 in LQFP100<br>40 in WLCSP100 and UFBGA100 |             |     | 70               |     |
| DMA channels                     |                                       | 12  |  |             |     |                  |     |
| Capacitive sensing channels      |                                       | 18  | 24   |             |     |                  |     |
| 12-bit ADCs                      |                                       | 2<br>16 channels  | 2<br>17 channels                             |             |     | 2<br>18 channels |     |
| 12-bit DAC channels              |                                       | 1   |  |             |     |                  |     |
| Analog comparator                |                                       | 4   |  |             |     |                  |     |
| Operational amplifiers           |                                       | 2   |  |             |     |                  |     |
| CPU frequency                    |                                       | 72 MHz  |  |             |     |                  |     |
| Operating voltage                |                                       | 2.0 to 3.6 V  |  |             |     |                  |     |
| Operating temperature            |                                       | Ambient operating temperature: - 40 to 85 °C / - 40 to 105 °C<br>Junction temperature: - 40 to 125 °C |  |             |     |                  |     |
| Packages                         |                                       | LQFP64  | LQFP100<br>,WLCSP100<br>UFBGA100             |             |     | LQFP144          |     |

1. This total number considers also the PWMs generated on the complementary output channels.  
 2. The SPI interfaces works in an exclusive way in either the SPI mode or the I<sup>2</sup>S audio mode.

Figure 1. STM32F302xD/E block diagram



1. AF: alternate function on I/O pins.

## 3 Functional overview

### 3.1 ARM<sup>®</sup> Cortex<sup>®</sup>-M4 core with FPU with embedded Flash and SRAM

The ARM<sup>®</sup> Cortex<sup>®</sup>-M4 processor with FPU is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The ARM<sup>®</sup> Cortex<sup>®</sup>-M4 32-bit RISC processor with FPU features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The processor supports a set of DSP instructions which allows efficient signal processing and complex algorithm execution.

Its single precision FPU speeds up software development by using metalanguage development tools, while avoiding saturation.

With its embedded ARM core, the STM32F302xD/E family is compatible with all ARM tools and software.

*Figure 1* shows the general block diagram of the STM32F302xD/E family devices.

### 3.2 Memory protection unit (MPU)

The memory protection unit (MPU) is used to separate the processing of tasks from the data protection. The MPU manage up to 8 protection areas that are further divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The memory protection unit is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS detects it and takes action. In an RTOS environment, the kernel dynamically updates the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

### 3.3 Embedded Flash memory

All STM32F302xD/E devices feature 384/512 Kbyte of embedded Flash memory available for storing programs and data. The Flash memory access time is adjusted to the CPU clock frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states above).

### 3.4 Embedded SRAM

STM32F302xD/E devices feature 64 Kbyte of embedded SRAM with hardware parity check implemented on the first 32 Kbyte. The memory can be accessed in read/write at CPU clock speed with 0 wait states.

### 3.5 Boot modes

At startup, Boot0 pin and Boot1 option bit are used to select one of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

The boot loader is located in the system memory. It is used to reprogram the Flash memory by using USART1 (PA9/PA10), USART2 (PA2/PA3) or USB (PA11/PA12) through DFU (device firmware upgrade).

### 3.6 Cyclic redundancy check (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at linktime and stored at a given memory location.



## 3.7 Power management

### 3.7.1 Power supply schemes

- $V_{SS}, V_{DD} = 2.0$  to  $3.6$  V: external power supply for I/Os and the internal regulator. It is provided externally through  $V_{DD}$  pins.
- $V_{SSA}, V_{DDA} = 2.0$  to  $3.6$  V: external analog power supply for ADC, DAC, comparators, operational amplifier, reset blocks, RCs and PLL. The minimum voltage to be applied to  $V_{DDA}$  differs from one analog peripheral to another. [Table 3](#) provides the summary of the  $V_{DDA}$  ranges for analog peripherals. The  $V_{DDA}$  voltage level must always be greater than or equal to the  $V_{DD}$  voltage level and must be provided first.

**Table 3. External analog supply values for analog peripherals**

| Analog peripheral | Minimum $V_{DDA}$ supply | Maximum $V_{DDA}$ supply |
|-------------------|--------------------------|--------------------------|
| ADC/COMP          | 2.0 V                    | 3.6 V                    |
| DAC/OPAMP         | 2.4 V                    | 3.6 V                    |

- $V_{BAT} = 1.65$  to  $3.6$  V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when  $V_{DD}$  is not present.

### 3.7.2 Power supply supervisor

The device has an integrated power-on reset (POR) and power-down reset (PDR) circuits. They are always active, and ensure proper operation above a threshold of 2 V. The device remains in reset mode when the monitored supply voltage is below a specified threshold,  $V_{POR/PDR}$ , without the need for an external reset circuit.

- The POR monitors only the  $V_{DD}$  supply voltage. During the startup phase it is required that  $V_{DDA}$  should arrive first and be greater than or equal to  $V_{DD}$ .
- The PDR monitors both the  $V_{DD}$  and  $V_{DDA}$  supply voltages, however the  $V_{DDA}$  power supply supervisor can be disabled (by programming a dedicated Option bit) to reduce the power consumption if the application design ensures that  $V_{DDA}$  is higher than or equal to  $V_{DD}$ .

The device features an embedded programmable voltage detector (PVD) that monitors the  $V_{DD}$  power supply and compares it to the  $V_{PVD}$  threshold. An interrupt can be generated when  $V_{DD}$  drops below the  $V_{PVD}$  threshold and/or when  $V_{DD}$  is higher than the  $V_{PVD}$  threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

### 3.7.3 Voltage regulator

The regulator has three operation modes: main (MR), low power (LPR), and power-down.

- The MR mode is used in the nominal regulation mode (Run)
- The LPR mode is used in Stop mode.
- The power-down mode is used in Standby mode: the regulator output is in high impedance, and the kernel circuitry is powered down thus inducing zero consumption.

The voltage regulator is always enabled after reset. It is disabled in Standby mode.

### 3.7.4 Low-power modes

The STM32F302xD/E supports three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- Sleep mode  
In Sleep mode, only the CPU is stopped. All peripherals continue to operate and wake up the CPU when an interrupt/event occurs.
- Stop mode  
Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low-power mode.  
The device can be woken up from Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the PVD output, the USB wakeup, the RTC alarm, COMPx, I2Cx or U(S)ARTx.
- Standby mode  
The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the Backup domain and Standby circuitry.  
The device exits Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pin or an RTC alarm occurs.

*Note: The RTC, the IWDG and the corresponding clock sources are not stopped by entering Stop or Standby mode.*

### 3.8 Interconnect matrix

Several peripherals have direct connections between them. This allows autonomous communication between peripherals, saving CPU resources thus power supply consumption. In addition, these hardware connections allow fast and predictable latency.

**Table 4. STM32F302xD/E peripheral interconnect matrix**

| Interconnect source | Interconnect destination | Interconnect action                         |
|---------------------|--------------------------|---|
| TIMx                | TIMx                     | Timers synchronization or chaining          |
|                     | ADCx<br>DAC1             | Conversion triggers                         |
|                     | DMA                      | Memory to memory transfer trigger           |
|                     | Comp <sub>x</sub>        | Comparator output blanking                  |
| COMPx               | TIMx                     | Timer input: OCREF_CLR input, input capture |
| ADCx                | TIMx                     | Timer triggered by analog watchdog          |

**Table 4. STM32F302xD/E peripheral interconnect matrix (continued)**

| Interconnect source                      | Interconnect destination | Interconnect action  |
|--|--------------------------|--|
| GPIO<br>RTCCLK<br>HSE/32<br>MC0          | TIM16                    | Clock source used as input channel for HSI and LSI calibration |
| CSS<br>CPU (hard fault)<br>COMPx<br>GPIO | TIM1<br>TIM15, 16, 17    | Timer break  |
| GPIO                                     | TIMx                     | External trigger, timer break                                  |
|  | ADCx<br>DAC1             | Conversion external trigger                                    |
| DAC1                                     | COMPx                    | Comparator inverting input                                     |

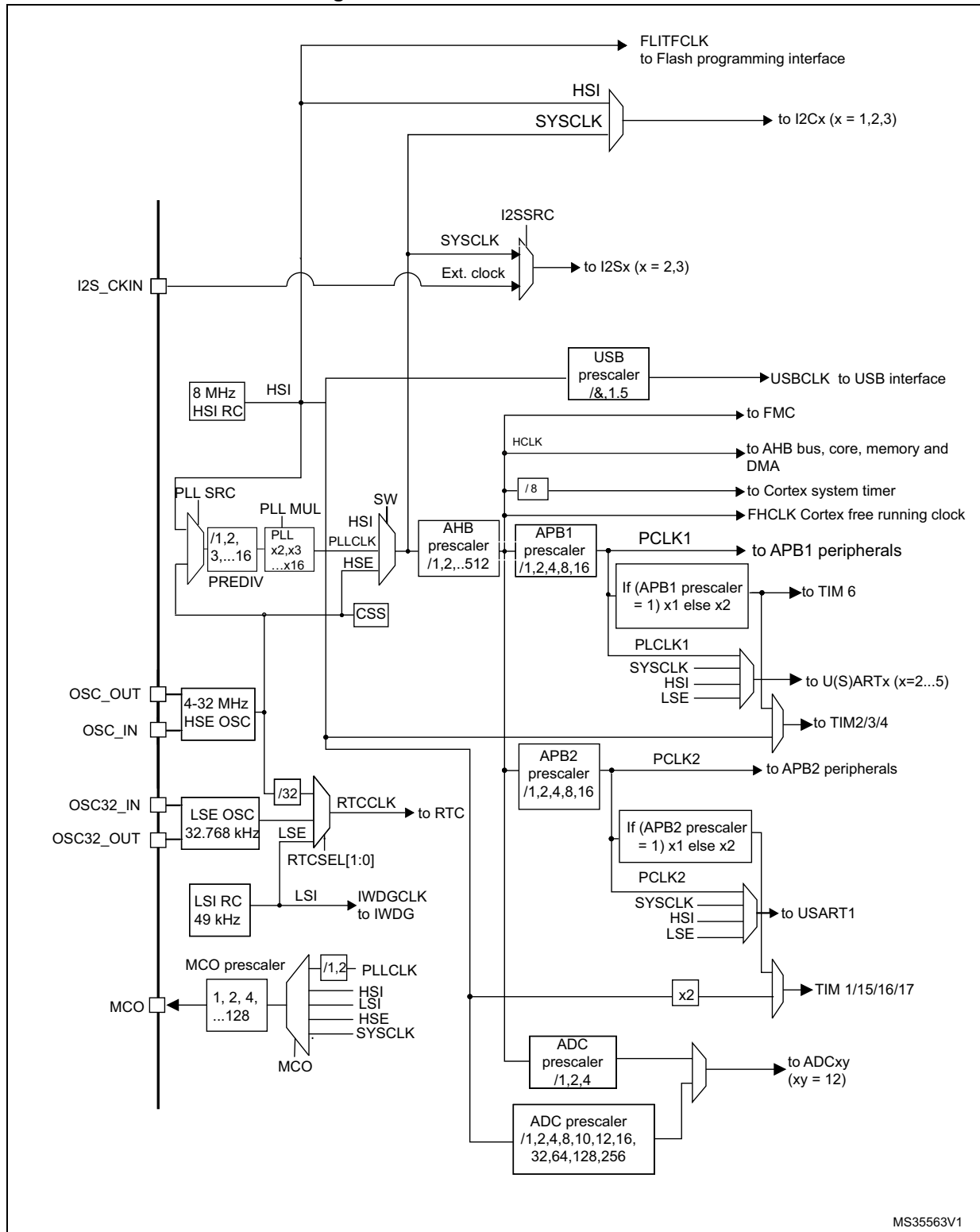
*Note:* For more details about the interconnect actions, refer to the corresponding sections in the STM32F302xD/E reference manual (RM0365).

### 3.9 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-32 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example with failure of an indirectly used external oscillator).

Several prescalers allow to configure the AHB frequency, the high speed APB (APB2) and the low speed APB (APB1) domains. The maximum frequency of the AHB and the high speed APB domains is 72 MHz, while the maximum allowed frequency of the low speed APB domain is 36 MHz.

Figure 2. STM32F302xD/E clock tree



MS35563V1

### 3.10 General-purpose input/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current capable except for analog inputs.

The I/Os alternate function configuration can be locked if needed following a specific sequence to avoid spurious writing to the I/Os registers.

Fast I/O handling allows I/O toggling up to 36 MHz.

### 3.11 Direct memory access (DMA)

The flexible general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each of the 12 DMA channels is connected to dedicated hardware DMA requests, with software trigger support for each channel. Configuration is done by software and transfer sizes between source and destination are independent.

The DMA is used with the main peripherals: SPI, I<sup>2</sup>C, USART, general-purpose timers, DAC and ADC.

### 3.12 Flexible static memory controller (FSMC)

The flexible static memory controller (FSMC) includes two memory controllers:

- The NOR/PSRAM memory controller,
- The NAND/PC Card memory controller.

This memory controller is also named Flexible memory controller (FMC).

The main features of the FMC controller are the following:

- Interface with static-memory mapped devices including:
  - Static random access memory (SRAM),
  - NOR Flash memory/OneNAND Flash memory,
  - PSRAM (four memory banks),
  - NAND Flash memory with ECC hardware to check up to 8 Kbyte of data,
  - 16-bit PC Card compatible devices.
- 8-,16-bit data bus width,
- Independent Chip Select control for each memory bank,
- Independent configuration for each memory bank,
- Write FIFO,
- LCD parallel interface.

The FMC can be configured to interface seamlessly with most graphic LCD controllers. It supports the Intel 8080 and Motorola 6800 modes, and is flexible enough to adapt to specific LCD interfaces. This LCD parallel interface capability makes it easy to build cost

effective graphic applications using LCD modules with embedded controllers or high performance solutions using external controllers with dedicated acceleration.

## 3.13 Interrupts and events

### 3.13.1 Nested vectored interrupt controller (NVIC)

The STM32F302xD/E devices embed a nested vectored interrupt controller (NVIC) able to handle up to 73 maskable interrupt channels and 16 priority levels.

The NVIC benefits are the following:

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

The NVIC hardware block provides flexible interrupt management features with minimal interrupt latency.

## 3.14 Fast analog-to-digital converter (ADC)

Two fast analog-to-digital converters 5 MSPS, with selectable resolution between 12 and 6 bit, are embedded in the STM32F302xD/E family devices. The ADCs have up to 18 external channels. The ADCs can perform conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADCs have also internal channels: Temperature sensor connected to ADC1 channel 16, VBAT/2 connected to ADC1 channel 17, Voltage reference VREFINT connected to the 2 ADCs channel 18, VREFOPAMP1 connected to ADC1 channel 15, VREFOPAMP2 connected to ADC2 channel 17.

Additional logic functions embedded in the ADC interface allow:

- Simultaneous sample and hold
- Interleaved sample and hold
- Single-shunt phase current reading techniques.

The ADC can be served by the DMA controller.

Three analog watchdogs are available per ADC.

The analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers and the advanced-control timer (TIM1) can be internally connected to the ADC start trigger and injection trigger, respectively, to allow the application to synchronize A/D conversion and timers.

### 3.14.1 Temperature sensor

The temperature sensor (TS) generates a voltage  $V_{\text{SENSE}}$  that varies linearly with temperature.

The temperature sensor is internally connected to the ADC1\_IN16 input channel which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode.

### 3.14.2 Internal voltage reference ( $V_{\text{REFINT}}$ )

The internal voltage reference ( $V_{\text{REFINT}}$ ) provides a stable (bandgap) voltage output for the ADC and Comparators.  $V_{\text{REFINT}}$  is internally connected to the ADCx\_IN18, x=1...4 input channel. The precise voltage of  $V_{\text{REFINT}}$  is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode.

### 3.14.3 $V_{\text{BAT}}$ battery voltage monitoring

This embedded hardware feature allows the application to measure the  $V_{\text{BAT}}$  battery voltage using the internal ADC channel ADC1\_IN17. As the  $V_{\text{BAT}}$  voltage may be higher than  $V_{\text{DDA}}$ , and thus outside the ADC input range, the  $V_{\text{BAT}}$  pin is internally connected to a bridge divider by 2. As a consequence, the converted digital value is half the  $V_{\text{BAT}}$  voltage.

### 3.14.4 OPAMP reference voltage ( $V_{\text{REFOPAMP}}$ )

Every OPAMP reference voltage can be measured using a corresponding ADC internal channel:  $V_{\text{REFO}}$ ,  $V_{\text{REFOPAMP1}}$  connected to ADC1 channel 15,  $V_{\text{REFOPAMP2}}$  connected to ADC2 channel 17.

## 3.15 Digital-to-analog converter (DAC)

One 12-bit buffered DAC channel can be used to convert digital signals into analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in inverting configuration.

This digital interface supports the following features:

- One DAC output channel
- 8-bit or 10-bit monotonic output
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation
- Triangular-wave generation
- DMA capability (for each channel)

- External triggers for conversion
- Input voltage reference VREF+

### 3.16 Operational amplifier (OPAMP)

The STM32F302xD/E embed two operational amplifiers (OPAMP1 and OPAMP2) with external or internal follower routing and PGA capability (or even amplifier and filter capability with external components). When an operational amplifier is selected, an external ADC channel is used to enable output measurement.

The operational amplifier features:

- 8.2 MHz bandwidth
- 0.5 mA output capability
- Rail-to-rail input/output
- In PGA mode, the gain is programmed to be 2, 4, 8 or 16.

### 3.17 Ultra-fast comparators (COMP)

The STM32F302xD/E devices embed four ultra-fast rail-to-rail comparators (COMP1, 2, 4, 6) with programmable reference voltage (internal or external) and selectable output polarity.

The reference voltage can be one of the following:

- External I/O
- DAC output pin
- Internal reference voltage or submultiple (1/4, 1/2, 3/4). Refer to [Table 23: Embedded internal reference voltage](#) for the value and precision of the internal reference voltage.

All comparators can wake up from STOP mode, generate interrupts and breaks for the timers.

### 3.18 Timers and watchdogs

The STM32F302xD/E include one advanced control timer, up to six general-purpose timers, one basic timer, two watchdog timers and one SysTick timer. The table below compares the features of the advanced control, general purpose and basic timers.

Table 5. Timer feature comparison

| Timer type      | Timer | Counter resolution | Counter type      | Prescaler factor                | DMA request generation | Capture/compare channels | Complementary outputs |
|-----------------|-------|--------------------|-------------------|---------------------------------|------------------------|--------------------------|-----------------------|
| Advanced        | TIM1  | 16-bit             | Up, Down, Up/Down | Any integer between 1 and 65536 | Yes                    | 4                        | Yes                   |
| General-purpose | TIM2  | 32-bit             | Up, Down, Up/Down | Any integer between 1 and 65536 | Yes                    | 4                        | No                    |



**Table 5. Timer feature comparison (continued)**

| Timer type      | Timer        | Counter resolution | Counter type      | Prescaler factor                | DMA request generation | Capture/compare channels | Complementary outputs |
|-----------------|--------------|--------------------|-------------------|---------------------------------|------------------------|--------------------------|-----------------------|
| General-purpose | TIM3, TIM4   | 16-bit             | Up, Down, Up/Down | Any integer between 1 and 65536 | Yes                    | 4                        | No                    |
| General-purpose | TIM15        | 16-bit             | Up                | Any integer between 1 and 65536 | Yes                    | 2                        | 1                     |
| General-purpose | TIM16, TIM17 | 16-bit             | Up                | Any integer between 1 and 65536 | Yes                    | 1                        | 1                     |
| Basic           | TIM6         | 16-bit             | Up                | Any integer between 1 and 65536 | Yes                    | 0                        | No                    |

*Note:* TIM1/2/3/4/15/16/17 can have PLL as clock source, and therefore can be clocked at 144 MHz.

### 3.18.1 Advanced timers (TIM1)

The advanced-control timer (TIM1) can be seen as a three-phase PWM multiplexed on six channels. It has complementary PWM outputs with programmable inserted dead-times. It can also be seen as a complete general-purpose timer. The four independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes) with full modulation capability (0-100%)
- One-pulse mode output

In debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled to turn off any power switches driven by these outputs.

Many features are shared with those of the general-purpose TIM timer (described in [Section 3.18.2](#)) using the same architecture, so the advanced-control timers can work together with the TIM timers via the Timer Link feature for synchronization or event chaining.

### 3.18.2 General-purpose timers (TIM2, TIM3, TIM4, TIM15, TIM16, TIM17)

There are up to six synchronizable general-purpose timers embedded in the STM32F302xD/E (see [Table 5](#) for differences). Each general-purpose timer can be used to generate PWM outputs, or act as a simple time base.

- TIM2, 3, and TIM4  
These are full-featured general-purpose timers:
  - TIM2 has a 32-bit auto-reload up/downcounter and 32-bit prescaler
  - TIM3 and 4 have 16-bit auto-reload up/downcounters and 16-bit prescalers.These timers all feature 4 independent channels for input capture/output compare, PWM or one-pulse mode output. They can work together, or with the other general-purpose timers via the Timer Link feature for synchronization or event chaining. The counters can be frozen in debug mode.  
All have independent DMA request generation and support quadrature encoders.
- TIM15, 16 and 17  
These three timers general-purpose timers with mid-range features:  
They have 16-bit auto-reload upcounters and 16-bit prescalers.
  - TIM15 has 2 channels and 1 complementary channel
  - TIM16 and TIM17 have 1 channel and 1 complementary channelAll channels can be used for input capture/output compare, PWM or one-pulse mode output.  
The timers can work together via the Timer Link feature for synchronization or event chaining. The timers have independent DMA request generation.  
The counters can be frozen in debug mode.

### 3.18.3 Basic timers (TIM6)

This timer is mainly used for DAC trigger generation. It can also be used as a generic 16-bit time base.

### 3.18.4 Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

### 3.18.5 Window watchdog (WWDG)

The window watchdog is based on a 7-bit downcounter that can be set as free running. It is used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

### 3.18.6 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

## 3.19 Real-time clock (RTC) and backup registers

The RTC and the 16 backup registers are supplied through a switch that takes power from either the  $V_{DD}$  supply when present or the  $V_{BAT}$  pin. The backup registers are sixteen 32-bit registers used to store 64 bytes of user application data when  $V_{DD}$  power is not present.

They are not reset by a system or power reset, or when the device wakes up from Standby mode.

The RTC is an independent BCD timer/counter. It supports the following features:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.
- Automatic correction for 28, 29 (leap year), 30 and 31 days of the month.
- Two programmable alarms with wake up from Stop and Standby mode capability.
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Digital calibration circuit with 1 ppm resolution, to compensate for quartz crystal inaccuracy.
- Three anti-tamper detection pins with programmable filter. The MCU can be woken up from Stop and Standby modes on tamper event detection.
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event. The MCU can be woken up from Stop and Standby modes on timestamp event detection.
- 17-bit Auto-reload counter for periodic interrupt with wakeup from STOP/STANDBY capability.

The RTC clock sources can be:

- A 32.768 kHz external crystal
- A resonator or oscillator
- The internal low-power RC oscillator (typical frequency of 40 kHz)
- The high-speed external clock divided by 32.

## 3.20 Inter-integrated circuit interface (I<sup>2</sup>C)

Up to three I<sup>2</sup>C bus interfaces can operate in multimaster and slave modes. They can support standard (up to 100 kHz), fast (up to 400 kHz) and fast mode + (up to 1 MHz) modes.

All I<sup>2</sup>C bus interfaces support 7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (2 addresses, 1 with configurable mask). They also include programmable analog and digital noise filters.

**Table 6. Comparison of I<sup>2</sup>C analog and digital filters**

| -                                | Analog filter   | Digital filter   |
|----------------------------------|---|--|
| Pulse width of suppressed spikes | ≥ 50 ns   | Programmable length from 1 to 15 I <sup>2</sup> C peripheral clocks                |
| Benefits                         | Available in Stop mode                                | 1. Extra filtering capability vs. standard requirements.<br>2. Stable length       |
| Drawbacks                        | Variations depending on temperature, voltage, process | Wakeup from Stop on address match is not available when digital filter is enabled. |

In addition, they provide hardware support for SMBUS 2.0 and PMBUS 1.1: ARP capability, Host notify protocol, hardware CRC (PEC) generation/verification, timeouts verifications and ALERT protocol management. They also have a clock domain independent from the CPU clock, allowing the I2Cx (x=1,2,3) to wake up the MCU from Stop mode on address match.

The I<sup>2</sup>C interfaces can be served by the DMA controller.

Refer to [Table 7](#) for the features available in I2C1, I2C2 and I2C3.

**Table 7. STM32F302xD/E I<sup>2</sup>C implementation**

| I <sup>2</sup> C features <sup>(1)</sup>                    | I2C1 | I2C2 | I2C3 |
|---|------|------|------|
| 7-bit addressing mode                                       | X    | X    | X    |
| 10-bit addressing mode                                      | X    | X    | X    |
| Standard mode (up to 100 kbit/s)                            | X    | X    | X    |
| Fast mode (up to 400 kbit/s)                                | X    | X    | X    |
| Fast Mode Plus with 20mA output drive I/Os (up to 1 Mbit/s) | X    | X    | X    |
| Independent clock   | X    | X    | X    |
| SMBus   | X    | X    | X    |
| Wakeup from STOP  | X    | X    | X    |

1. X = supported.

### 3.21 Universal synchronous/asynchronous receiver transmitter (USART)

The STM32F302xD/E devices have three embedded universal synchronous/asynchronous receiver transmitters (USART1, USART2 and USART3).

The USART interfaces are able to communicate at speeds of up to 9 Mbit/s.

They provide hardware management of the CTS and RTS signals, they support IrDA SIR ENDEC, the multiprocessor communication mode, the single-wire half-duplex

communication mode and have LIN Master/Slave capability. The USART interfaces can be served by the DMA controller.

### 3.22 Universal asynchronous receiver transmitter (UART)

The STM32F302xD/E devices have 2 embedded universal asynchronous receiver transmitters (UART4, and UART5). The UART interfaces support IrDA SIR ENDEC, multiprocessor communication mode and single-wire half-duplex communication mode. The UART4 interface can be served by the DMA controller.

Refer to [Table 8](#) for the features available in all U(S)ART interfaces.

**Table 8. USART features**

| USART modes/features <sup>(1)</sup>         | USART1 | USART2 | USART3 | UART4 | UART5 |
|---|--------|--------|--------|-------|-------|
| Hardware flow control for modem             | X      | X      | X      | -     | -     |
| Continuous communication using DMA          | X      | X      | X      | X     | -     |
| Multiprocessor communication                | X      | X      | X      | X     | X     |
| Synchronous mode                            | X      | X      | X      | -     | -     |
| Smartcard mode                              | X      | X      | X      | -     | -     |
| Single-wire half-duplex communication       | X      | X      | X      | X     | X     |
| IrDA SIR ENDEC block                        | X      | X      | X      | X     | X     |
| LIN mode                                    | X      | X      | X      | X     | X     |
| Dual clock domain and wakeup from Stop mode | X      | X      | X      | X     | X     |
| Receiver timeout interrupt                  | X      | X      | X      | X     | X     |
| Modbus communication                        | X      | X      | X      | X     | X     |
| Auto baud rate detection                    | X      | X      | X      | -     | -     |
| Driver Enable                               | X      | X      | X      | -     | -     |

1. X = supported.

### 3.23 Serial peripheral interface (SPI)/Inter-integrated sound interfaces (I<sup>2</sup>S)

Up to four SPIs are able to communicate up to 18 Mbit/s in slave and master modes in full-duplex and half-duplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame size is configurable from 4 bits to 16 bits.

Two standard I<sup>2</sup>S interfaces (multiplexed with SPI2 and SPI3) supporting four different audio standards can operate as master or slave at half-duplex and full duplex communication modes. They can be configured to transfer 16 and 24 or 32 bits with 16-bit or 32-bit data resolution and synchronized by a specific signal. Audio sampling frequency from 8 kHz up to 192 kHz can be set by 8-bit programmable linear prescaler. When operating in master mode it can output a clock for an external audio component at 256 times the sampling frequency.

Refer to [Table 9](#) for the features available in SPI1, SPI2, SPI3 and SPI4.

Table 9. STM32F302xD/E SPI/I<sup>2</sup>S implementation

| SPI features <sup>(1)</sup> | SPI1 | SPI2 | SPI3 | SPI4 |
|-----------------------------|------|------|------|------|
| Hardware CRC calculation    | X    | X    | X    | X    |
| Rx/Tx FIFO                  | X    | X    | X    | X    |
| NSS pulse mode              | X    | X    | X    | X    |
| I <sup>2</sup> S mode       | -    | X    | X    | -    |
| TI mode                     | X    | X    | X    | X    |

1. X = supported.

### 3.24 Controller area network (CAN)

The CAN is compliant with specifications 2.0A and B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has three transmit mailboxes, two receive FIFOs with 3 stages and 14 scalable filter banks.

### 3.25 Universal serial bus (USB)

The STM32F302xD/E embeds a full-speed USB device peripheral compliant with the USB specification version 2.0. The USB interface implements a full-speed (12 Mbit/s) function interface with added support for USB 2.0 Link Power Management. It has software-configurable endpoint setting with packet memory up-to 1 Kbyte (256 bytes are used for CAN peripheral if enabled) and suspend/resume support.

The dedicated 48 MHz clock is generated from the internal main PLL (the clock source must use a HSE crystal oscillator).

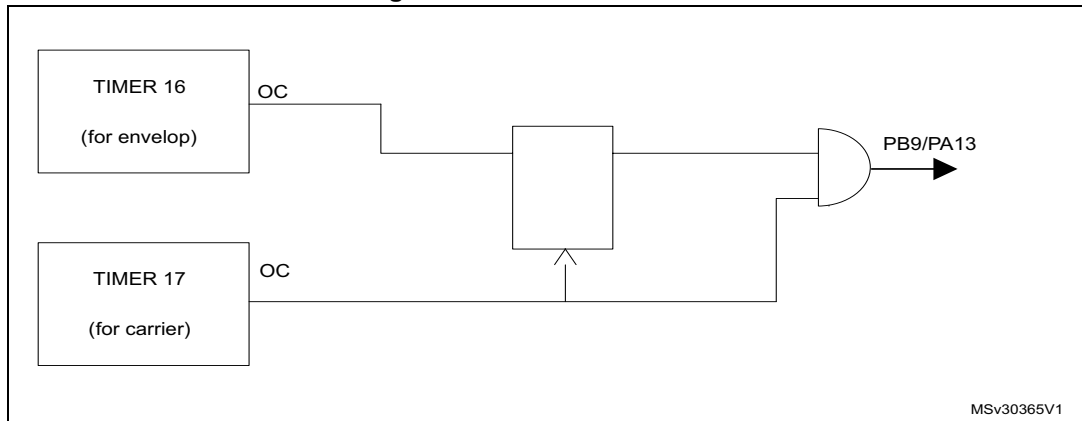
### 3.26 Infrared transmitter

The STM32F302xD/E devices provide an infrared transmitter solution. The solution is based on internal connections between TIM16 and TIM17 as shown in the figure below.

TIM17 is used to provide the carrier frequency and TIM16 provides the main signal to be sent. The infrared output signal is available on PB9 or PA13.

To generate the infrared remote control signals, TIM16 channel 1 and TIM17 channel 1 must be properly configured to generate correct waveforms. All standard IR pulse modulation modes can be obtained by programming the two timers output compare channels.

Figure 3. Infrared transmitter



### 3.27 Touch sensing controller (TSC)

The STM32F302xD/E devices provide a simple solution for adding capacitive sensing functionality to any application. These devices offer up to 24 capacitive sensing channels distributed over 8 analog I/O groups.

Capacitive sensing technology is able to detect the presence of a finger near a sensor which is protected from direct touch by a dielectric (glass, plastic, etc.). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle. It consists of charging the sensor capacitance and then transferring a part of the accumulated charges into a sampling capacitor until the voltage across this capacitor has reached a specific threshold. To limit the CPU bandwidth usage this acquisition is directly managed by the hardware touch sensing controller and only requires few external components to operate.

The touch sensing controller is fully supported by the STMTouch touch sensing firmware library which is free to use and allows touch sensing functionality to be implemented reliably in the end application.

Table 10. Capacitive sensing GPIOs available on STM32F302xD/E devices

| Group | Capacitive sensing signal name | Pin name | Group | Capacitive sensing signal name | Pin name |
|-------|--------------------------------|----------|-------|--------------------------------|----------|
| 1     | TSC_G1_IO1                     | PA0      | 5     | TSC_G5_IO1                     | PB3      |
|       | TSC_G1_IO2                     | PA1      |       | TSC_G5_IO2                     | PB4      |
|       | TSC_G1_IO3                     | PA2      |       | TSC_G5_IO3                     | PB6      |
|       | TSC_G1_IO4                     | PA3      |       | TSC_G5_IO4                     | PB7      |
| 2     | TSC_G2_IO1                     | PA4      | 6     | TSC_G6_IO1                     | PB11     |
|       | TSC_G2_IO2                     | PA5      |       | TSC_G6_IO2                     | PB12     |
|       | TSC_G2_IO3                     | PA6      |       | TSC_G6_IO3                     | PB13     |
|       | TSC_G2_IO4                     | PA7      |       | TSC_G6_IO4                     | PB14     |

**Table 10. Capacitive sensing GPIOs available on STM32F302xD/E devices (continued)**

| Group | Capacitive sensing signal name | Pin name | Group | Capacitive sensing signal name | Pin name |
|-------|--------------------------------|----------|-------|--------------------------------|----------|
| 3     | TSC_G3_IO1                     | PC5      | 7     | TSC_G7_IO1                     | PE2      |
|       | TSC_G3_IO2                     | PB0      |       | TSC_G7_IO2                     | PE3      |
|       | TSC_G3_IO3                     | PB1      |       | TSC_G7_IO3                     | PE4      |
|       | TSC_G3_IO4                     | PB2      |       | TSC_G7_IO4                     | PE5      |
| 4     | TSC_G4_IO1                     | PA9      | 8     | TSC_G8_IO1                     | PD12     |
|       | TSC_G4_IO2                     | PA10     |       | TSC_G8_IO2                     | PD13     |
|       | TSC_G4_IO3                     | PA13     |       | TSC_G8_IO3                     | PD14     |
|       | TSC_G4_IO4                     | PA14     |       | TSC_G8_IO4                     | PD15     |

**Table 11. Number of capacitive sensing channels available on STM32F302xD/E devices**

| Analog I/O group                      | Number of capacitive sensing channels |             |
|---------------------------------------|---------------------------------------|-------------|
|                                       | STM32F302VE/ZE                        | STM32F302RE |
| G1                                    | 3                                     | 3           |
| G2                                    | 3                                     | 3           |
| G3                                    | 3                                     | 3           |
| G4                                    | 3                                     | 3           |
| G5                                    | 3                                     | 3           |
| G6                                    | 3                                     | 3           |
| G7                                    | 3                                     | 0           |
| G8                                    | 3                                     | 0           |
| Number of capacitive sensing channels | 24                                    | 18          |

### 3.28 Development support

#### 3.28.1 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP Interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

The JTAG TMS and TCK pins are shared respectively with SWDIO and SWCLK and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

#### 3.28.2 Embedded Trace Macrocell

The ARM embedded trace macrocell (ETM™) provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32F302xD/E through a small number of ETM™ pins to an external hardware trace



port analyzer (TPA) device. The TPA is connected to a host computer using a high-speed channel. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer running debugger software. TPA hardware is commercially available from common development tool vendors. It operates with third party debugger software tools.

# 4 Pinout and pin description

Figure 4. STM32F302xD/E LQFP64 pinout

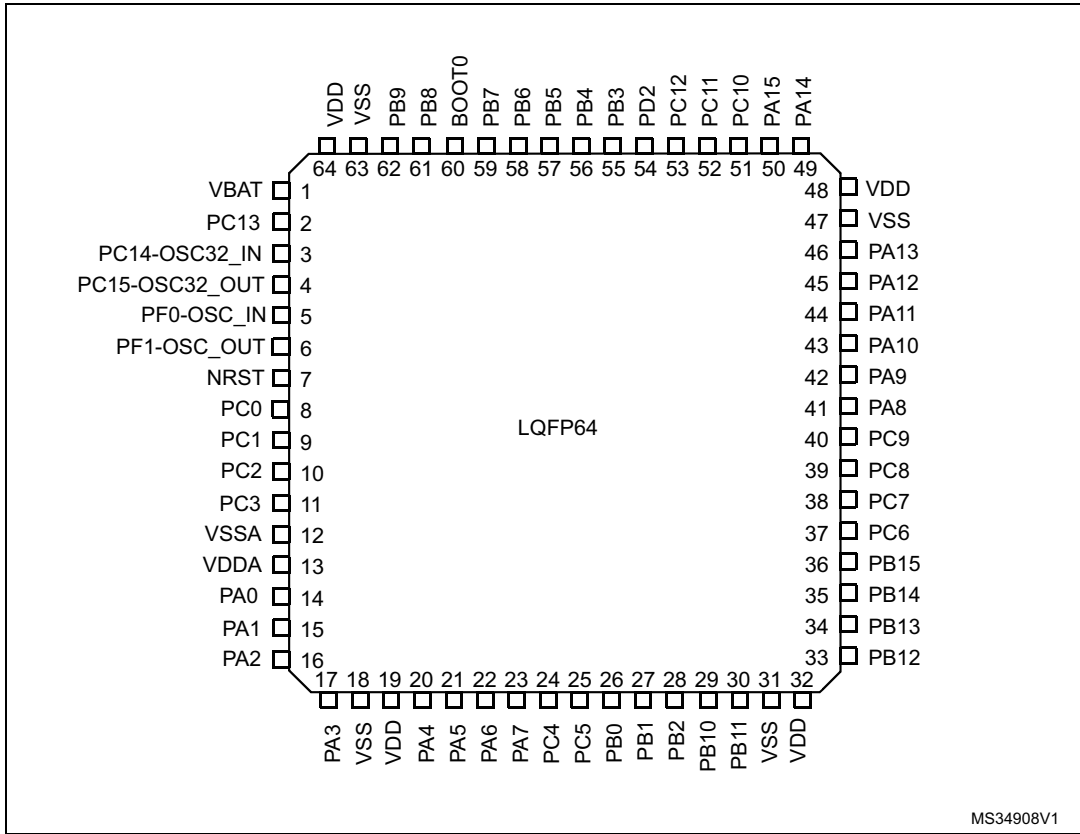
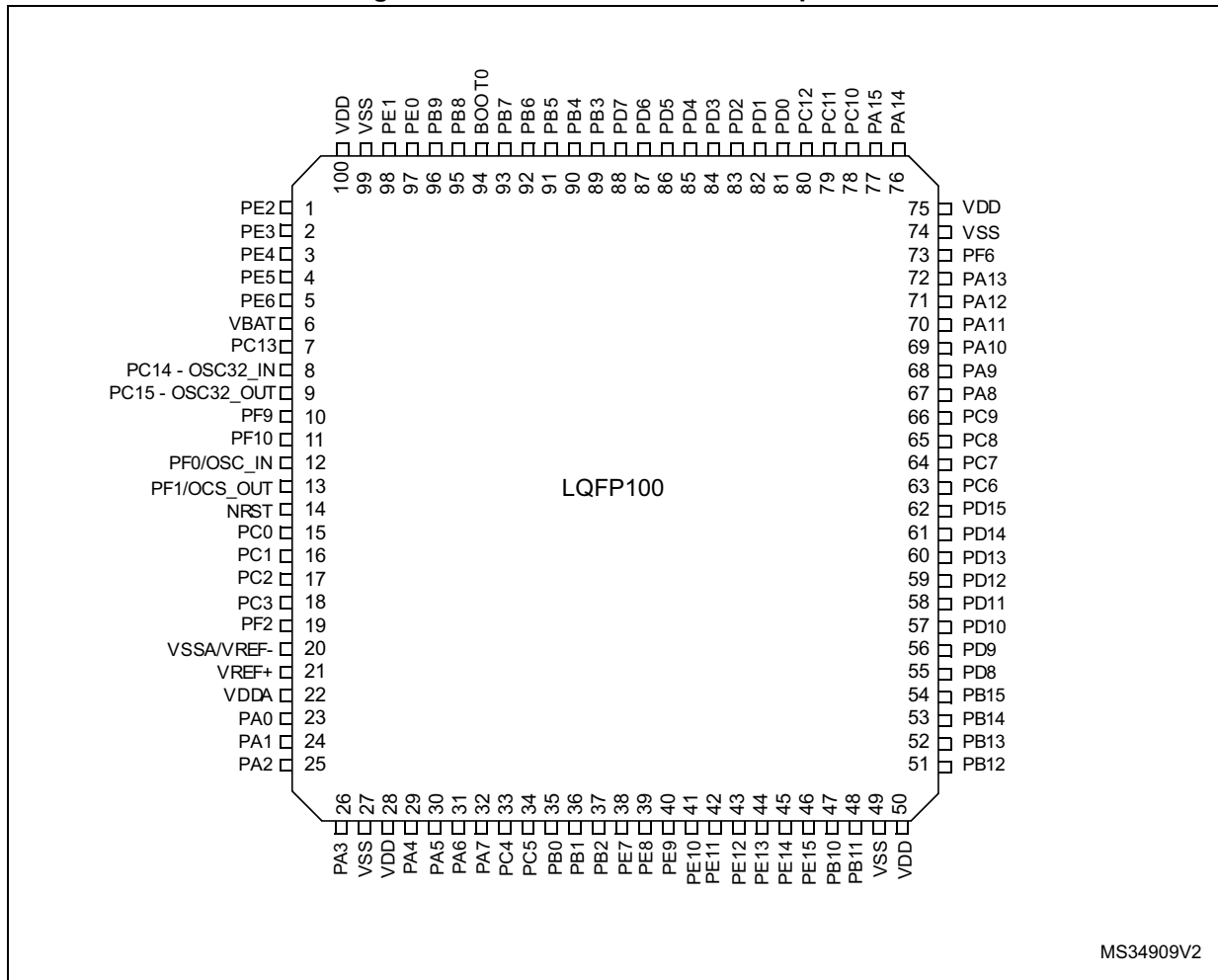
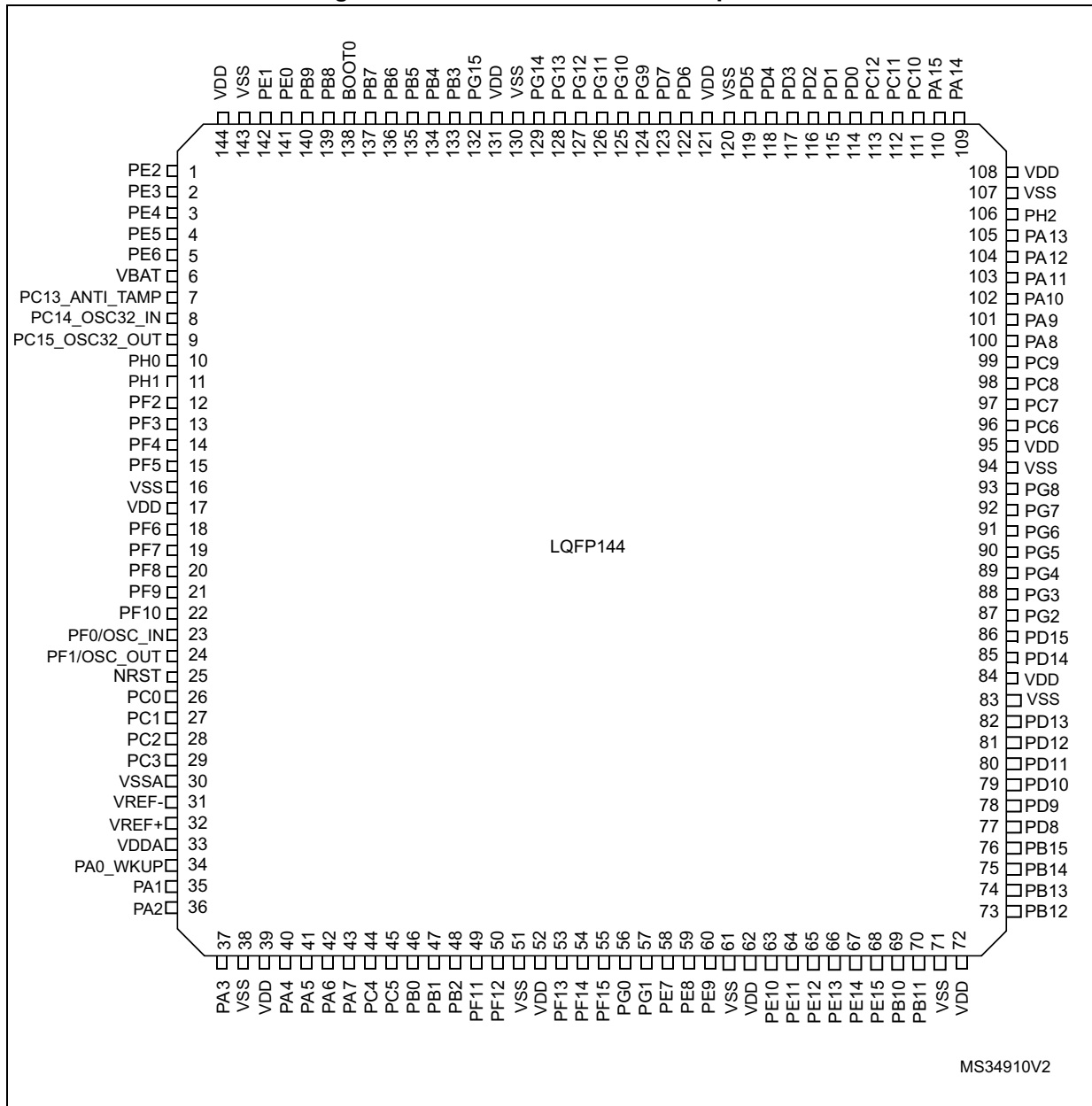


Figure 5. STM32F302xD/E LQFP100 pinout



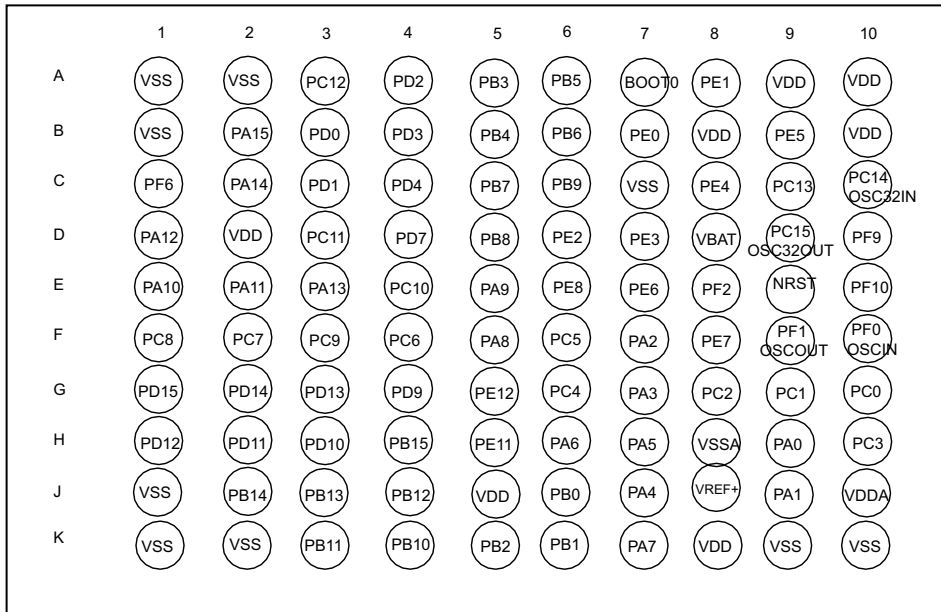
MS34909V2

Figure 6. STM32F302xD/E LQFP144 pinout



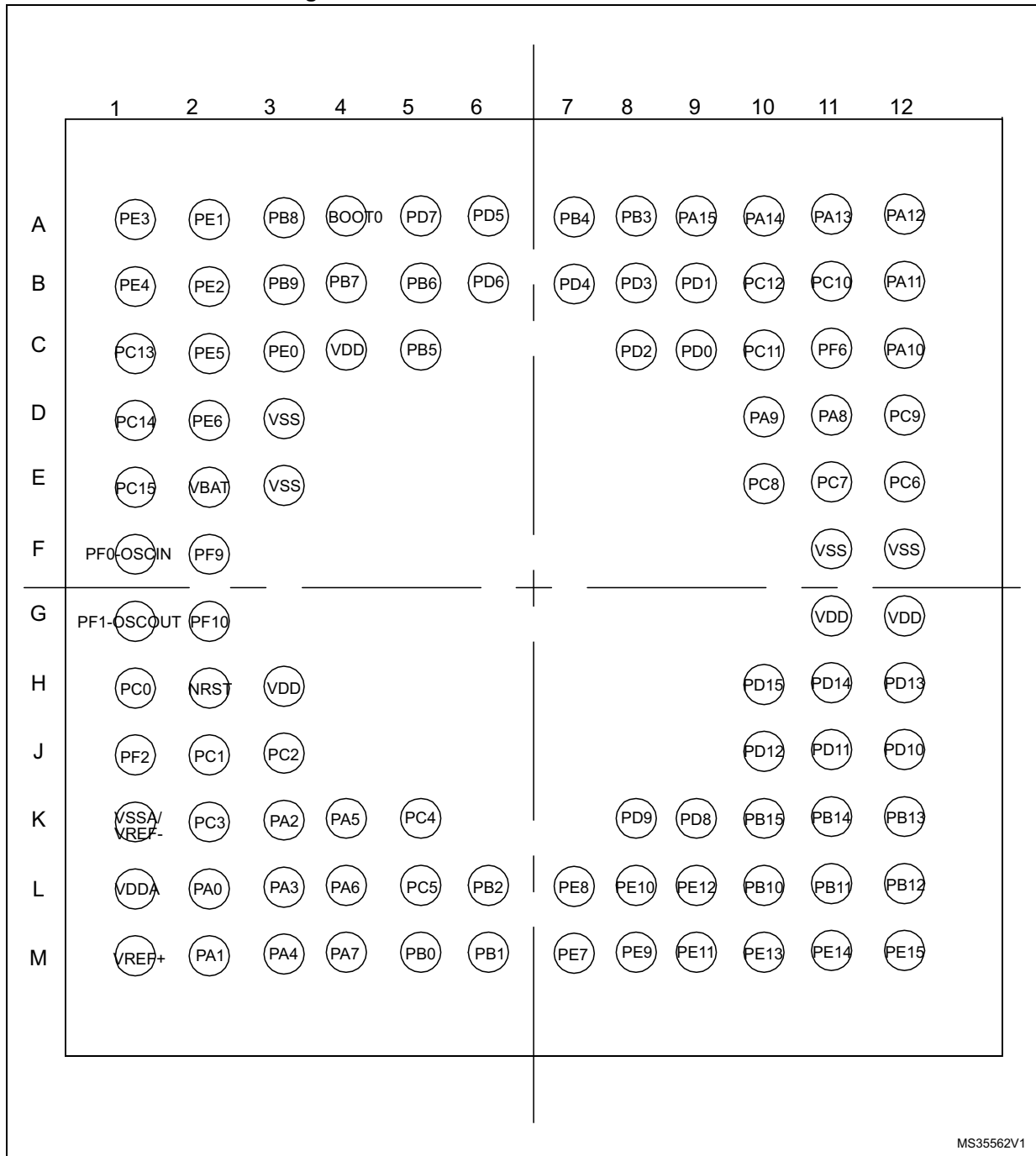
MS34910V2

Figure 7. STM32F302xD/E WLCSP100 ballout



MSv40453V1

Figure 8. STM32F302xD/E UFBGA100 ballout



MS35562V1

**Table 12. Legend/abbreviations used in the pinout table**

| Name          |                      | Abbreviation  | Definition   |
|---------------|----------------------|---|--|
| Pin name      |                      | Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name |  |
| I/O structure |                      | FT  | 5 V tolerant I/O   |
|               |                      | FTf   | 5 V tolerant I/O, I <sup>2</sup> C FM+ option                |
|               |                      | TTa   | 3.3 V tolerant I/O   |
|               |                      | TC  | Standard 3.3V I/O  |
|               |                      | B   | Dedicated to BOOT0 pin                                       |
|               |                      | RST   | Bi-directional reset pin with embedded weak pull-up resistor |
| Notes         |                      | Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset                                      |  |
| Pin functions | Alternate functions  | Functions selected through GPIOx_AFR registers  |  |
|               | Additional functions | Functions directly selected/enabled through peripheral registers  |  |

**Table 13. STM32F302xD/E pin definitions**

| Pin number |         |          |         | Pin name<br>(function after reset) | Pin type | I/O structure | Notes | Alternate functions   | Additional functions |
|------------|---------|----------|---------|------------------------------------|----------|---------------|-------|---|----------------------|
| LQFP64     | LQFP100 | WLCSP100 | LQFP144 |                                    |          |               |       |   |                      |
| -          | 1       | D6       | 1       | PE2                                | I/O      | FT            | (1)   | TRACECK, EVENTOUT, TIM3_CH1, TSC_G7_IO1, SPI4_SCK, FMC_A23  | -                    |
| -          | 2       | D7       | 2       | PE3                                | I/O      | FT            | (1)   | TRACED0, EVENTOUT, TIM3_CH2, TSC_G7_IO2, SPI4_NSS, FMC_A19  | -                    |
| -          | 3       | C8       | 3       | PE4                                | I/O      | FT            | (1)   | TRACED1, EVENTOUT, TIM3_CH3, TSC_G7_IO3, SPI4_NSS, FMC_A20  | -                    |
| -          | 4       | B9       | 4       | PE5                                | I/O      | FT            | (1)   | TRACED2, EVENTOUT, TIM3_CH4, TSC_G7_IO4, SPI4_MISO, FMC_A21 | -                    |
| -          | 5       | E7       | 5       | PE6                                | I/O      | FT            | (1)   | TRACED3, EVENTOUT, SPI4_MOSI, FMC_A22                       | WKUP3, RTC_TAMP3     |
| 1          | 6       | D8       | 6       | VBAT                               | S        | -             | -     | -   | -                    |



Table 13. STM32F302xD/E pin definitions (continued)

| Pin number |         |          |         | Pin name<br>(function<br>after reset) | Pin type | I/O structure | Notes | Alternate functions                                       | Additional functions                 |
|------------|---------|----------|---------|---------------------------------------|----------|---------------|-------|---|--------------------------------------|
| LQFP64     | LQFP100 | WLCSP100 | LQFP144 |                                       |          |               |       |   |                                      |
| 2          | 7       | C9       | 7       | PC13 <sup>(2)</sup>                   | I/O      | TC            | -     | EVENTOUT, TIM1_CH1N                                       | WKUP2, RTC_TAMP1,<br>RTC_TS, RTC_OUT |
| 3          | 8       | C10      | 8       | PC14 -<br>OSC32_IN <sup>(2)</sup>     | I/O      | TC            | -     | EVENTOUT  | OSC32_IN                             |
| 4          | 9       | D9       | 9       | PC15 -<br>OSC32_OUT <sup>(2)</sup>    | I/O      | TC            | -     | EVENTOUT  | OSC32_OUT                            |
| -          | -       | -        | 10      | PH0                                   | I/O      | FT            | (1)   | EVENTOUT, FMC_A0  | -                                    |
| -          | -       | -        | 11      | PH1                                   | I/O      | FT            | (1)   | EVENTOUT, FMC_A1  | -                                    |
| -          | 19      | E8       | 12      | PF2                                   | I/O      | TTa           | (1)   | EVENTOUT, FMC_A2  | ADC12_IN10                           |
| -          | -       | -        | 13      | PF3                                   | I/O      | FT            | (1)   | EVENTOUT, FMC_A3  | -                                    |
| -          | -       | -        | 14      | PF4                                   | I/O      | TTa           | (1)   | EVENTOUT, COMP1_OUT,<br>FMC_A4                            | ADC1_IN5 <sup>(3)</sup>              |
| -          | -       | -        | 15      | PF5                                   | I/O      | FT            | (1)   | EVENTOUT, FMC_A5  | -                                    |
| -          | -       | -        | 16      | VSS                                   | S        | -             | (1)   | -   | -                                    |
| -          | -       | -        | 17      | VDD                                   | S        | -             | (1)   | -   | -                                    |
| -          | 73      | C1       | 18      | PF6                                   | I/O      | FTf           | (1)   | EVENTOUT, TIM4_CH4,<br>I2C2_SCL, USART3_RTS,<br>FMC_NIORD | -                                    |
| -          | -       | -        | 19      | PF7                                   | I/O      | FT            | (1)   | EVENTOUT, FMC_NREG  | -                                    |
| -          | -       | -        | 20      | PF8                                   | I/O      | FT            | (1)   | EVENTOUT, FMC_NIOWR                                       | -                                    |
| -          | 10      | D10      | 21      | PF9                                   | I/O      | FT            | (1)   | EVENTOUT, TIM15_CH1,<br>SPI2_SCK, FMC_CD                  | -                                    |
| -          | 11      | E10      | 22      | PF10                                  | I/O      | FT            | (1)   | EVENTOUT, TIM15_CH2,<br>SPI2_SCK, FMC_INTR                | -                                    |
| 5          | 12      | F10      | 23      | PF0-OSC_IN                            | I        | FTf           | -     | EVENTOUT, I2C2_SDA,<br>SPI2_NSS/I2S2_WS,<br>TIM1_CH3N     | OSC_IN                               |
| 6          | 13      | F9       | 24      | PF1-<br>OSC_OUT                       | O        | FTf           | -     | EVENTOUT, I2C2_SCL,<br>SPI2_SCK/I2S2_CK                   | OSC_OUT                              |
| 7          | 14      | E9       | 25      | NRST                                  | I-O      | RST           | -     | Device reset input/internal reset output (active low)     |                                      |
| 8          | 15      | G10      | 26      | PC0                                   | I/O      | TTa           | -     | EVENTOUT, TIM1_CH1  | ADC12_IN6                            |



Table 13. STM32F302xD/E pin definitions (continued)

| Pin number |         |            |         | Pin name<br>(function<br>after reset) | Pin type | I/O structure | Notes | Alternate functions  | Additional functions   |
|------------|---------|------------|---------|---------------------------------------|----------|---------------|-------|--|--|
| LQFP64     | LQFP100 | WLCSP100   | LQFP144 |                                       |          |               |       |  |  |
| 9          | 16      | G9         | 27      | PC1                                   | I/O      | TTa           | -     | EVENTOUT, TIM1_CH2   | ADC12_IN7  |
| 10         | 17      | G8         | 28      | PC2                                   | I/O      | TTa           | -     | EVENTOUT, TIM1_CH3   | ADC12_IN8  |
| 11         | 18      | H10        | 29      | PC3                                   | I/O      | TTa           | -     | EVENTOUT, TIM1_CH4,<br>TIM1_BKIN2  | ADC12_IN9  |
| 12         | 20      | H8         | 30      | VSSA                                  | S        | -             | (1)   | -  | -  |
| -          | -       | -          | 31      | VREF-                                 | S        | -             | (1)   | -  | -  |
| -          | 21      | J8         | 32      | VREF+ <sup>(4)</sup>                  | S        | -             | -     | -  | -  |
| 13         | 22      | J10        | 33      | VDDA                                  | S        | -             | -     | -  | -  |
| 14         | 23      | H9         | 34      | PA0                                   | I/O      | TTa           | -     | TIM2_CH1/TIM2_ETR,<br>TSC_G1_IO1,<br>USART2_CTS,<br>COMP1_OUT, EVENTOUT        | ADC1_IN1 <sup>(3)</sup> , COMP1_INM,<br>RTC_TAMP2, WKUP1                                     |
| 15         | 24      | J9         | 35      | PA1                                   | I/O      | TTa           | -     | RTC_REFIN, TIM2_CH2,<br>TSC_G1_IO2,<br>USART2_RTS,<br>TIM15_CH1N, EVENTOUT     | ADC1_IN2 <sup>(3)</sup> , COMP1_INP,<br>OPAMP1_VINP  |
| 16         | 25      | F7         | 36      | PA2                                   | I/O      | TTa           | (5)   | TIM2_CH3, TSC_G1_IO3,<br>USART2_TX,<br>COMP2_OUT, TIM15_CH1,<br>EVENTOUT       | ADC1_IN3 <sup>(3)</sup> , COMP2_INM,<br>OPAMP1_VOUT  |
| 17         | 26      | G7         | 37      | PA3                                   | I/O      | TTa           | -     | TIM2_CH4, TSC_G1_IO4,<br>USART2_RX, TIM15_CH2,<br>EVENTOUT                     | ADC1_IN4 <sup>(3)</sup> ,<br>OPAMP1_VINM/<br>OPAMP1_VINP                                     |
| 18         | 27      | K9,<br>K10 | 38      | VSS                                   | S        | -             | -     | -  | -  |
| 19         | 28      | K8         | 39      | VDD                                   | S        | -             | (1)   | -  | -  |
| 20         | 29      | J7         | 40      | PA4                                   | I/O      | TTa           | (5)   | TIM3_CH2, TSC_G2_IO1,<br>SPI1_NSS,<br>SPI3_NSS/I2S3_WS,<br>USART2_CK, EVENTOUT | ADC2_IN1 <sup>(3)</sup> , DAC1_OUT1,<br>COMP1_INM,<br>COMP2_INM,<br>COMP4_INM,<br>COMP6_INM, |

Table 13. STM32F302xD/E pin definitions (continued)

| Pin number |         |          |         | Pin name<br>(function<br>after reset) | Pin type | I/O structure | Notes | Alternate functions   | Additional functions   |
|------------|---------|----------|---------|---------------------------------------|----------|---------------|-------|---|--|
| LQFP64     | LQFP100 | WLCSP100 | LQFP144 |                                       |          |               |       |   |  |
| 21         | 30      | H7       | 41      | PA5                                   | I/O      | TTa           | (5)   | TIM2_CH1/TIM2_ETR,<br>TSC_G2_IO2, SPI1_SCK,<br>EVENTOUT                             | ADC2_IN2 <sup>(3)</sup> , COMP1_INM,<br>COMP2_INM,<br>COMP4_INM,<br>COMP6_INM,<br>OPAMP1_VINP,<br>OPAMP2_VINM, |
| 22         | 31      | H6       | 42      | PA6                                   | I/O      | TTa           | (5)   | TIM16_CH1, TIM3_CH1,<br>TSC_G2_IO3, SPI1_MISO,<br>TIM1_BKIN, COMP1_OUT,<br>EVENTOUT | ADC2_IN3 <sup>(3)</sup> ,<br>OPAMP2_VOUT   |
| 23         | 32      | K7       | 43      | PA7                                   | I/O      | TTa           | -     | TIM17_CH1, TIM3_CH2,<br>TSC_G2_IO4, SPI1_MOSI,<br>TIM1_CH1N, EVENTOUT               | ADC2_IN4 <sup>(3)</sup> , COMP2_INP,<br>OPAMP1_VINP,<br>OPAMP2_VINP  |
| 24         | 33      | G6       | 44      | PC4                                   | I/O      | TTa           | -     | EVENTOUT, TIM1_ETR,<br>USART1_TX  | ADC2_IN5 <sup>(3)</sup>  |
| 25         | 34      | F6       | 45      | PC5                                   | I/O      | TTa           | -     | EVENTOUT, TIM15_BKIN,<br>TSC_G3_IO1, USART1_RX                                      | ADC2_IN11,<br>OPAMP1_VINM,<br>OPAMP2_VINM  |
| 26         | 35      | J6       | 46      | PB0                                   | I/O      | TTa           | -     | TIM3_CH3, TSC_G3_IO2,<br>TIM1_CH2N, EVENTOUT  | COMP4_INP,<br>OPAMP2_VINP,   |
| 27         | 36      | K6       | 47      | PB1                                   | I/O      | TTa           | (5)   | TIM3_CH4, TSC_G3_IO3,<br>TIM1_CH3N, COMP4_OUT,<br>EVENTOUT                          | -  |
| 28         | 37      | K5       | 48      | PB2                                   | I/O      | TTa           | -     | TSC_G3_IO4, EVENTOUT  | ADC2_IN12, COMP4_INM   |
| -          | -       | -        | 49      | PF11                                  | I/O      | FT            | (1)   | EVENTOUT  | -  |
| -          | -       | -        | 50      | PF12                                  | I/O      | FT            | (1)   | EVENTOUT, FMC_A6  | -  |
| -          | -       | -        | 51      | VSS                                   | S        | -             | -     | -   | -  |
| -          | -       | -        | 52      | VDD                                   | S        | -             | (1)   | -   | -  |
| -          | -       | -        | 53      | PF13                                  | I/O      | FT            | (1)   | EVENTOUT, FMC_A7  | -  |
| -          | -       | -        | 54      | PF14                                  | I/O      | FT            | (1)   | EVENTOUT, FMC_A8  | -  |
| -          | -       | -        | 55      | PF15                                  | I/O      | FT            | (1)   | EVENTOUT, FMC_A9  | -  |
| -          | -       | -        | 56      | PG0                                   | I/O      | FT            | (1)   | EVENTOUT, FMC_A10   | -  |
| -          | -       | -        | 57      | PG1                                   | I/O      | FT            | (1)   | EVENTOUT, FMC_A11   | -  |

Table 13. STM32F302xD/E pin definitions (continued)

| Pin number |         |                  |         | Pin name<br>(function<br>after reset) | Pin type | I/O structure | Notes | Alternate functions  | Additional functions  |
|------------|---------|------------------|---------|---------------------------------------|----------|---------------|-------|--|-----------------------|
| LQFP64     | LQFP100 | WLCSP100         | LQFP144 |                                       |          |               |       |  |                       |
| -          | 38      | F8               | 58      | PE7                                   | I/O      | TTa           | (1)   | EVENTOUT, TIM1_ETR,<br>FMC_D4  | -                     |
| -          | 39      | E6               | 59      | PE8                                   | I/O      | TTa           | (1)   | EVENTOUT, TIM1_CH1N,<br>FMC_D5   | COMP4_INM             |
| -          | 40      | -                | 60      | PE9                                   | I/O      | TTa           | (1)   | EVENTOUT, TIM1_CH1,<br>FMC_D6  | -                     |
| -          | -       | -                | 61      | VSS                                   | S        | -             | (1)   | -  | -                     |
| -          | -       | -                | 62      | VDD                                   | S        | -             | (1)   | -  | -                     |
| -          | 41      | -                | 63      | PE10                                  | I/O      | TTa           | (1)   | EVENTOUT, TIM1_CH2N,<br>FMC_D7   | -                     |
| -          | 42      | H5               | 64      | PE11                                  | I/O      | TTa           | (1)   | EVENTOUT, TIM1_CH2,<br>SPI4_NSS, FMC_D8  | -                     |
| -          | 43      | G5               | 65      | PE12                                  | I/O      | TTa           | (1)   | EVENTOUT, TIM1_CH3N,<br>SPI4_SCK, FMC_D9   | -                     |
| -          | 44      | -                | 66      | PE13                                  | I/O      | TTa           | (1)   | EVENTOUT, TIM1_CH3,<br>SPI4_MISO, FMC_D10  | -                     |
| -          | 45      | -                | 67      | PE14                                  | I/O      | TTa           | (1)   | EVENTOUT, TIM1_CH4,<br>SPI4_MOSI, TIM1_BKIN2,<br>FMC_D11                             | -                     |
| -          | 46      | -                | 68      | PE15                                  | I/O      | TTa           | (1)   | EVENTOUT, TIM1_BKIN,<br>USART3_RX, FMC_D12   | -                     |
| 29         | 47      | K4               | 69      | PB10                                  | I/O      | TTa           | -     | TIM2_CH3, TSC_SYNC,<br>USART3_TX, EVENTOUT   | -                     |
| 30         | 48      | K3               | 70      | PB11                                  | I/O      | TTa           | -     | TIM2_CH4, TSC_G6_IO1,<br>USART3_RX, EVENTOUT   | ADC12_IN14, COMP6_INP |
| 31         | 49      | K1,<br>J1,<br>K2 | 71      | VSS                                   | S        | -             | -     | -  | -                     |
| 32         | 50      | J5               | 72      | VDD                                   | S        | -             | -     | -  | -                     |
| 33         | 51      | J4               | 73      | PB12                                  | I/O      | TTa           | (5)   | TSC_G6_IO2,<br>I2C2_SMBAL,<br>SPI2_NSS/I2S2_WS,<br>TIM1_BKIN, USART3_CK,<br>EVENTOUT | -                     |

Table 13. STM32F302xD/E pin definitions (continued)

| Pin number |         |          |         | Pin name<br>(function<br>after reset) | Pin type | I/O structure | Notes | Alternate functions   | Additional functions |
|------------|---------|----------|---------|---------------------------------------|----------|---------------|-------|---|----------------------|
| LQFP64     | LQFP100 | WLCSP100 | LQFP144 |                                       |          |               |       |   |                      |
| 34         | 52      | J3       | 74      | PB13                                  | I/O      | TTa           | -     | TSC_G6_IO3,<br>SPI2_SCK/I2S2_CK,<br>TIM1_CH1N,<br>USART3_CTS, EVENTOUT                | -                    |
| 35         | 53      | J2       | 75      | PB14                                  | I/O      | TTa           | -     | TIM15_CH1, TSC_G6_IO4,<br>SPI2_MISO/I2S2ext_SD,<br>TIM1_CH2N,<br>USART3_RTS, EVENTOUT | OPAMP2_VINP          |
| 36         | 54      | H4       | 76      | PB15                                  | I/O      | TTa           | -     | RTC_REFIN, TIM15_CH2,<br>TIM15_CH1N, TIM1_CH3N,<br>SPI2_MOSI/I2S2_SD,<br>EVENTOUT     | COMP6_INM            |
| -          | 55      | -        | 77      | PD8                                   | I/O      | TTa           | (1)   | EVENTOUT, USART3_TX,<br>FMC_D13   | -                    |
| -          | 56      | G4       | 78      | PD9                                   | I/O      | TTa           | (1)   | EVENTOUT, USART3_RX,<br>FMC_D14   | -                    |
| -          | 57      | H3       | 79      | PD10                                  | I/O      | TTa           | (1)   | EVENTOUT, USART3_CK,<br>FMC_D15   | COMP6_INM            |
| -          | 58      | H2       | 80      | PD11                                  | I/O      | TTa           | (1)   | EVENTOUT,<br>USART3_CTS, FMC_A16  | -                    |
| -          | 59      | H1       | 81      | PD12                                  | I/O      | TTa           | (1)   | EVENTOUT, TIM4_CH1,<br>TSC_G8_IO1,<br>USART3_RTS, FMC_A17                             | -                    |
| -          | 60      | G3       | 82      | PD13                                  | I/O      | TTa           | (1)   | EVENTOUT, TIM4_CH2,<br>TSC_G8_IO2, FMC_A18  | -                    |
| -          | -       | -        | 83      | VSS                                   | S        | -             | (1)   | -   | -                    |
| -          | -       | -        | 84      | VDD                                   | S        | -             | (1)   | -   | -                    |
| -          | 61      | G2       | 85      | PD14                                  | I/O      | TTa           | (1)   | EVENTOUT, TIM4_CH3,<br>TSC_G8_IO3, FMC_D0   | OPAMP2_VINP          |
| -          | 62      | G1       | 86      | PD15                                  | I/O      | TTa           | (1)   | EVENTOUT, TIM4_CH4,<br>TSC_G8_IO4, SPI2_NSS,<br>FMC_D1                                | -                    |
| -          | -       | -        | 87      | PG2                                   | I/O      | FT            | (1)   | EVENTOUT, FMC_A12   | -                    |
| -          | -       | -        | 88      | PG3                                   | I/O      | FT            | (1)   | EVENTOUT, FMC_A13   | -                    |
| -          | -       | -        | 89      | PG4                                   | I/O      | FT            | (1)   | EVENTOUT, FMC_A14   | -                    |

Table 13. STM32F302xD/E pin definitions (continued)

| Pin number |         |          |         | Pin name<br>(function<br>after reset) | Pin type | I/O structure | Notes | Alternate functions   | Additional functions |
|------------|---------|----------|---------|---------------------------------------|----------|---------------|-------|---|----------------------|
| LQFP64     | LQFP100 | WLCSP100 | LQFP144 |                                       |          |               |       |   |                      |
| -          | -       | -        | 90      | PG5                                   | I/O      | FT            | (1)   | EVENTOUT, FMC_A15   | -                    |
| -          | -       | -        | 91      | PG6                                   | I/O      | FT            | (1)   | EVENTOUT, FMC_INT2  | -                    |
| -          | -       | -        | 92      | PG7                                   | I/O      | FT            | (1)   | EVENTOUT, FMC_INT3  | -                    |
| -          | -       | -        | 93      | PG8                                   | I/O      | FT            | (1)   | EVENTOUT  | -                    |
| -          | -       | -        | 94      | VSS                                   | S        | -             | (1)   | -   | -                    |
| -          | -       | -        | 95      | VDD                                   | S        | -             | (1)   | -   | -                    |
| 37         | 63      | F4       | 96      | PC6                                   | I/O      | FT            | -     | EVENTOUT, TIM3_CH1,<br>I2S2_MCK, COMP6_OUT  | -                    |
| 38         | 64      | F2       | 97      | PC7                                   | I/O      | FT            | -     | EVENTOUT, TIM3_CH2,<br>I2S3_MCK   | -                    |
| 39         | 65      | F1       | 98      | PC8                                   | I/O      | FT            | -     | EVENTOUT, TIM3_CH3  | -                    |
| 40         | 66      | F3       | 99      | PC9                                   | I/O      | FTf           | -     | EVENTOUT, TIM3_CH4,<br>I2C3_SDA, I2SCKIN  | -                    |
| 41         | 67      | F5       | 100     | PA8                                   | I/O      | FTf           | -     | MCO, I2C3_SCL,<br>I2C2_SMBAL, I2S2_MCK,<br>TIM1_CH1, USART1_CK,<br>TIM4_ETR, EVENTOUT                                     | -                    |
| 42         | 68      | E5       | 101     | PA9                                   | I/O      | FTf           | -     | I2C3_SMBAL,<br>TSC_G4_IO1, I2C2_SCL,<br>I2S3_MCK, TIM1_CH2,<br>USART1_TX, TIM15_BKIN,<br>TIM2_CH3, EVENTOUT               | -                    |
| 43         | 69      | E1       | 102     | PA10                                  | I/O      | FTf           | -     | TIM17_BKIN,<br>TSC_G4_IO2, I2C2_SDA,<br>SPI2_MISO/I2S2ext_SD,<br>TIM1_CH3, USART1_RX,<br>COMP6_OUT, TIM2_CH4,<br>EVENTOUT | -                    |
| 44         | 70      | E2       | 103     | PA11                                  | I/O      | FT            | -     | SPI2_MOSI/I2S2_SD,<br>TIM1_CH1N,<br>USART1_CTS,<br>COMP1_OUT, CAN_RX,<br>TIM4_CH1, TIM1_CH4,<br>TIM1_BKIN2, EVENTOUT      | USB_DM               |

Table 13. STM32F302xD/E pin definitions (continued)

| Pin number |         |                  |         | Pin name<br>(function<br>after reset) | Pin type | I/O structure | Notes | Alternate functions   | Additional functions |
|------------|---------|------------------|---------|---------------------------------------|----------|---------------|-------|---|----------------------|
| LQFP64     | LQFP100 | WLCSP100         | LQFP144 |                                       |          |               |       |   |                      |
| 45         | 71      | D1               | 104     | PA12                                  | I/O      | FT            | -     | TIM16_CH1, I2SCKIN,<br>TIM1_CH2N,<br>USART1_RTS,<br>COMP2_OUT, CAN_TX,<br>TIM4_CH2, TIM1_ETR,<br>EVENTOUT                 | USB_DP               |
| 46         | 72      | E3               | 105     | PA13                                  | I/O      | FT            | -     | SWDIO-JTMS,<br>TIM16_CH1N,<br>TSC_G4_IO3, IR-OUT,<br>USART3_CTS, TIM4_CH3,<br>EVENTOUT                                    | -                    |
| -          | -       | -                | 106     | PH2                                   | I/O      | FT            | (1)   | EVENTOUT  | -                    |
| 47         | 74      | A1,<br>A2,<br>B1 | 107     | VSS                                   | S        | -             | -     | -   | -                    |
| 48         | 75      | D2               | 108     | VDD                                   | S        | -             | -     | -   | -                    |
| 49         | 76      | C2               | 109     | PA14                                  | I/O      | FTf           | -     | SWCLK-JTCK,<br>TSC_G4_IO4, I2C1_SDA,<br>TIM1_BKIN, USART2_TX,<br>EVENTOUT   | -                    |
| 50         | 77      | B2               | 110     | PA15                                  | I/O      | FTf           | -     | JTDI,<br>TIM2_CH1/TIM2_ETR,<br>TSC_SYNC, I2C1_SCL,<br>SPI1_NSS,<br>SPI3_NSS/I2S3_WS,<br>USART2_RX, TIM1_BKIN,<br>EVENTOUT | -                    |
| 51         | 78      | E4               | 111     | PC10                                  | I/O      | FT            | -     | EVENTOUT, UART4_TX,<br>SPI3_SCK/I2S3_CK,<br>USART3_TX   | -                    |
| 52         | 79      | D3               | 112     | PC11                                  | I/O      | FT            | -     | EVENTOUT, UART4_RX,<br>SPI3_MISO/I2S3ext_SD,<br>USART3_RX   | -                    |
| 53         | 80      | A3               | 113     | PC12                                  | I/O      | FT            | -     | EVENTOUT, UART5_TX,<br>SPI3_MOSI/I2S3_SD,<br>USART3_CK  | -                    |
| -          | 81      | B3               | 114     | PD0                                   | I/O      | FT            | (1)   | EVENTOUT, CAN_RX,<br>FMC_D2   | -                    |

Table 13. STM32F302xD/E pin definitions (continued)

| Pin number |         |          |         | Pin name<br>(function<br>after reset) | Pin type | I/O structure | Notes | Alternate functions                                    | Additional functions |
|------------|---------|----------|---------|---------------------------------------|----------|---------------|-------|--|----------------------|
| LQFP64     | LQFP100 | WLCSP100 | LQFP144 |                                       |          |               |       |  |                      |
| -          | 82      | C3       | 115     | PD1                                   | I/O      | FT            | (1)   | EVENTOUT, CAN_TX,<br>FMC_D3                            | -                    |
| 54         | 83      | A4       | 116     | PD2                                   | I/O      | FT            | -     | EVENTOUT, TIM3_ETR,<br>UART5_RX                        | -                    |
| -          | 84      | B4       | 117     | PD3                                   | I/O      | FT            | (1)   | EVENTOUT,<br>TIM2_CH1/TIM2_ETR,<br>USART2_CTS, FMC_CLK | -                    |
| -          | 85      | C4       | 118     | PD4                                   | I/O      | FT            | (1)   | EVENTOUT, TIM2_CH2,<br>USART2_RTS, FMC_NOE             | -                    |
| -          | 86      | -        | 119     | PD5                                   | I/O      | FT            | (1)   | EVENTOUT, USART2_TX,<br>FMC_NWE                        | -                    |
| -          | -       | -        | 120     | VSS                                   | S        | -             | (1)   | -  | -                    |
| -          | -       | -        | 121     | VDD                                   | S        | -             | (1)   | -  | -                    |
| -          | 87      | -        | 122     | PD6                                   | I/O      | FT            | (1)   | EVENTOUT, TIM2_CH4,<br>USART2_RX, FMC_NWAIT            | -                    |
| -          | 88      | D4       | 123     | PD7                                   | I/O      | FT            | (1)   | EVENTOUT, TIM2_CH3,<br>USART2_CK,<br>FMC_NE1/FMC_NCE2  | -                    |
| -          | -       | -        | 124     | PG9                                   | I/O      | FT            | (1)   | EVENTOUT,<br>FMC_NE2/FMC_NCE3                          | -                    |
| -          | -       | -        | 125     | PG10                                  | I/O      | FT            | (1)   | EVENTOUT,<br>FMC_NCE4_1/FMC_NE3                        | -                    |
| -          | -       | -        | 126     | PG11                                  | I/O      | FT            | (1)   | EVENTOUT, FMC_NCE4_2                                   | -                    |
| -          | -       | -        | 127     | PG12                                  | I/O      | FT            | (1)   | EVENTOUT, FMC_NE4                                      | -                    |
| -          | -       | -        | 128     | PG13                                  | I/O      | FT            | (1)   | EVENTOUT, FMC_A24                                      | -                    |
| -          | -       | -        | 129     | PG14                                  | I/O      | FT            | (1)   | EVENTOUT, FMC_A25                                      | -                    |
| -          | -       | -        | 130     | VSS                                   | S        | -             | (1)   | -  | -                    |
| -          | -       | -        | 131     | VDD                                   | S        | -             | (1)   | -  | -                    |
| -          | -       | -        | 132     | PG15                                  | I/O      | FT            | (1)   | EVENTOUT   | -                    |

Table 13. STM32F302xD/E pin definitions (continued)

| Pin number |         |          |         | Pin name<br>(function<br>after reset) | Pin type | I/O structure | Notes | Alternate functions   | Additional functions |
|------------|---------|----------|---------|---------------------------------------|----------|---------------|-------|---|----------------------|
| LQFP64     | LQFP100 | WLCSP100 | LQFP144 |                                       |          |               |       |   |                      |
| 55         | 89      | A5       | 133     | PB3                                   | I/O      | FT            | -     | JTDO-TRACESWO,<br>TIM2_CH2, TIM4_ETR,<br>TSC_G5_IO1, SPI1_SCK,<br>SPI3_SCK/I2S3_CK,<br>USART2_TX, TIM3_ETR,<br>EVENTOUT | -                    |
| 56         | 90      | B5       | 134     | PB4                                   | I/O      | FT            | -     | JTRST, TIM16_CH1,<br>TIM3_CH1, TSC_G5_IO2,<br>SPI1_MISO,<br>SPI3_MISO/I2S3ext_SD,<br>USART2_RX, TIM17_BKIN,<br>EVENTOUT | -                    |
| 57         | 91      | A6       | 135     | PB5                                   | I/O      | FTf           | -     | TIM16_BKIN, TIM3_CH2,<br>I2C1_SMBAL, SPI1_MOSI,<br>SPI3_MOSI/I2S3_SD,<br>USART2_CK, I2C3_SDA,<br>TIM17_CH1, EVENTOUT    | -                    |
| 58         | 92      | B6       | 136     | PB6                                   | I/O      | FTf           | -     | TIM16_CH1N, TIM4_CH1,<br>TSC_G5_IO3, I2C1_SCL,<br>USART1_TX, EVENTOUT   | -                    |
| 59         | 93      | C5       | 137     | PB7                                   | I/O      | FTf           | -     | TIM17_CH1N, TIM4_CH2,<br>TSC_G5_IO4, I2C1_SDA,<br>USART1_RX, TIM3_CH4,<br>FMC_NADV, EVENTOUT                            | -                    |
| 60         | 94      | A7       | 138     | BOOT0                                 | I        | -             | -     | -   | -                    |
| 61         | 95      | D5       | 139     | PB8                                   | I/O      | FTf           | -     | TIM16_CH1, TIM4_CH3,<br>TSC_SYNC, I2C1_SCL,<br>USART3_RX,<br>COMP1_OUT, CAN_RX,<br>TIM1_BKIN, EVENTOUT                  | -                    |
| 62         | 96      | C6       | 140     | PB9                                   | I/O      | FTf           | -     | TIM17_CH1, TIM4_CH4,<br>I2C1_SDA, IR-OUT,<br>USART3_TX,<br>COMP2_OUT, CAN_TX,<br>EVENTOUT                               | -                    |
| -          | 97      | B7       | 141     | PE0                                   | I/O      | FT            | (1)   | EVENTOUT, TIM4_ETR,<br>TIM16_CH1, USART1_TX,<br>FMC_NBL0  | -                    |



Table 13. STM32F302xD/E pin definitions (continued)

| Pin number |         |                                   |         | Pin name<br>(function<br>after reset) | Pin type | I/O structure | Notes | Alternate functions                         | Additional functions |
|------------|---------|-----------------------------------|---------|---------------------------------------|----------|---------------|-------|---|----------------------|
| LQFP64     | LQFP100 | WLCSP100                          | LQFP144 |                                       |          |               |       |   |                      |
| -          | 98      | A8                                | 142     | PE1                                   | I/O      | FT            | (1)   | EVENTOUT, TIM17_CH1,<br>USART1_RX, FMC_NBL1 | -                    |
| 63         | 99      | C7                                | 143     | VSS                                   | S        | -             | -     | -   | -                    |
| 64         | 100     | A9,<br>A10<br>,<br>B10<br>,<br>B8 | 144     | VDD                                   | S        | -             | -     | -   | -                    |

- Function availability depends on the chosen device.
- PC13, PC14 and PC15 are supplied through the power switch. Since the switch sinks only a limited amount of current (3 mA), the use of GPIO PC13 to PC15 in output mode is limited:
  - The speed should not exceed 2 MHz with a maximum load of 30 pF
  - These GPIOs must not be used as current sources (e.g. to drive an LED)
 After the first backup domain power-up, PC13, PC14 and PC15 operate as GPIOs. Their function then depends on the content of the Backup registers which is not reset by the main reset. For details on how to manage these GPIOs, refer to the Battery backup domain and BKP register description sections in the RM0316 reference manual.
- Fast ADC channel.
- The VREF+ functionality is not available on the 64-pin package. In this package, the VREF+ is internally connected to VDDA.
- These GPIOs offer a reduced touch sensing sensitivity. It is thus recommended to use them as sampling capacitor I/O.



Table 14. STM32F302xD/E alternate function mapping

| Port   | AF0    | AF1                         | AF2   | AF3              | AF4                         | AF5  | AF6  | AF7                            | AF8                            | AF9               | AF10              | AF11         | AF12          | AF13 | AF14 | AF15 |              |              |
|--------|--------|-----------------------------|---|------------------|-----------------------------|--|--|--------------------------------|--------------------------------|-------------------|-------------------|--------------|---------------|------|------|------|--------------|--------------|
|        | SYS_AF | TIM2/15/<br>16/17/E<br>VENT | I2C3/TIM1<br>/2/3/4/8/20<br>/15/GPCO<br>MP1 | I2C3//15/<br>TSC | I2C1/2/TI<br>M1/8/16/<br>17 | SPI1/SPI2<br>/I2S2/SPI3<br>/I2S3/SPI4<br>/UART4/5/<br>Infrared | SPI2/I2S2/<br>SPI3/I2S3/<br>TIM1/8/20/<br>Infrared | USART1/2<br>/3/CAN/GP<br>COMP6 | I2C3/GPC<br>OMP1/2/3/<br>4/5/6 | CAN/TIM1<br>/8/15 | TIM2/3/<br>4/8/17 | TIM1/8       | FSMC<br>/TIM1 | -    | -    | -    | EVENT        |              |
| Port A | PA0    | -                           | TIM2_<br>CH1/TIM<br>2_ETR                   | -                | TSC_G1<br>_IO1              | -  | -  | -                              | USART2_<br>CTS                 | COMP1_<br>OUT     | --                | -            | -             | -    | -    | -    | EVENT<br>OUT |              |
|        | PA1    | RTC_<br>REFIN               | TIM2_<br>CH2                                | -                | TSC_G1<br>_IO2              | -  | -  | -                              | USART2_<br>RTS                 | -                 | TIM15_<br>CH1N    | -            | -             | -    | -    | -    | EVENT<br>OUT |              |
|        | PA2    | -                           | TIM2_<br>CH3                                | -                | TSC_G1<br>_IO3              | -  | -  | -                              | USART2_<br>TX                  | COMP2_<br>OUT     | TIM15_<br>CH1     | -            | -             | -    | -    | -    | EVENT<br>OUT |              |
|        | PA3    | -                           | TIM2_<br>CH4                                | -                | TSC_G1<br>_IO4              | -  | -  | -                              | USART2_<br>RX                  | -                 | TIM15_<br>CH2     | -            | -             | -    | -    | -    | EVENT<br>OUT |              |
|        | PA4    | -                           | -   | TIM3_<br>CH2     | TSC_G2<br>_IO1              | -  | SPI1_NSS   | SPI3_NSS<br>/I2S3_WS           | USART2_<br>CK                  | -                 | -                 | -            | -             | -    | -    | -    | -            | EVENT<br>OUT |
|        | PA5    | -                           | TIM2_<br>CH1/TIM<br>2_ETR                   | -                | TSC_G2<br>_IO2              | -  | SPI1_SCK   | -                              | -                              | -                 | -                 | -            | -             | -    | -    | -    | -            | EVENT<br>OUT |
|        | PA6    | -                           | TIM16_<br>CH1                               | TIM3_<br>CH1     | TSC_G2<br>_IO3              | -  | SPI1_<br>MISO                                      | TIM1_<br>BKIN                  | -                              | COMP1_<br>OUT     | -                 | -            | -             | -    | -    | -    | -            | EVENT<br>OUT |
|        | PA7    | -                           | TIM17_<br>CH1                               | TIM3_<br>CH2     | TSC_G2<br>_IO4              | -  | SPI1_<br>MOSI                                      | TIM1_<br>CH1N                  | -                              | -                 | -                 | -            | -             | -    | -    | -    | -            | EVENT<br>OUT |
|        | PA8    | MCO                         | -   | -                | I2C3_<br>SCL                | I2C2_<br>SMBAL   | I2S2_<br>MCK                                       | TIM1_<br>CH1                   | USART1_<br>CK                  | -                 | -                 | TIM4_<br>ETR | -             | -    | -    | -    | -            | EVENT<br>OUT |
|        | PA9    | -                           | -   | I2C3_<br>SMBAL   | TSC_G4<br>_IO1              | I2C2_<br>SCL   | I2S3_<br>MCK                                       | TIM1_<br>CH2                   | USART1_<br>TX                  | -                 | TIM15_<br>BKIN    | TIM2_<br>CH3 | -             | -    | -    | -    | -            | EVENT<br>OUT |



Table 14. STM32F302xD/E alternate function mapping (continued)

| Port   |      | AF0                   | AF1                         | AF2   | AF3              | AF4                         | AF5  | AF6  | AF7                            | AF8                            | AF9               | AF10              | AF11         | AF12           | AF13 | AF14 | AF15         |              |
|--------|------|-----------------------|-----------------------------|---|------------------|-----------------------------|--|--|--------------------------------|--------------------------------|-------------------|-------------------|--------------|----------------|------|------|--------------|--------------|
|        |      | SYS_AF                | TIM2/15/<br>16/17/E<br>VENT | I2C3/TIM1<br>/2/3/4/8/20<br>/15/GPCO<br>MP1 | I2C3//15/<br>TSC | I2C1/2/TI<br>M1/8/16/<br>17 | SPI1/SPI2<br>/I2S2/SPI3<br>/I2S3/SPI4<br>/UART4/5/<br>Infrared | SPI2/I2S2/<br>SPI3/I2S3/<br>TIM1/8/20/<br>Infrared | USART1/2<br>/3/CAN/GP<br>COMP6 | I2C3/GPC<br>OMP1/2/3/<br>4/5/6 | CAN/TIM1<br>/8/15 | TIM2/3/<br>4/8/17 | TIM1/8       | FSMC<br>/TIM1  | -    | -    | -            | EVENT        |
| Port A | PA10 | -                     | TIM17_<br>BKIN              | -   | TSC_G4<br>_IO2   | I2C2_SDA                    | SPI2_MIS<br>O/I2S2ext<br>_SD                                   | TIM1_<br>CH3                                       | USART1_<br>RX                  | COMP6_<br>OUT                  | -                 | TIM2_<br>CH4      | -            | -              | -    | -    | EVENT<br>OUT |              |
|        | PA11 | -                     | -                           | -   | -                | -                           | SPI2_MO<br>SI/I2S2_<br>SD                                      | TIM1_<br>CH1N                                      | USART1_<br>CTS                 | COMP1_<br>OUT                  | CAN_RX            | TIM4_<br>CH1      | TIM1_<br>CH4 | TIM1_<br>BKIN2 | -    | -    | EVENT<br>OUT |              |
|        | PA12 | -                     | TIM16_<br>CH1               | -   | -                | -                           | I2SCKIN  | TIM1_<br>CH2N                                      | USART1_<br>RTS                 | COMP2_<br>OUT                  | CAN_TX            | TIM4_<br>CH2      | TIM1_<br>ETR | -              | -    | -    | EVENT<br>OUT |              |
|        | PA13 | SWDIO-<br>JTMS        | TIM16_<br>CH1N              | -   | TSC_G4<br>_IO3   | -                           | IR-OUT   | -  | USART3_<br>CTS                 | -                              | -                 | TIM4_<br>CH3      | -            | -              | -    | -    | EVENT<br>OUT |              |
|        | PA14 | SWCLK-<br>JTCK        | -                           | -   | TSC_G4<br>_IO4   | I2C1_SDA                    | -  | TIM1_<br>BKIN                                      | USART2_<br>TX                  | -                              | -                 | -                 | -            | -              | -    | -    | -            | EVENT<br>OUT |
|        | PA15 | JTDI                  | TIM2_<br>CH1/TIM<br>2_ETR   | -   | TSC_<br>SYNC     | I2C1_SCL                    | SPI1_NSS   | SPI3_NSS<br>/I2S3_WS                               | USART2_<br>RX                  | -                              | -                 | TIM1_<br>BKIN     | -            | -              | -    | -    | -            | EVENT<br>OUT |
| Port B | PB0  | -                     | -                           | TIM3_<br>CH3                                | TSC_G3<br>_IO2   | -                           | -  | TIM1_<br>CH2N                                      | -                              | -                              | -                 | -                 | -            | -              | -    | -    | EVENT<br>OUT |              |
|        | PB1  | -                     | -                           | TIM3_<br>CH4                                | TSC_G3<br>_IO3   | -                           | -  | TIM1_<br>CH3N                                      | -                              | COMP4_<br>OUT                  | -                 | -                 | -            | -              | -    | -    | EVENT<br>OUT |              |
|        | PB2  | -                     | -                           | -   | TSC_G3<br>_IO4   | -                           | -  | -  | -                              | -                              | -                 | -                 | -            | -              | -    | -    | EVENT<br>OUT |              |
|        | PB3  | JTDO-<br>TRACES<br>WO | TIM2_<br>CH2                | TIM4_<br>ETR                                | TSC_G5<br>_IO1   | -                           | SPI1_SCK   | SPI3_SCK<br>/I2S3_CK                               | USART2_<br>TX                  | -                              | -                 | TIM3_<br>ETR      | -            | -              | -    | -    | EVENT<br>OUT |              |



Table 14. STM32F302xD/E alternate function mapping (continued)

| Port   | AF0    | AF1                         | AF2   | AF3              | AF4                         | AF5  | AF6  | AF7                            | AF8                            | AF9               | AF10              | AF11           | AF12          | AF13          | AF14         | AF15         |
|--------|--------|-----------------------------|---|------------------|-----------------------------|--|--|--------------------------------|--------------------------------|-------------------|-------------------|----------------|---------------|---------------|--------------|--------------|
|        | SYS_AF | TIM2/15/<br>16/17/E<br>VENT | I2C3/TIM1<br>/2/3/4/8/20<br>/15/GPCO<br>MP1 | I2C3//15/<br>TSC | I2C1/2/TI<br>M1/8/16/<br>17 | SPI1/SPI2<br>/I2S2/SPI3<br>/I2S3/SPI4<br>/UART4/5/<br>Infrared | SPI2/I2S2/<br>SPI3/I2S3/<br>TIM1/8/20/<br>Infrared | USART1/2<br>/3/CAN/GP<br>COMP6 | I2C3/GPC<br>OMP1/2/3/<br>4/5/6 | CAN/TIM1<br>/8/15 | TIM2/3/<br>4/8/17 | TIM1/8         | FSMC<br>/TIM1 | -             | -            | EVENT        |
| Port B | PB4    | JTRST                       | TIM16_<br>CH1                               | TIM3_<br>CH1     | TSC_G5<br>_IO2              | -  | SPI1_<br>MISO                                      | SPI3_MIS<br>O/I2S3ext<br>_SD   | USART2_<br>RX                  | -                 | -                 | TIM17_<br>BKIN | -             | -             | -            | EVENT<br>OUT |
|        | PB5    | -                           | TIM16_<br>BKIN                              | TIM3_<br>CH2     | -                           | I2C1_<br>SMBAI   | SPI1_<br>MOSI                                      | SPI3_MO<br>SI/I2S3_<br>SD      | USART2_<br>CK                  | I2C3_SDA          | -                 | TIM17_<br>CH1  | -             | -             | -            | EVENT<br>OUT |
|        | PB6    | -                           | TIM16_<br>CH1N                              | TIM4_<br>CH1     | TSC_G5<br>_IO3              | I2C1_SCL   | -  | -                              | USART1_<br>TX                  | -                 | -                 | -              | -             | -             | -            | EVENT<br>OUT |
|        | PB7    | -                           | TIM17_<br>CH1N                              | TIM4_<br>CH2     | TSC_G5<br>_IO4              | I2C1_SDA   | -  | -                              | USART1_<br>RX                  | -                 | -                 | TIM3_<br>CH4   | -             | FMC_<br>NADV  | -            | EVENT<br>OUT |
|        | PB8    | -                           | TIM16_<br>CH1                               | TIM4_<br>CH3     | TSC_<br>SYNC                | I2C1_SCL   | -  | -                              | USART3_<br>RX                  | COMP1_<br>OUT     | CAN_RX            | -              | -             | TIM1_<br>BKIN | -            | EVENT<br>OUT |
|        | PB9    | -                           | TIM17_<br>CH1                               | TIM4_<br>CH4     | -                           | I2C1_SDA   | -  | IR-OUT                         | USART3_<br>TX                  | COMP2_<br>OUT     | CAN_TX            | -              | -             | -             | -            | EVENT<br>OUT |
|        | PB10   | -                           | TIM2_<br>CH3                                | -                | TSC_<br>SYNC                | -  | -  | -                              | USART3_<br>TX                  | -                 | -                 | -              | -             | -             | -            | EVENT<br>OUT |
|        | PB11   | -                           | TIM2_<br>CH4                                | -                | TSC_G6<br>_IO1              | -  | -  | -                              | USART3_<br>RX                  | -                 | -                 | -              | -             | -             | -            | EVENT<br>OUT |
|        | PB12   | -                           | -   | -                | TSC_G6<br>_IO2              | I2C2_<br>SMBAL   | SPI2_NSS<br>/I2S2_WS                               | TIM1_<br>BKIN                  | USART3_<br>CK                  | -                 | -                 | -              | -             | -             | -            | EVENT<br>OUT |
| PB13   | -      | -                           | -   | TSC_G6<br>_IO3   | -                           | SPI2_SCK<br>/I2S2_CK   | TIM1_<br>CH1N                                      | USART3_<br>CTS                 | -                              | -                 | -                 | -              | -             | -             | EVENT<br>OUT |              |



Table 14. STM32F302xD/E alternate function mapping (continued)

| Port   |      | AF0           | AF1                         | AF2   | AF3              | AF4                         | AF5  | AF6  | AF7                            | AF8                            | AF9               | AF10              | AF11   | AF12          | AF13 | AF14 | AF15         |
|--------|------|---------------|-----------------------------|---|------------------|-----------------------------|--|--|--------------------------------|--------------------------------|-------------------|-------------------|--------|---------------|------|------|--------------|
|        |      | SYS_AF        | TIM2/15/<br>16/17/E<br>VENT | I2C3/TIM1<br>/2/3/4/8/20<br>/15/GPCO<br>MP1 | I2C3//15/<br>TSC | I2C1/2/TI<br>M1/8/16/<br>17 | SPI1/SPI2<br>/I2S2/SPI3<br>/I2S3/SPI4<br>/UART4/5/<br>Infrared | SPI2/I2S2/<br>SPI3/I2S3/<br>TIM1/8/20/<br>Infrared | USART1/2<br>/3/CAN/GP<br>COMP6 | I2C3/GPC<br>OMP1/2/3/<br>4/5/6 | CAN/TIM1<br>/8/15 | TIM2/3/<br>4/8/17 | TIM1/8 | FSMC<br>/TIM1 | -    | -    | EVENT        |
| Port B | PB14 | -             | TIM15_<br>CH1               | -   | TSC_G6<br>_IO4   | -                           | SPI2_MIS<br>O/I2S2ext<br>_SD                                   | TIM1_<br>CH2N                                      | USART3_<br>RTS                 | -                              | -                 | -                 | -      | -             | -    | -    | EVENT<br>OUT |
|        | PB15 | RTC_<br>REFIN | TIM15_<br>CH2               | TIM15_<br>CH1N                              | -                | TIM1_<br>CH3N               | SPI2_MO<br>SI/I2S2_S<br>D                                      | -  | -                              | -                              | -                 | -                 | -      | -             | -    | -    | EVENT<br>OUT |
| Port C | PC0  | -             | EVENT<br>OUT                | TIM1_<br>CH1                                | -                | -                           | -  | -  | -                              | -                              | -                 | -                 | -      | -             | -    | -    | -            |
|        | PC1  | -             | EVENT<br>OUT                | TIM1_<br>CH2                                | -                | -                           | -  | -  | -                              | -                              | -                 | -                 | -      | -             | -    | -    | -            |
|        | PC2  | -             | EVENT<br>OUT                | TIM1_<br>CH3                                | -                | -                           | -  | -  | -                              | -                              | -                 | -                 | -      | -             | -    | -    | -            |
|        | PC3  | -             | EVENT<br>OUT                | TIM1_<br>CH4                                | -                | -                           | -  | TIM1_<br>BKIN2                                     | -                              | -                              | -                 | -                 | -      | -             | -    | -    | -            |
|        | PC4  | -             | EVENT<br>OUT                | TIM1_<br>ETR                                | -                | -                           | -  | -  | USART1_<br>TX                  | -                              | -                 | -                 | -      | -             | -    | -    | -            |
|        | PC5  | -             | EVENT<br>OUT                | TIM15_<br>BKIN                              | TSC_G3<br>_IO1   | -                           | -  | -  | USART1_<br>RX                  | -                              | -                 | -                 | -      | -             | -    | -    | -            |
|        | PC6  | -             | EVENT<br>OUT                | TIM3_<br>CH1                                | -                | -                           | -  | I2S2_<br>MCK                                       | COMP6_O<br>UT                  | -                              | -                 | -                 | -      | -             | -    | -    | -            |
|        | PC7  | -             | EVENT<br>OUT                | TIM3_<br>CH2                                | -                | -                           | -  | I2S3_<br>MCK                                       | -                              | -                              | -                 | -                 | -      | -             | -    | -    | -            |
|        | PC8  | -             | EVENT<br>OUT                | TIM3_<br>CH3                                | -                | -                           | -  | -  | -                              | -                              | -                 | -                 | -      | -             | -    | -    | -            |
|        | PC9  | -             | EVENT<br>OUT                | TIM3_<br>CH4                                | I2C3_<br>SDA     | -                           | I2SCKIN  | -  | -                              | -                              | -                 | -                 | -      | -             | -    | -    | -            |



Table 14. STM32F302xD/E alternate function mapping (continued)

| Port   | AF0    | AF1                         | AF2   | AF3                       | AF4                         | AF5  | AF6  | AF7                            | AF8                            | AF9               | AF10              | AF11   | AF12          | AF13        | AF14 | AF15  |
|--------|--------|-----------------------------|---|---------------------------|-----------------------------|--|--|--------------------------------|--------------------------------|-------------------|-------------------|--------|---------------|-------------|------|-------|
|        | SYS_AF | TIM2/15/<br>16/17/E<br>VENT | I2C3/TIM1<br>/2/3/4/8/20<br>/15/GPCO<br>MP1 | I2C3//15/<br>TSC          | I2C1/2/TI<br>M1/8/16/<br>17 | SPI1/SPI2<br>/I2S2/SPI3<br>/I2S3/SPI4<br>/UART4/5/<br>Infrared | SPI2/I2S2/<br>SPI3/I2S3/<br>TIM1/8/20/<br>Infrared | USART1/2<br>/3/CAN/GP<br>COMP6 | I2C3/GPC<br>OMP1/2/3/<br>4/5/6 | CAN/TIM1<br>/8/15 | TIM2/3/<br>4/8/17 | TIM1/8 | FSMC<br>/TIM1 | -           | -    | EVENT |
| Port C | PC10   | -                           | EVENT<br>OUT                                | -                         | -                           | -  | UART4_<br>TX                                       | SPI3_SCK<br>/I2S3_SCK          | USART3_<br>TX                  | -                 | -                 | -      | -             | -           | -    | -     |
|        | PC11   | -                           | EVENT<br>OUT                                | -                         | -                           | -  | UART4_<br>RX                                       | SPI3_MIS<br>O/I2S3ext<br>_SD   | USART3_<br>RX                  | -                 | -                 | -      | -             | -           | -    | -     |
|        | PC12   | -                           | EVENT<br>OUT                                | -                         | -                           | -  | UART5_<br>TX                                       | SPI3_MO<br>SI/I2S3_<br>SD      | USART3_<br>CK                  | -                 | -                 | -      | -             | -           | -    | -     |
|        | PC13   | -                           | EVENT<br>OUT                                | -                         | -                           | TIM1_<br>CH1N  | -  | -                              | -                              | -                 | -                 | -      | -             | -           | -    | -     |
|        | PC14   | -                           | EVENT<br>OUT                                | -                         | -                           | -  | -  | -                              | -                              | -                 | -                 | -      | -             | -           | -    | -     |
|        | PC15   | -                           | EVENT<br>OUT                                | -                         | -                           | -  | -  | -                              | -                              | -                 | -                 | -      | -             | -           | -    | -     |
| Port D | PD0    | -                           | EVENT<br>OUT                                | -                         | -                           | -  | -  | -                              | CAN_RX                         | -                 | -                 | -      | -             | FMC_D2      | -    | -     |
|        | PD1    | -                           | EVENT<br>OUT                                | -                         | -                           | -  | -  | -                              | CAN_TX                         | -                 | -                 | -      | -             | FMC_D3      | -    | -     |
|        | PD2    | -                           | EVENT<br>OUT                                | TIM3_<br>ETR              | -                           | -  | -  | UART5_<br>RX                   | -                              | -                 | -                 | -      | -             | -           | -    | -     |
|        | PD3    | -                           | EVENT<br>OUT                                | TIM2_CH<br>1/TIM2_<br>ETR | -                           | -  | -  | -                              | USART2_<br>CTS                 | -                 | -                 | -      | -             | FMC_<br>CLK | -    | -     |
|        | PD4    | -                           | EVENT<br>OUT                                | TIM2_<br>CH2              | -                           | -  | -  | -                              | USART2_<br>RTS                 | -                 | -                 | -      | -             | FMC_<br>NOE | -    | -     |



Table 14. STM32F302xD/E alternate function mapping (continued)

| Port   |      | AF0          | AF1                         | AF2   | AF3              | AF4                         | AF5  | AF6  | AF7                            | AF8                            | AF9               | AF10              | AF11   | AF12                     | AF13 | AF14 | AF15  |
|--------|------|--------------|-----------------------------|---|------------------|-----------------------------|--|--|--------------------------------|--------------------------------|-------------------|-------------------|--------|--------------------------|------|------|-------|
|        |      | SYS_AF       | TIM2/15/<br>16/17/E<br>VENT | I2C3/TIM1<br>/2/3/4/8/20<br>/15/GPCO<br>MP1 | I2C3//15/<br>TSC | I2C1/2/TI<br>M1/8/16/<br>17 | SPI1/SPI2<br>/I2S2/SPI3<br>/I2S3/SPI4<br>/UART4/5/<br>Infrared | SPI2/I2S2/<br>SPI3/I2S3/<br>TIM1/8/20/<br>Infrared | USART1/2<br>/3/CAN/GP<br>COMP6 | I2C3/GPC<br>OMP1/2/3/<br>4/5/6 | CAN/TIM1<br>/8/15 | TIM2/3/<br>4/8/17 | TIM1/8 | FSMC<br>/TIM1            | -    | -    | EVENT |
| Port D | PD5  | -            | EVENT<br>OUT                | -   | -                | -                           | -  | -  | USART2_<br>TX                  | -                              | -                 | -                 | -      | FMC_<br>NWE              | -    | -    | -     |
|        | PD6  | -            | EVENT<br>OUT                | TIM2_<br>CH4                                | -                | -                           | -  | -  | USART2_<br>RX                  | -                              | -                 | -                 | -      | FMC_<br>NWAIT            | -    | -    | -     |
|        | PD7  | -            | EVENT<br>OUT                | TIM2_<br>CH3                                | -                | -                           | -  | -  | USART2_<br>CK                  | -                              | -                 | -                 | -      | FMC_NE<br>1/FMC_<br>NCE2 | -    | -    | -     |
|        | PD8  | -            | EVENT<br>OUT                | -   | -                | -                           | -  | -  | USART3_<br>TX                  | -                              | -                 | -                 | -      | FMC_<br>D13              | -    | -    | -     |
|        | PD9  | -            | EVENT<br>OUT                | -   | -                | -                           | -  | -  | USART3_<br>RX                  | -                              | -                 | -                 | -      | FMC_<br>D14              | -    | -    | -     |
|        | PD10 | -            | EVENT<br>OUT                | -   | -                | -                           | -  | -  | USART3_<br>CK                  | -                              | -                 | -                 | -      | FMC_<br>D15              | -    | -    | -     |
|        | PD11 | -            | EVENT<br>OUT                | -   | -                | -                           | -  | -  | USART3_<br>CTS                 | -                              | -                 | -                 | -      | FMC_<br>A16              | -    | -    | -     |
|        | PD12 | -            | EVENT<br>OUT                | TIM4_<br>CH1                                | TSC_G8<br>_IO1   | -                           | -  | -  | USART3_<br>RTS                 | -                              | -                 | -                 | -      | FMC_<br>A17              | -    | -    | -     |
|        | PD13 | -            | EVENT<br>OUT                | TIM4_<br>CH2                                | TSC_G8<br>_IO2   | -                           | -  | -  | -                              | -                              | -                 | -                 | -      | FMC_<br>A18              | -    | -    | -     |
|        | PD14 | -            | EVENT<br>OUT                | TIM4_<br>CH3                                | TSC_G8<br>_IO3   | -                           | -  | -  | -                              | -                              | -                 | -                 | -      | FMC_D0                   | -    | -    | -     |
| PD15   | -    | EVENT<br>OUT | TIM4_<br>CH4                | TSC_G8<br>_IO4                              | -                | -                           | -  | SPI2_NSS   | -                              | -                              | -                 | -                 | FMC_D1 | -                        | -    | -    |       |



Table 14. STM32F302xD/E alternate function mapping (continued)

| Port  | AF0    | AF1                         | AF2   | AF3              | AF4                         | AF5  | AF6  | AF7                            | AF8                            | AF9               | AF10              | AF11   | AF12          | AF13         | AF14 | AF15  |   |
|-------|--------|-----------------------------|---|------------------|-----------------------------|--|--|--------------------------------|--------------------------------|-------------------|-------------------|--------|---------------|--------------|------|-------|---|
|       | SYS_AF | TIM2/15/<br>16/17/E<br>VENT | I2C3/TIM1<br>/2/3/4/8/20<br>/15/GPCO<br>MP1 | I2C3//15/<br>TSC | I2C1/2/TI<br>M1/8/16/<br>17 | SPI1/SPI2<br>/I2S2/SPI3<br>/I2S3/SPI4<br>/UART4/5/<br>Infrared | SPI2/I2S2/<br>SPI3/I2S3/<br>TIM1/8/20/<br>Infrared | USART1/2<br>/3/CAN/GP<br>COMP6 | I2C3/GPC<br>OMP1/2/3/<br>4/5/6 | CAN/TIM1<br>/8/15 | TIM2/3/<br>4/8/17 | TIM1/8 | FSMC<br>/TIM1 | -            | -    | EVENT |   |
| PortE | PE0    | -                           | EVENT<br>OUT                                | TIM4_<br>ETR     | -                           | TIM16_<br>CH1  | -  | -                              | USART1_<br>TX                  | -                 | -                 | -      | -             | FMC_<br>NBL0 | -    | -     | - |
|       | PE1    | -                           | EVENT<br>OUT                                | -                | -                           | TIM17_<br>CH1  | -  | -                              | USART1_<br>RX                  | -                 | -                 | -      | -             | FMC_<br>NBL1 | -    | -     | - |
|       | PE2    | TRACECK                     | EVENT<br>OUT                                | TIM3_<br>CH1     | TSC_G7<br>_IO1              | -  | SPI4_SCK   | -                              | -                              | -                 | -                 | -      | -             | FMC_<br>A23  | -    | -     | - |
|       | PE3    | TRACED0                     | EVENT<br>OUT                                | TIM3_<br>CH2     | TSC_G7<br>_IO2              | -  | SPI4_NSS   | -                              | -                              | -                 | -                 | -      | -             | FMC_<br>A19  | -    | -     | - |
|       | PE4    | TRACED1                     | EVENT<br>OUT                                | TIM3_<br>CH3     | TSC_G7<br>_IO3              | -  | SPI4_NSS   | -                              | -                              | -                 | -                 | -      | -             | FMC_<br>A20  | -    | -     | - |
|       | PE5    | TRACED2                     | EVENT<br>OUT                                | TIM3_<br>CH4     | TSC_G7<br>_IO4              | -  | SPI4_<br>MISO                                      | -                              | -                              | -                 | -                 | -      | -             | FMC_<br>A21  | -    | -     | - |
|       | PE6    | TRACED3                     | EVENT<br>OUT                                | -                | -                           | -  | SPI4_<br>MOSI                                      | -                              | -                              | -                 | -                 | -      | -             | FMC_<br>A22  | -    | -     | - |
|       | PE7    | -                           | EVENT<br>OUT                                | TIM1_<br>ETR     | -                           | -  | -  | -                              | -                              | -                 | -                 | -      | -             | FMC_D4       | -    | -     | - |
|       | PE8    | -                           | EVENT<br>OUT                                | TIM1_<br>CH1N    | -                           | -  | -  | -                              | -                              | -                 | -                 | -      | -             | FMC_D5       | -    | -     | - |
|       | PE9    | -                           | EVENT<br>OUT                                | TIM1_<br>CH1     | -                           | -  | -  | -                              | -                              | -                 | -                 | -      | -             | FMC_D6       | -    | -     | - |
|       | PE10   | -                           | EVENT<br>OUT                                | TIM1_<br>CH2N    | -                           | -  | -  | -                              | -                              | -                 | -                 | -      | -             | FMC_D7       | -    | -     | - |
|       | PE11   | -                           | EVENT<br>OUT                                | TIM1_<br>CH2     | -                           | -  | SPI4_NSS   | -                              | -                              | -                 | -                 | -      | -             | FMC_D8       | -    | -     | - |



Table 14. STM32F302xD/E alternate function mapping (continued)

| Port   |      | AF0    | AF1                         | AF2   | AF3              | AF4                         | AF5  | AF6  | AF7                            | AF8                            | AF9               | AF10              | AF11   | AF12          | AF13 | AF14 | AF15  |
|--------|------|--------|-----------------------------|---|------------------|-----------------------------|--|--|--------------------------------|--------------------------------|-------------------|-------------------|--------|---------------|------|------|-------|
|        |      | SYS_AF | TIM2/15/<br>16/17/E<br>VENT | I2C3/TIM1<br>/2/3/4/8/20<br>/15/GPCO<br>MP1 | I2C3//15/<br>TSC | I2C1/2/TI<br>M1/8/16/<br>17 | SPI1/SPI2<br>/I2S2/SPI3<br>/I2S3/SPI4<br>/UART4/5/<br>Infrared | SPI2/I2S2/<br>SPI3/I2S3/<br>TIM1/8/20/<br>Infrared | USART1/2<br>/3/CAN/GP<br>COMP6 | I2C3/GPC<br>OMP1/2/3/<br>4/5/6 | CAN/TIM1<br>/8/15 | TIM2/3/<br>4/8/17 | TIM1/8 | FSMC<br>/TIM1 | -    | -    | EVENT |
| Port E | PE12 | -      | EVENT<br>OUT                | TIM1_<br>CH3N                               | -                | -                           | SPI4_SCK   | -  | -                              | -                              | -                 | -                 | -      | FMC_D9        | -    | -    | -     |
|        | PE13 | -      | EVENT<br>OUT                | TIM1_<br>CH3                                | -                | -                           | SPI4_<br>MISO  | -  | -                              | -                              | -                 | -                 | -      | FMC_<br>D10   | -    | -    | -     |
|        | PE14 | -      | EVENT<br>OUT                | TIM1_<br>CH4                                | -                | -                           | SPI4_<br>MOSI  | TIM1_<br>BKIN2                                     | -                              | -                              | -                 | -                 | -      | FMC_<br>D11   | -    | -    | -     |
|        | PE15 | -      | EVENT<br>OUT                | TIM1_<br>BKIN                               | -                | -                           | -  | -  | USART3_<br>RX                  | -                              | -                 | -                 | -      | FMC_<br>D12   | -    | -    | -     |
| Port F | PF0  | -      | EVENT<br>OUT                | -   | -                | I2C2_SDA                    | SPI2_NSS<br>/I2S2_WS   | TIM1_<br>CH3N                                      | -                              | -                              | -                 | -                 | -      | -             | -    | -    | -     |
|        | PF1  | -      | EVENT<br>OUT                | -   | -                | I2C2_SCL                    | SPI2_SCK<br>/I2S2_CK   | -  | -                              | -                              | -                 | -                 | -      | -             | -    | -    | -     |
|        | PF2  | -      | EVENT<br>OUT                | -   | -                | -                           | -  | -  | -                              | -                              | -                 | -                 | -      | FMC_A2        | -    | -    | -     |
|        | PF3  | -      | EVENT<br>OUT                | -   | -                | -                           | -  | -  | -                              | -                              | -                 | -                 | -      | FMC_A3        | -    | -    | -     |
|        | PF4  | -      | EVENT<br>OUT                | COMP1_<br>OUT                               | -                | -                           | -  | -  | -                              | -                              | -                 | -                 | -      | FMC_A4        | -    | -    | -     |
|        | PF5  | -      | EVENT<br>OUT                | -   | -                | -                           | -  | -  | -                              | -                              | -                 | -                 | -      | FMC_A5        | -    | -    | -     |
|        | PF6  | -      | EVENT<br>OUT                | TIM4_<br>CH4                                | -                | I2C2_SCL                    | -  | -  | USART3_<br>RTS                 | -                              | -                 | -                 | -      | FMC_<br>NIORD | -    | -    | -     |
|        | PF7  | -      | EVENT<br>OUT                | -   | -                | -                           | -  | -  | -                              | -                              | -                 | -                 | -      | FMC_<br>NREG  | -    | -    | -     |



Table 14. STM32F302xD/E alternate function mapping (continued)

| Port   |      | AF0    | AF1                         | AF2   | AF3              | AF4                         | AF5  | AF6  | AF7                            | AF8                            | AF9               | AF10              | AF11   | AF12          | AF13 | AF14 | AF15  |
|--------|------|--------|-----------------------------|---|------------------|-----------------------------|--|--|--------------------------------|--------------------------------|-------------------|-------------------|--------|---------------|------|------|-------|
|        |      | SYS_AF | TIM2/15/<br>16/17/E<br>VENT | I2C3/TIM1<br>/2/3/4/8/20<br>/15/GPCO<br>MP1 | I2C3//15/<br>TSC | I2C1/2/TI<br>M1/8/16/<br>17 | SPI1/SPI2<br>/I2S2/SPI3<br>/I2S3/SPI4<br>/UART4/5/<br>Infrared | SPI2/I2S2/<br>SPI3/I2S3/<br>TIM1/8/20/<br>Infrared | USART1/2<br>/3/CAN/GP<br>COMP6 | I2C3/GPC<br>OMP1/2/3/<br>4/5/6 | CAN/TIM1<br>/8/15 | TIM2/3/<br>4/8/17 | TIM1/8 | FSMC<br>/TIM1 | -    | -    | EVENT |
| Port F | PF8  | -      | EVENT<br>OUT                | -   | -                | -                           | -  | -  | -                              | -                              | -                 | -                 | -      | FMC_<br>NIOWR | -    | -    | -     |
|        | PF9  | -      | EVENT<br>OUT                | -   | TIM15_<br>CH1    | -                           | SPI2_SCK   | -  | -                              | -                              | -                 | -                 | -      | FMC_CD        | -    | -    | -     |
|        | PF10 | -      | EVENT<br>OUT                | -   | TIM15_<br>CH2    | -                           | SPI2_SCK   | -  | -                              | -                              | -                 | -                 | -      | FMC_<br>INTR  | -    | -    | -     |
|        | PF11 | -      | EVENT<br>OUT                | -   | -                | -                           | -  | -  | -                              | -                              | -                 | -                 | -      | -             | -    | -    | -     |
|        | PF12 | -      | EVENT<br>OUT                | -   | -                | -                           | -  | -  | -                              | -                              | -                 | -                 | -      | FMC_A6        | -    | -    | -     |
|        | PF13 | -      | EVENT<br>OUT                | -   | -                | -                           | -  | -  | -                              | -                              | -                 | -                 | -      | FMC_A7        | -    | -    | -     |
|        | PF14 | -      | EVENT<br>OUT                | -   | -                | -                           | -  | -  | -                              | -                              | -                 | -                 | -      | FMC_A8        | -    | -    | -     |
|        | PF15 | -      | EVENT<br>OUT                | -   | -                | -                           | -  | -  | -                              | -                              | -                 | -                 | -      | FMC_A9        | -    | -    | -     |
| Port G | PG0  | -      | EVENT<br>OUT                | -   | -                | -                           | -  | -  | -                              | -                              | -                 | -                 | -      | FMC_<br>A10   | -    | -    | -     |
|        | PG1  | -      | EVENT<br>OUT                | -   | -                | -                           | -  | -  | -                              | -                              | -                 | -                 | -      | FMC_<br>A11   | -    | -    | -     |
|        | PG2  | -      | EVENT<br>OUT                | -   | -                | -                           | -  | -  | -                              | -                              | -                 | -                 | -      | FMC_<br>A12   | -    | -    | -     |
|        | PG3  | -      | EVENT<br>OUT                | -   | -                | -                           | -  | -  | -                              | -                              | -                 | -                 | -      | FMC_<br>A13   | -    | -    | -     |
|        | PG4  | -      | EVENT<br>OUT                | -   | -                | -                           | -  | -  | -                              | -                              | -                 | -                 | -      | FMC_<br>A14   | -    | -    | -     |



Table 14. STM32F302xD/E alternate function mapping (continued)

| Port   | AF0    | AF1                         | AF2   | AF3              | AF4                         | AF5  | AF6  | AF7                            | AF8                            | AF9               | AF10              | AF11   | AF12                           | AF13 | AF14 | AF15  |
|--------|--------|-----------------------------|---|------------------|-----------------------------|--|--|--------------------------------|--------------------------------|-------------------|-------------------|--------|--------------------------------|------|------|-------|
|        | SYS_AF | TIM2/15/<br>16/17/E<br>VENT | I2C3/TIM1<br>/2/3/4/8/20<br>/15/GPCO<br>MP1 | I2C3//15/<br>TSC | I2C1/2/TI<br>M1/8/16/<br>17 | SPI1/SPI2<br>/I2S2/SPI3<br>/I2S3/SPI4<br>/UART4/5/<br>Infrared | SPI2/I2S2/<br>SPI3/I2S3/<br>TIM1/8/20/<br>Infrared | USART1/2<br>/3/CAN/GP<br>COMP6 | I2C3/GPC<br>OMP1/2/3/<br>4/5/6 | CAN/TIM1<br>/8/15 | TIM2/3/<br>4/8/17 | TIM1/8 | FSMC<br>/TIM1                  | -    | -    | EVENT |
| Port G | PG5    | -                           | EVENT<br>OUT                                | -                | -                           | -  | -  | -                              | -                              | -                 | -                 | -      | FMC_<br>A15                    | -    | -    | -     |
|        | PG6    | -                           | EVENT<br>OUT                                | -                | -                           | -  | -  | -                              | -                              | -                 | -                 | -      | FMC_<br>INT2                   | -    | -    | -     |
|        | PG7    | -                           | EVENT<br>OUT                                | -                | -                           | -  | -  | -                              | -                              | -                 | -                 | -      | FMC_<br>INT3                   | -    | -    | -     |
|        | PG8    | -                           | EVENT<br>OUT                                | -                | -                           | -  | -  | -                              | -                              | -                 | -                 | -      | -                              | -    | -    | -     |
|        | PG9    | -                           | EVENT<br>OUT                                | -                | -                           | -  | -  | -                              | -                              | -                 | -                 | -      | FMC_NE<br>2/FMC_<br>NCE3       | -    | -    | -     |
|        | PG10   | -                           | EVENT<br>OUT                                | -                | -                           | -  | -  | -                              | -                              | -                 | -                 | -      | FMC_<br>NCE4_1/<br>FMC_<br>NE3 | -    | -    | -     |
|        | PG11   | -                           | EVENT<br>OUT                                | -                | -                           | -  | -  | -                              | -                              | -                 | -                 | -      | FMC_<br>NCE4_2                 | -    | -    | -     |
|        | PG12   | -                           | EVENT<br>OUT                                | -                | -                           | -  | -  | -                              | -                              | -                 | -                 | -      | FMC_<br>NE4                    | -    | -    | -     |
|        | PG13   | -                           | EVENT<br>OUT                                | -                | -                           | -  | -  | -                              | -                              | -                 | -                 | -      | FMC_<br>A24                    | -    | -    | -     |
|        | PG14   | -                           | EVENT<br>OUT                                | -                | -                           | -  | -  | -                              | -                              | -                 | -                 | -      | FMC_<br>A25                    | -    | -    | -     |
| PG15   | -      | EVENT<br>OUT                | -   | -                | -                           | -  | -  | -                              | -                              | -                 | -                 | -      | -                              | -    | -    |       |

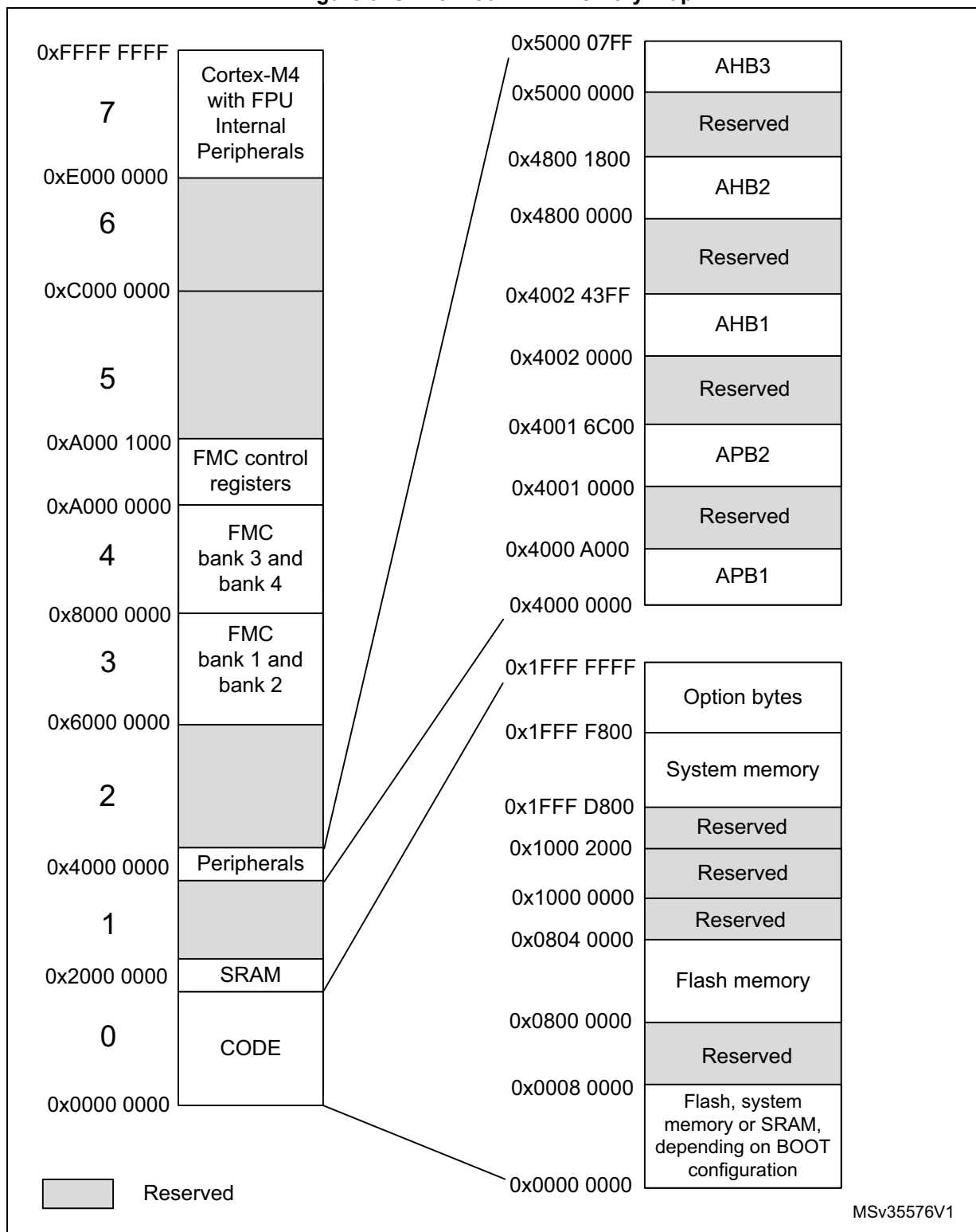


Table 14. STM32F302xD/E alternate function mapping (continued)

| Port   |     | AF0    | AF1                         | AF2   | AF3              | AF4                         | AF5  | AF6  | AF7                            | AF8                            | AF9               | AF10              | AF11   | AF12          | AF13 | AF14 | AF15 |
|--------|-----|--------|-----------------------------|---|------------------|-----------------------------|--|--|--------------------------------|--------------------------------|-------------------|-------------------|--------|---------------|------|------|------|
|        |     | SYS_AF | TIM2/15/<br>16/17/E<br>VENT | I2C3/TIM1<br>/2/3/4/8/20<br>/15/GPCO<br>MP1 | I2C3//15/<br>TSC | I2C1/2/TI<br>M1/8/16/<br>17 | SPI1/SPI2<br>/I2S2/SPI3<br>/I2S3/SPI4<br>/UART4/5/<br>Infrared | SPI2/I2S2/<br>SPI3/I2S3/<br>TIM1/8/20/<br>Infrared | USART1/2<br>/3/CAN/GP<br>COMP6 | I2C3/GPC<br>OMP1/2/3/<br>4/5/6 | CAN/TIM1<br>/8/15 | TIM2/3/<br>4/8/17 | TIM1/8 | FSMC<br>/TIM1 | -    | -    | -    |
| Port H | PH0 | -      | EVENT<br>OUT                | -   | -                | -                           | -  | -  | -                              | -                              | -                 | -                 | -      | FMC_A0        | -    | -    | -    |
|        | PH1 | -      | EVENT<br>OUT                | -   | -                | -                           | -  | -  | -                              | -                              | -                 | -                 | -      | FMC_A1        | -    | -    | -    |
|        | PH2 | -      | EVENT<br>OUT                | -   | -                | -                           | -  | -  | -                              | -                              | -                 | -                 | -      | -             | -    | -    | -    |

# 5 Memory mapping

Figure 9. STM32F302xD/E memory map



MSv35576V1

Table 15. Memory map, peripheral register boundary addresses

| Bus  | Boundary address          | Size (bytes) | Peripheral             |
|------|---------------------------|--------------|------------------------|
| AHB4 | 0xA000 0000 - 0xA000 0FFF | 4 K          | FSMC control registers |
|      | 0x8000 0000 - 0x9FFF FFFF | 512 M        | FSMC Banks 3 and 4     |
|      | 0x6000 0000 - 0x7FFF FFFF | 512 M        | FSMC Banks 1 and 2     |
| -    | 0x5000 0400 - 0x5FFF FFFF | ~384 M       | Reserved               |
| AHB3 | 0x5000 0000 - 0x5000 03FF | 1 K          | ADC1 - ADC2            |
| -    | 0x4800 2000 - 0x4FFF FFFF | ~132 M       | Reserved               |
| AHB2 | 0x4800 1C00 - 0x4800 1FFF | 1 K          | GPIOH                  |
|      | 0x4800 1800 - 0x4800 1BFF | 1 K          | GPIOG                  |
|      | 0x4800 1400 - 0x4800 17FF | 1 K          | GPIOF                  |
|      | 0x4800 1000 - 0x4800 13FF | 1 K          | GPIOE                  |
|      | 0x4800 0C00 - 0x4800 0FFF | 1 K          | GIOD                   |
|      | 0x4800 0800 - 0x4800 0BFF | 1 K          | GPIOC                  |
|      | 0x4800 0400 - 0x4800 07FF | 1 K          | GPIOB                  |
|      | 0x4800 0000 - 0x4800 03FF | 1 K          | GPIOA                  |
| -    | 0x4002 4400 - 0x47FF FFFF | ~128 M       | Reserved               |
| AHB1 | 0x4002 4000 - 0x4002 43FF | 1 K          | TSC                    |
|      | 0x4002 3400 - 0x4002 3FFF | 3 K          | Reserved               |
|      | 0x4002 3000 - 0x4002 33FF | 1 K          | CRC                    |
|      | 0x4002 2400 - 0x4002 2FFF | 3 K          | Reserved               |
|      | 0x4002 2000 - 0x4002 23FF | 1 K          | Flash interface        |
|      | 0x4002 1400 - 0x4002 1FFF | 3 K          | Reserved               |
|      | 0x4002 1000 - 0x4002 13FF | 1 K          | RCC                    |
|      | 0x4002 0800 - 0x4002 0FFF | 2 K          | Reserved               |
|      | 0x4002 0400 - 0x4002 07FF | 1 K          | DMA2                   |
|      | 0x4002 0000 - 0x4002 03FF | 1 K          | DMA1                   |
| -    | 0x4001 8000 - 0x4001 FFFF | 32 K         | Reserved               |
| APB2 | 0x4001 4C00 - 0x4001 7FFF | 13 K         | Reserved               |
|      | 0x4001 4800 - 0x4001 4BFF | 1 K          | TIM17                  |
|      | 0x4001 4400 - 0x4001 47FF | 1 K          | TIM16                  |
|      | 0x4001 4000 - 0x4001 43FF | 1 K          | TIM15                  |
|      | 0x4001 3C00 - 0x4001 3FFF | 1 K          | SPI4                   |
|      | 0x4001 3800 - 0x4001 3BFF | 1 K          | USART1                 |
|      | 0x4001 3400 - 0x4001 37FF | 1 K          | Reserved               |
|      | 0x4001 3000 - 0x4001 33FF | 1 K          | SPI1                   |

**Table 15. Memory map, peripheral register boundary addresses (continued)**

| Bus                       | Boundary address          | Size (bytes) | Peripheral            |
|---------------------------|---------------------------|--------------|-----------------------|
| APB2                      | 0x4001 2C00 - 0x4001 2FFF | 1 K          | TIM1                  |
|                           | 0x4001 0800 - 0x4001 2BFF | 9 K          | Reserved              |
|                           | 0x4001 0400 - 0x4001 07FF | 1 K          | EXTI                  |
|                           | 0x4001 0000 - 0x4001 03FF | 1 K          | SYSCFG + COMP + OPAMP |
| -                         | 0x4000 7C00 - 0x4000 FFFF | 32 K         | Reserved              |
| APB1                      | 0x4000 7800 - 0x4000 7BFF | 1 K          | I2C3                  |
|                           | 0x4000 7400 - 0x4000 77FF | 1 K          | DAC                   |
|                           | 0x4000 7000 - 0x4000 73FF | 1 K          | PWR                   |
|                           | 0x4000 6800 - 0x4000 6FFF | 2 K          | Reserved              |
|                           | 0x4000 6400 - 0x4000 67FF | 1 K          | bxCAN                 |
|                           | 0x4000 6000 - 0x4000 63FF | 1 K          | USB/CAN SRAM          |
|                           | 0x4000 5C00 - 0x4000 5FFF | 1 K          | USB device FS         |
|                           | 0x4000 5800 - 0x4000 5BFF | 1 K          | I2C2                  |
|                           | 0x4000 5400 - 0x4000 57FF | 1 K          | I2C1                  |
|                           | 0x4000 5000 - 0x4000 53FF | 1 K          | UART5                 |
|                           | 0x4000 4C00 - 0x4000 4FFF | 1 K          | UART4                 |
|                           | 0x4000 4800 - 0x4000 4BFF | 1 K          | USART3                |
|                           | 0x4000 4400 - 0x4000 47FF | 1 K          | USART2                |
|                           | 0x4000 4000 - 0x4000 43FF | 1 K          | I2S3ext               |
|                           | 0x4000 3C00 - 0x4000 3FFF | 1 K          | SPI3/I2S3             |
|                           | 0x4000 3800 - 0x4000 3BFF | 1 K          | SPI2/I2S2             |
|                           | 0x4000 3400 - 0x4000 37FF | 1 K          | I2S2ext               |
|                           | 0x4000 3000 - 0x4000 33FF | 1 K          | IWDG                  |
|                           | 0x4000 2C00 - 0x4000 2FFF | 1 K          | WWDG                  |
|                           | 0x4000 2800 - 0x4000 2BFF | 1 K          | RTC                   |
|                           | 0x4000 1800 - 0x4000 27FF | 4 K          | Reserved              |
|                           | 0x4000 1000 - 0x4000 13FF | 1 K          | TIM6                  |
|                           | 0x4000 0C00 - 0x4000 0FFF | 1 K          | Reserved              |
|                           | 0x4000 0800 - 0x4000 0BFF | 1 K          | TIM4                  |
| 0x4000 0400 - 0x4000 07FF | 1 K                       | TIM3         |                       |
| 0x4000 0000 - 0x4000 03FF | 1 K                       | TIM2         |                       |

## 6 Electrical characteristics

### 6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to  $V_{SS}$ .

#### 6.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at  $T_A = 25\text{ }^\circ\text{C}$  and  $T_A = T_{Amax}$  (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation ( $\text{mean} \pm 3\sigma$ ).

#### 6.1.2 Typical values

Unless otherwise specified, typical data are based on  $T_A = 25\text{ }^\circ\text{C}$ ,  $V_{DD} = V_{DDA} = 2.0$  to  $3.6\text{ V}$ . They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated ( $\text{mean} \pm 2\sigma$ ).

#### 6.1.3 Typical curves

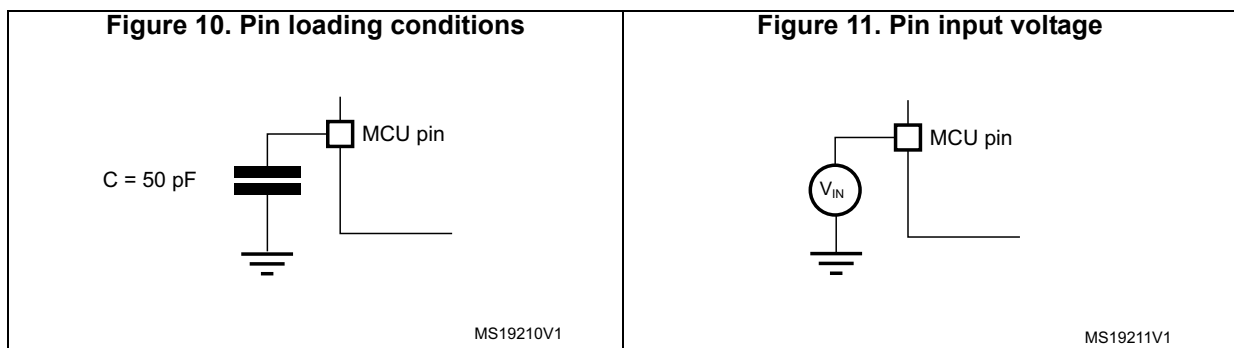
Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

#### 6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in [Figure 10](#).

#### 6.1.5 Pin input voltage

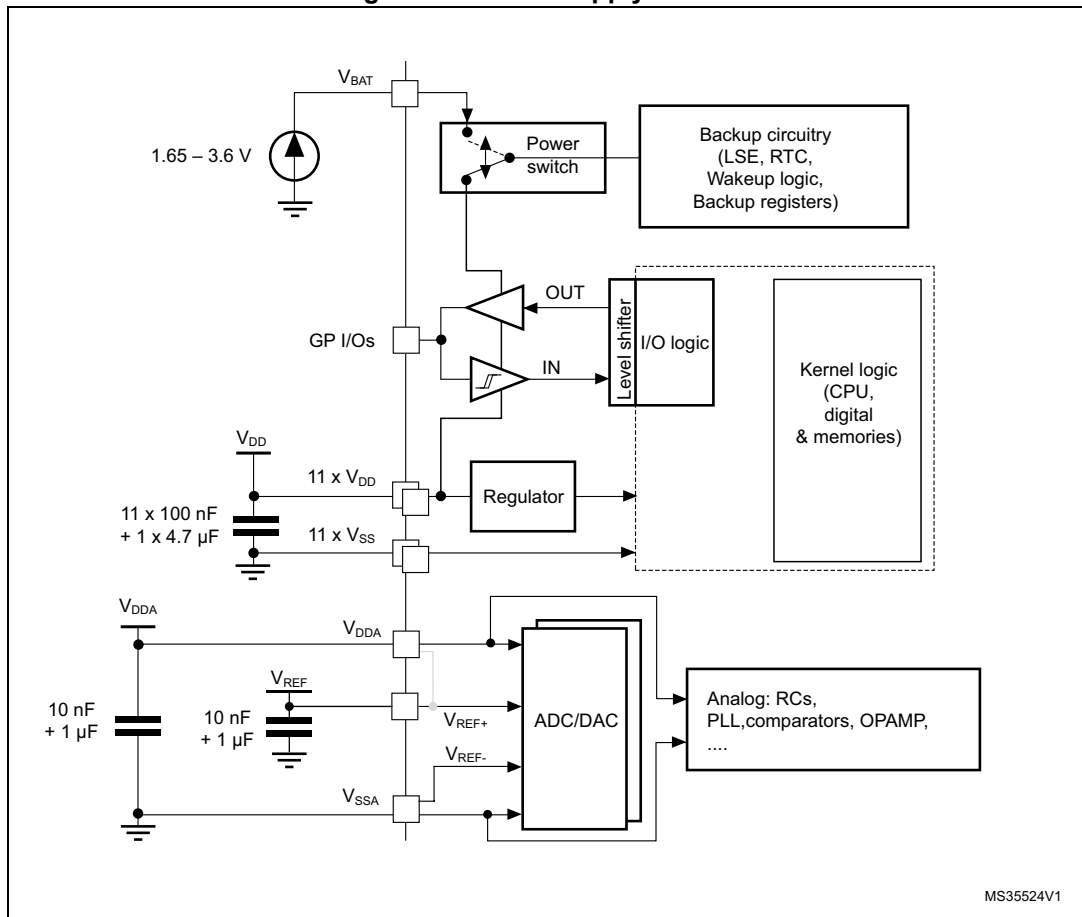
The input voltage measurement on a pin of the device is described in [Figure 11](#).





6.1.6 Power supply scheme

Figure 12. Power supply scheme

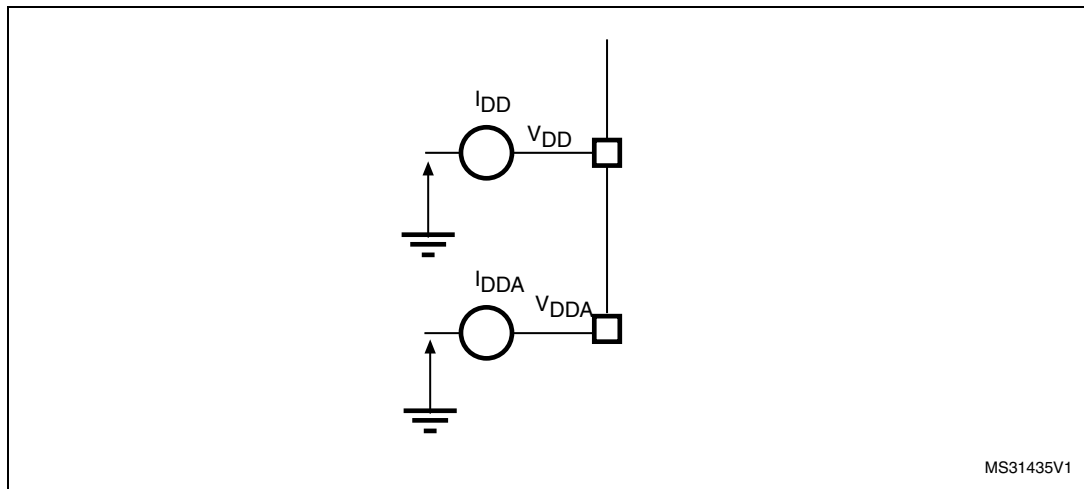


1. Dotted lines represent the internal connections on low pin count packages, joining the dedicated supply pins.

**Caution:** Each power supply pair ( $V_{DD}/V_{SS}$ ,  $V_{DDA}/V_{SSA}$  etc.) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

### 6.1.7 Current consumption measurement

Figure 13. Current consumption measurement scheme



## 6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in [Table 16: Voltage characteristics](#), [Table 17: Current characteristics](#), and [Table 18: Thermal characteristics](#) may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 16. Voltage characteristics<sup>(1)</sup>

| Symbol                            | Ratings  | Min  | Max            | Unit |
|-----------------------------------|--|--|----------------|------|
| $V_{DD}-V_{SS}$                   | External main supply voltage (including $V_{DDA}$ , $V_{BAT}$ and $V_{DD}$ ) | -0.3   | 4.0            | V    |
| $V_{DD}-V_{DDA}$                  | Allowed voltage difference for $V_{DD} > V_{DDA}$                            | -  | 0.4            |      |
| $V_{REF+}-V_{DDA}$ <sup>(2)</sup> | Allowed voltage difference for $V_{REF+} > V_{DDA}$                          | -  | 0.4            |      |
| $V_{IN}$ <sup>(3)</sup>           | Input voltage on FT and FTf pins   | $V_{SS} - 0.3$   | $V_{DD} + 4.0$ | V    |
|                                   | Input voltage on TTa pins  | $V_{SS} - 0.3$   | 4.0            |      |
|                                   | Input voltage on any other pin   | $V_{SS} - 0.3$   | 4.0            |      |
|                                   | Input voltage on Boot0 pin   | 0  | 9              |      |
| $ \Delta V_{DDx} $                | Variations between different $V_{DD}$ power pins                             | -  | 50             | mV   |
| $ V_{SSx} - V_{SS} $              | Variations between all the different ground pins                             | -  | 50             |      |
| $V_{ESD(HBM)}$                    | Electrostatic discharge voltage (human body model)                           | see <a href="#">Section 6.3.13: Electrical sensitivity characteristics</a> |                | -    |

- All main power ( $V_{DD}$ ,  $V_{DDA}$ ) and ground ( $V_{SS}$ ,  $V_{SSA}$ ) pins must always be connected to the external power supply, in the permitted range. The following relationship must be respected between  $V_{DDA}$  and  $V_{DD}$ :  
 $V_{DDA}$  must power on before or at the same time as  $V_{DD}$  in the power up sequence.  
 $V_{DDA}$  must be greater than or equal to  $V_{DD}$ .
- $V_{REF+}$  must be always lower or equal than  $V_{DDA}$  ( $V_{REF+} \leq V_{DDA}$ ). If unused then it must be connected to  $V_{DDA}$ .
- $V_{IN}$  maximum must always be respected. Refer to [Table 17: Current characteristics](#) for the maximum allowed injected current values.

**Table 17. Current characteristics**

| Symbol                | Ratings  | Max.  | Unit |
|-----------------------|--|-------|------|
| $\Sigma I_{VDD}$      | Total current into sum of all VDD_x power lines (source)                       | 160   | mA   |
| $\Sigma I_{VSS}$      | Total current out of sum of all VSS_x ground lines (sink)                      | -160  |      |
| $I_{VDD}$             | Maximum current into each VDD_x power line (source) <sup>(1)</sup>             | 100   |      |
| $I_{VSS}$             | Maximum current out of each VSS_x ground line (sink) <sup>(1)</sup>            | 100   |      |
| $I_{IO(PIN)}$         | Output current sunk by any I/O and control pin                                 | 25    |      |
|                       | Output current source by any I/O and control pin                               | -25   |      |
| $\Sigma I_{IO(PIN)}$  | Total output current sunk by sum of all IOs and control pins <sup>(2)</sup>    | 80    |      |
|                       | Total output current sourced by sum of all IOs and control pins <sup>(2)</sup> | -80   |      |
| $I_{INJ(PIN)}$        | Injected current on FT, FTf, and B pins <sup>(3)</sup>                         | -5/+0 |      |
|                       | Injected current on TC and RST pin <sup>(4)</sup>                              | ±5    |      |
|                       | Injected current on TTa pins <sup>(5)</sup>                                    | ±5    |      |
| $\Sigma I_{INJ(PIN)}$ | Total injected current (sum of all I/O and control pins) <sup>(6)</sup>        | ±25   |      |

1. All main power (VDD, VDDA) and ground (VSS and VSSA) pins must always be connected to the external power supply, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.
3. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
4. A positive injection is induced by  $V_{IN} > V_{DD}$  while a negative injection is induced by  $V_{IN} < V_{SS}$ .  $I_{INJ(PIN)}$  must never be exceeded. Refer to [Table 16: Voltage characteristics](#) for the maximum allowed input voltage values.
5. A positive injection is induced by  $V_{IN} > V_{DDA}$  while a negative injection is induced by  $V_{IN} < V_{SS}$ .  $I_{INJ(PIN)}$  must never be exceeded. Refer also to [Table 16: Voltage characteristics](#) for the maximum allowed input voltage values. Negative injection disturbs the analog performance of the device. See note <sup>(2)</sup> below [Table 81](#).
6. When several inputs are submitted to a current injection, the maximum  $\Sigma I_{INJ(PIN)}$  is the absolute sum of the positive and negative injected currents (instantaneous values).

**Table 18. Thermal characteristics**

| Symbol    | Ratings                      | Value       | Unit |
|-----------|------------------------------|-------------|------|
| $T_{STG}$ | Storage temperature range    | -65 to +150 | °C   |
| $T_J$     | Maximum junction temperature | 150         | °C   |

## 6.3 Operating conditions

### 6.3.1 General operating conditions

Table 19. General operating conditions

| Symbol      | Parameter   | Conditions   | Min  | Max           | Unit |
|-------------|---|--|------|---------------|------|
| $f_{HCLK}$  | Internal AHB clock frequency  | -  | 0    | 72            | MHz  |
| $f_{PCLK1}$ | Internal APB1 clock frequency   | -  | 0    | 36            |      |
| $f_{PCLK2}$ | Internal APB2 clock frequency   | -  | 0    | 72            |      |
| $V_{DD}$    | Standard operating voltage  | -  | 2    | 3.6           | V    |
| $V_{DDA}$   | Analog operating voltage (OPAMP and DAC not used)   | Must have a potential equal to or higher than $V_{DD}$ | 2    | 3.6           | V    |
|             | Analog operating voltage (OPAMP and DAC used)   |  | 2.4  | 3.6           |      |
| $V_{BAT}$   | Backup operating voltage  | -  | 1.65 | 3.6           | V    |
| $V_{IN}$    | I/O input voltage   | TC I/O   | -0.3 | $V_{DD}+0.3$  | V    |
|             |   | TTa I/O  | -0.3 | $V_{DDA}+0.3$ |      |
|             |   | FT and FTf I/O <sup>(1)</sup>                          | -0.3 | 5.5           |      |
|             |   | BOOT0  | 0    | 5.5           |      |
| $P_D$       | Power dissipation at $T_A = 85\text{ °C}$ for suffix 6 or $T_A = 105\text{ °C}$ for suffix 7 <sup>(2)</sup> | LQFP144  | -    | 606           | mW   |
|             |   | WLCSP100   | -    | 454           |      |
|             |   | LQFP100  | -    | 476           |      |
|             |   | UFBGA100   | -    | 339           |      |
|             |   | LQFP64   | -    | 435           |      |
| $T_A$       | Ambient temperature for 6 suffix version  | Maximum power dissipation                              | -40  | 85            | °C   |
|             |   | Low power dissipation <sup>(3)</sup>                   | -40  | 105           |      |
|             | Ambient temperature for 7 suffix version  | Maximum power dissipation                              | -40  | 105           | °C   |
|             |   | Low power dissipation <sup>(3)</sup>                   | -40  | 125           |      |
| $T_J$       | Junction temperature range  | 6 suffix version                                       | -40  | 105           | °C   |
|             |   | 7 suffix version                                       | -40  | 125           |      |

1. To sustain a voltage higher than  $V_{DD}+0.3\text{ V}$ , the internal pull-up/pull-down resistors must be disabled.
2. If  $T_A$  is lower, higher  $P_D$  values are allowed as long as  $T_J$  does not exceed  $T_{Jmax}$  (see [Section 7.7: Thermal characteristics](#)).
3. In low power dissipation state,  $T_A$  can be extended to this range as long as  $T_J$  does not exceed  $T_{Jmax}$  (see [Section 7.7: Thermal characteristics](#)).

### 6.3.2 Operating conditions at power-up / power-down

The parameters given in [Table 20](#) are derived from tests performed under the ambient temperature condition summarized in [Table 19](#).

**Table 20. Operating conditions at power-up / power-down**

| Symbol     | Parameter                | Conditions | Min | Max      | Unit            |
|------------|--------------------------|------------|-----|----------|-----------------|
| $t_{VDD}$  | $V_{DD}$ rise time rate  | -          | 0   | $\infty$ | $\mu\text{s/V}$ |
|            | $V_{DD}$ fall time rate  |            | 20  | $\infty$ |                 |
| $t_{VDDA}$ | $V_{DDA}$ rise time rate | -          | 0   | $\infty$ |                 |
|            | $V_{DDA}$ fall time rate |            | 20  | $\infty$ |                 |

### 6.3.3 Embedded reset and power control block characteristics

The parameters given in [Table 21](#) are derived from tests performed under ambient temperature and  $V_{DD}$  supply voltage conditions summarized in [Table 19](#).

**Table 21. Embedded reset and power control block characteristics**

| Symbol              | Parameter                           | Conditions   | Min.               | Typ. | Max. | Unit |
|---------------------|-------------------------------------|--------------|--------------------|------|------|------|
| $V_{POR/PDR}^{(1)}$ | Power on/power down reset threshold | Falling edge | 1.8 <sup>(2)</sup> | 1.88 | 1.96 | V    |
|                     |                                     | Rising edge  | 1.84               | 1.92 | 2.0  | V    |
| $V_{PDRhyst}^{(1)}$ | PDR hysteresis                      | -            | -                  | 40   | -    | mV   |

1. The PDR detector monitors  $V_{DD}$  and also  $V_{DDA}$  (if kept enabled in the option bytes). The POR detector monitors only  $V_{DD}$ .
2. The product behavior is guaranteed by design down to the minimum  $V_{POR/PDR}$  value.

**Table 22. Programmable voltage detector characteristics**

| Symbol     | Parameter       | Conditions   | Min <sup>(1)</sup> | Typ  | Max <sup>(1)</sup> | Unit |
|------------|-----------------|--------------|--------------------|------|--------------------|------|
| $V_{PVD0}$ | PVD threshold 0 | Rising edge  | 2.1                | 2.18 | 2.26               | V    |
|            |                 | Falling edge | 2                  | 2.08 | 2.16               |      |
| $V_{PVD1}$ | PVD threshold 1 | Rising edge  | 2.19               | 2.28 | 2.37               |      |
|            |                 | Falling edge | 2.09               | 2.18 | 2.27               |      |
| $V_{PVD2}$ | PVD threshold 2 | Rising edge  | 2.28               | 2.38 | 2.48               |      |
|            |                 | Falling edge | 2.18               | 2.28 | 2.38               |      |
| $V_{PVD3}$ | PVD threshold 3 | Rising edge  | 2.38               | 2.48 | 2.58               |      |
|            |                 | Falling edge | 2.28               | 2.38 | 2.48               |      |
| $V_{PVD4}$ | PVD threshold 4 | Rising edge  | 2.47               | 2.58 | 2.69               |      |
|            |                 | Falling edge | 2.37               | 2.48 | 2.59               |      |
| $V_{PVD5}$ | PVD threshold 5 | Rising edge  | 2.57               | 2.68 | 2.79               |      |
|            |                 | Falling edge | 2.47               | 2.58 | 2.69               |      |

Table 22. Programmable voltage detector characteristics (continued)

| Symbol                              | Parameter               | Conditions   | Min <sup>(1)</sup> | Typ  | Max <sup>(1)</sup> | Unit |
|-------------------------------------|-------------------------|--------------|--------------------|------|--------------------|------|
| V <sub>PVD6</sub>                   | PVD threshold 6         | Rising edge  | 2.66               | 2.78 | 2.9                | V    |
|                                     |                         | Falling edge | 2.56               | 2.68 | 2.8                |      |
| V <sub>PVD7</sub>                   | PVD threshold 7         | Rising edge  | 2.76               | 2.88 | 3                  |      |
|                                     |                         | Falling edge | 2.66               | 2.78 | 2.9                |      |
| V <sub>PVDhyst</sub> <sup>(2)</sup> | PVD hysteresis          | -            | -                  | 100  | -                  | mV   |
| IDD(PVD)                            | PVD current consumption | -            | -                  | 0.15 | 0.26               | μA   |

1. Data based on characterization results only, not tested in production.

2. Guaranteed by design, not tested in production.

### 6.3.4 Embedded reference voltage

The parameters given in [Table 23](#) are derived from tests performed under ambient temperature and V<sub>DD</sub> supply voltage conditions summarized in [Table 19](#).

Table 23. Embedded internal reference voltage

| Symbol                 | Parameter   | Conditions                        | Min  | Typ | Max                 | Unit   |
|------------------------|---|-----------------------------------|------|-----|---------------------|--------|
| V <sub>REFINT</sub>    | Internal reference voltage                                    | -40 °C < T <sub>A</sub> < +105 °C | 1.16 | 1.2 | 1.25                | V      |
|                        |   | -40 °C < T <sub>A</sub> < +85 °C  | 1.16 | 1.2 | 1.24 <sup>(1)</sup> | V      |
| T <sub>S_vrefint</sub> | ADC sampling time when reading the internal reference voltage | -                                 | 2.2  | -   | -                   | μs     |
| V <sub>REERINT</sub>   | Internal reference voltage spread over the temperature range  | V <sub>DD</sub> = 3 V ±10 mV      | -    | -   | 10 <sup>(2)</sup>   | mV     |
| T <sub>Coeff</sub>     | Temperature coefficient                                       | -                                 | -    | -   | 100 <sup>(2)</sup>  | ppm/°C |

1. Data based on characterization results, not tested in production.

2. Guaranteed by design, not tested in production.

Table 24. Internal reference voltage calibration values

| Calibration value name  | Description   | Memory address            |
|-------------------------|---|---------------------------|
| V <sub>REFINT_CAL</sub> | Raw data acquired at temperature of 30 °C<br>V <sub>DDA</sub> = 3.3 V | 0x1FFF F7BA - 0x1FFF F7BB |

### 6.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in [Figure 13: Current consumption measurement scheme](#).

All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to CoreMark code.

Note: The total current consumption is the sum of  $I_{DD}$  and  $I_{DDA}$ .

**Typical and maximum current consumption**

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at  $V_{DD}$  or  $V_{SS}$  (no load)
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted to the  $f_{HCLK}$  frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states from 48 to 72 MHz)
- Prefetch in ON (reminder: this bit must be set before clock setting and bus prescaling)
- When the peripherals are enabled  $f_{PCLK2} = f_{HCLK}$  and  $f_{PCLK1} = f_{HCLK}/2$
- When  $f_{HCLK} > 8$  MHz, the PLL is ON and the PLL input is equal to HSI/2 (4 MHz) or HSE (8 MHz) in bypass mode.

The parameters given in [Table 25](#) to [Table 29](#) are derived from tests performed under ambient temperature and supply voltage conditions summarized in [Table 19](#).

**Table 25. Typical and maximum current consumption from  $V_{DD}$  supply at  $V_{DD} = 3.6V$**

| Symbol   | Parameter  | Conditions                  | $f_{HCLK}$ | All peripherals enabled |                     |       |                     | All peripherals disabled |                     |       |                     | Unit |
|----------|--|-----------------------------|------------|-------------------------|---------------------|-------|---------------------|--------------------------|---------------------|-------|---------------------|------|
|          |  |                             |            | Typ                     | Max @ $T_A^{(1)}$   |       |                     | Typ                      | Max @ $T_A^{(1)}$   |       |                     |      |
|          |  |                             |            |                         | 25 °C               | 85 °C | 105 °C              |                          | 25 °C               | 85 °C | 105 °C              |      |
| $I_{DD}$ | Supply current in Run mode, executing from Flash | External clock (HSE bypass) | 72 MHz     | 66.4                    | 76.5                | 76.9  | 77.4                | 33.0                     | 37.2                | 38.1  | 38.9                | mA   |
|          |  |                             | 64 MHz     | 59.8                    | 66.4                | 67.7  | 68.6                | 29.7                     | 33.5                | 34.3  | 35.0                |      |
|          |  |                             | 48 MHz     | 47.3                    | 53.7                | 53.8  | 55.1                | 23.2                     | 26.2                | 27.1  | 28.0                |      |
|          |  |                             | 32 MHz     | 33.3                    | 36.8                | 37.4  | 38.5                | 16.8                     | 19.8                | 20.6  | 21.4                |      |
|          |  |                             | 24 MHz     | 26.0                    | 29.4                | 30.0  | 31.2                | 13.5                     | 16.6                | 17.4  | 18.6                |      |
|          |  |                             | 8 MHz      | 10.7                    | 13.8                | 14.4  | 15.3                | 6.63                     | 10.2                | 10.5  | 11.2                |      |
|          |  | Internal clock (HSI)        | 64 MHz     | 55.6                    | 59.6                | 62.8  | 63.2                | 29.4                     | 33.1                | 34.5  | 35.0                |      |
|          |  |                             | 48 MHz     | 43.6                    | 47.0                | 49.2  | 50.1                | 23.1                     | 26.2                | 27.1  | 28.0                |      |
|          |  |                             | 32 MHz     | 30.8                    | 33.6                | 35.3  | 35.8                | 16.7                     | 19.8                | 20.6  | 21.5                |      |
|          |  |                             | 24 MHz     | 24.0                    | 28.0                | 28.2  | 29.7                | 13.5                     | 16.5                | 17.5  | 18.4                |      |
| $I_{DD}$ | Supply current in Run mode, executing from RAM   | External clock (HSE bypass) | 72 MHz     | 66.2                    | 76.2 <sup>(2)</sup> | 76.7  | 77.2 <sup>(2)</sup> | 32.8                     | 36.9 <sup>(2)</sup> | 37.7  | 38.5 <sup>(2)</sup> |      |
|          |  |                             | 64 MHz     | 59.6                    | 66.2                | 67.6  | 68.4                | 29.3                     | 33.1                | 33.9  | 34.4                |      |
|          |  |                             | 48 MHz     | 47.0                    | 53.4                | 53.6  | 54.9                | 22.4                     | 25.6                | 26.2  | 27.2                |      |
|          |  |                             | 32 MHz     | 33.0                    | 36.6                | 37.2  | 38.1                | 16.0                     | 19.0                | 19.5  | 20.4                |      |
|          |  |                             | 24 MHz     | 25.6                    | 29.0                | 29.5  | 30.6                | 12.8                     | 15.7                | 16.3  | 17.6                |      |
|          |  |                             | 8 MHz      | 10.3                    | 13.4                | 13.8  | 14.7                | 6.40                     | 9.48                | 9.93  | 10.90               |      |

**Table 25. Typical and maximum current consumption from V<sub>DD</sub> supply at V<sub>DD</sub> = 3.6V (continued)**

| Symbol          | Parameter   | Conditions                  | f <sub>HCLK</sub> | All peripherals enabled |                                     |       |                     | All peripherals disabled |                                     |       |                     | Unit |
|-----------------|---|-----------------------------|-------------------|-------------------------|-------------------------------------|-------|---------------------|--------------------------|-------------------------------------|-------|---------------------|------|
|                 |   |                             |                   | Typ                     | Max @ T <sub>A</sub> <sup>(1)</sup> |       |                     | Typ                      | Max @ T <sub>A</sub> <sup>(1)</sup> |       |                     |      |
|                 |   |                             |                   |                         | 25 °C                               | 85 °C | 105 °C              |                          | 25 °C                               | 85 °C | 105 °C              |      |
| I <sub>DD</sub> | Supply current in Run mode, executing from RAM            | External clock (HSE bypass) | 1 MHz             | 3.92                    | 7.06                                | 7.54  | 8.60                | 3.42                     | 6.53                                | 7.05  | 8.10                | mA   |
|                 |   | Internal clock (HSI)        | 64 MHz            | 55.4                    | 59.2                                | 62.5  | 62.9                | 29.1                     | 32.7                                | 34.0  | 34.6                |      |
|                 |   |                             | 48 MHz            | 43.1                    | 46.7                                | 49.0  | 49.9                | 22.8                     | 26.1                                | 26.8  | 27.8                |      |
|                 |   |                             | 32 MHz            | 30.5                    | 33.2                                | 35.0  | 35.5                | 15.8                     | 18.8                                | 19.5  | 20.9                |      |
|                 |   |                             | 24 MHz            | 23.8                    | 27.8                                | 27.9  | 29.2                | 12.6                     | 15.6                                | 16.3  | 17.5                |      |
|                 |   |                             | 8 MHz             | 9.85                    | 13.1                                | 14.1  | 14.6                | 6.20                     | 9.37                                | 10.3  | 10.7                |      |
| I <sub>DD</sub> | Supply current in Sleep mode, executing from Flash or RAM | External clock (HSE bypass) | 72 MHz            | 48.8                    | 53.5 <sup>(2)</sup>                 | 53.6  | 54.0 <sup>(2)</sup> | 7.60                     | 8.20 <sup>(2)</sup>                 | 8.50  | 9.00 <sup>(2)</sup> |      |
|                 |   |                             | 64 MHz            | 43.5                    | 48.6                                | 49.1  | 49.3                | 6.90                     | 7.50                                | 7.80  | 8.00                |      |
|                 |   |                             | 48 MHz            | 33.6                    | 38.1                                | 40.0  | 41.3                | 5.30                     | 5.80                                | 6.00  | 6.40                |      |
|                 |   |                             | 32 MHz            | 24.3                    | 27.5                                | 28.1  | 29.3                | 3.80                     | 4.10                                | 4.40  | 4.70                |      |
|                 |   |                             | 24 MHz            | 18.6                    | 21.9                                | 22.4  | 22.6                | 2.90                     | 3.30                                | 3.40  | 3.90                |      |
|                 |   |                             | 8 MHz             | 8.24                    | 11.27                               | 11.79 | 12.70               | 1.36                     | 1.74                                | 1.85  | 2.00                |      |
|                 |   | Internal clock (HSI)        | 1 MHz             | 3.64                    | 6.72                                | 7.36  | 8.30                | 0.79                     | 1.17                                | 1.26  | 1.35                |      |
|                 |   |                             | 64 MHz            | 39.7                    | 43.9                                | 45.5  | 45.8                | 6.70                     | 7.30                                | 7.40  | 7.70                |      |
|                 |   |                             | 48 MHz            | 30.4                    | 33.9                                | 35.3  | 36.5                | 5.10                     | 5.60                                | 5.70  | 6.10                |      |
|                 |   |                             | 32 MHz            | 21.9                    | 25.8                                | 26.2  | 26.7                | 3.60                     | 4.10                                | 4.20  | 4.50                |      |
|                 |   |                             | 24 MHz            | 17.0                    | 20.2                                | 21.5  | 21.7                | 2.98                     | 3.41                                | 3.46  | 3.57                |      |
|                 |   |                             | 8 MHz             | 7.81                    | 11.0                                | 11.7  | 12.4                | 1.41                     | 1.74                                | 1.81  | 1.87                |      |

1. Data based on characterization results, not tested in production unless otherwise specified.

2. Data based on characterization results and tested in production with code executing from RAM.

**Table 26. Typical and maximum current consumption from the V<sub>DDA</sub> supply**

| Symbol           | Parameter  | Conditions <sup>(1)</sup> | f <sub>HCLK</sub> | V <sub>DDA</sub> = 2.4 V |                                     |       |        | V <sub>DDA</sub> = 3.6 V |                                     |       |        | Unit |
|------------------|--|---------------------------|-------------------|--------------------------|-------------------------------------|-------|--------|--------------------------|-------------------------------------|-------|--------|------|
|                  |  |                           |                   | Typ                      | Max @ T <sub>A</sub> <sup>(2)</sup> |       |        | Typ                      | Max @ T <sub>A</sub> <sup>(2)</sup> |       |        |      |
|                  |  |                           |                   |                          | 25 °C                               | 85 °C | 105 °C |                          | 25 °C                               | 85 °C | 105 °C |      |
| I <sub>DDA</sub> | Supply current in Run mode, code executing from Flash or RAM | HSE bypass                | 72 MHz            | 220                      | 243                                 | 255   | 260    | 241                      | 264                                 | 281   | 287    | µA   |
|                  |  |                           | 64 MHz            | 194                      | 215                                 | 226   | 231    | 212                      | 233                                 | 248   | 254    |      |
|                  |  |                           | 48 MHz            | 145                      | 164                                 | 172   | 176    | 158                      | 176                                 | 187   | 192    |      |
|                  |  |                           | 32 MHz            | 100                      | 116                                 | 121   | 124    | 108                      | 123                                 | 130   | 134    |      |
|                  |  |                           | 24 MHz            | 78                       | 92                                  | 96    | 98     | 85                       | 97                                  | 102   | 105    |      |
|                  |  |                           | 8 MHz             | 1.9                      | 3.1                                 | 3.6   | 4.4    | 2.5                      | 3.7                                 | 4.4   | 5.5    |      |



**Table 26. Typical and maximum current consumption from the V<sub>DDA</sub> supply (continued)**

| Symbol           | Parameter  | Conditions (1) | f <sub>HCLK</sub> | V <sub>DDA</sub> = 2.4 V |                          |       |        | V <sub>DDA</sub> = 3.6 V |                          |       |        | Unit |
|------------------|--|----------------|-------------------|--------------------------|--------------------------|-------|--------|--------------------------|--------------------------|-------|--------|------|
|                  |  |                |                   | Typ                      | Max @ T <sub>A</sub> (2) |       |        | Typ                      | Max @ T <sub>A</sub> (2) |       |        |      |
|                  |  |                |                   |                          | 25 °C                    | 85 °C | 105 °C |                          | 25 °C                    | 85 °C | 105 °C |      |
| I <sub>DDA</sub> | Supply current in Run mode, code executing from Flash or RAM | HSE bypass     | 1 MHz             | 1.9                      | 3.1                      | 3.6   | 4.4    | 2.5                      | 3.7                      | 4.4   | 5.5    | μA   |
|                  |  | HSI clock      | 64 MHz            | 266                      | 290                      | 301   | 306    | 295                      | 320                      | 335   | 341    |      |
|                  | 48 MHz   |                | 216               | 237                      | 247                      | 251   | 240    | 262                      | 274                      | 279   |        |      |
|                  | 32 MHz   |                | 170               | 188                      | 196                      | 199   | 190    | 208                      | 217                      | 221   |        |      |
|                  | 24 MHz   |                | 148               | 164                      | 170                      | 172   | 166    | 182                      | 189                      | 192   |        |      |
|                  | 8 MHz  | 70             | 78                | 81                       | 82                       | 84    | 92     | 95                       | 97                       |       |        |      |

1. Current consumption from the V<sub>DDA</sub> supply is independent of whether the peripherals are on or off. Furthermore when the PLL is off, I<sub>DDA</sub> is independent from the frequency.
2. Data based on characterization results, not tested in production.

**Table 27. Typical and maximum V<sub>DD</sub> consumption in Stop and Standby modes**

| Symbol   | Parameter            | Conditions | Typ @V <sub>DD</sub> (V <sub>DD</sub> =V <sub>DDA</sub> ) |                             |  |       |       |       | Max                    |                        |                         | Unit |
|--|----------------------|------------|---|-----------------------------|--|-------|-------|-------|------------------------|------------------------|-------------------------|------|
|  |                      |            | 2.0 V   | 2.4 V                       | 2.7 V                                      | 3.0 V | 3.3 V | 3.6 V | T <sub>A</sub> = 25 °C | T <sub>A</sub> = 85 °C | T <sub>A</sub> = 105 °C |      |
|  |                      |            | I <sub>DD</sub>   | Supply current in Stop mode | Regulator in run mode, all oscillators OFF | 18.4  | 18.7  | 18.8  | 18.9                   | 19.0                   | 19.1                    |      |
| Regulator in low-power mode, all oscillators OFF | 6.80                 | 6.94       |   |                             | 7.11                                       | 7.18  | 7.26  | 7.39  | 33                     | 408                    | 898                     |      |
| Supply current in Standby mode                   | LSI ON and IWDG ON   | 0.72       |   | 0.87                        | 0.99                                       | 1.10  | 1.23  | 1.37  | -                      | -                      | -                       |      |
|  | LSI OFF and IWDG OFF | 0.57       |   | 0.68                        | 0.76                                       | 0.85  | 0.94  | 1.03  | 6.2                    | 8.6                    | 13.5                    |      |

**Table 28. Typical and maximum  $V_{DDA}$  consumption in Stop and Standby modes**

| Symbol    | Parameter                      | Conditions   | Typ @ $V_{DD}$ ( $V_{DD} = V_{DDA}$ ) |       |       |       |       |       | Max <sup>(1)</sup>       |                          |                           | Unit          |
|-----------|--------------------------------|--|---------------------------------------|-------|-------|-------|-------|-------|--------------------------|--------------------------|---------------------------|---------------|
|           |                                |  | 2.0 V                                 | 2.4 V | 2.7 V | 3.0 V | 3.3 V | 3.6 V | $T_A = 25^\circ\text{C}$ | $T_A = 85^\circ\text{C}$ | $T_A = 105^\circ\text{C}$ |               |
| $I_{DDA}$ | Supply current in Stop mode    | $V_{DDA}$ supervisor ON<br>Regulator in run/low-power mode, all oscillators OFF  | 1.72                                  | 1.85  | 1.97  | 2.10  | 2.25  | 2.41  | 10.7                     | 11                       | 12                        | $\mu\text{A}$ |
|           | Supply current in Standby mode | $V_{DDA}$ supervisor ON<br>LSI ON and IWDG ON                                    | 2.08                                  | 2.26  | 2.43  | 2.61  | 2.82  | 3.05  | -                        | -                        | -                         |               |
|           |                                | $V_{DDA}$ supervisor OFF<br>LSI OFF and IWDG OFF                                 | 1.60                                  | 1.73  | 1.85  | 1.98  | 2.13  | 2.29  | 3.6                      | 4                        | 6                         |               |
|           | Supply current in Stop mode    | $V_{DDA}$ supervisor OFF<br>Regulator in run/low-power mode, all oscillators OFF | 1.00                                  | 1.02  | 1.05  | 1.10  | 1.16  | 1.24  | -                        | -                        | -                         |               |
|           | Supply current in Standby mode | $V_{DDA}$ supervisor ON<br>LSI ON and IWDG ON                                    | 1.36                                  | 1.43  | 1.51  | 1.61  | 1.74  | 1.88  | -                        | -                        | -                         |               |
|           |                                | $V_{DDA}$ supervisor OFF<br>LSI OFF and IWDG OFF                                 | 0.88                                  | 0.90  | 0.93  | 0.98  | 1.05  | 1.12  | -                        | -                        | -                         |               |

1. Data based on characterization results, not tested in production.

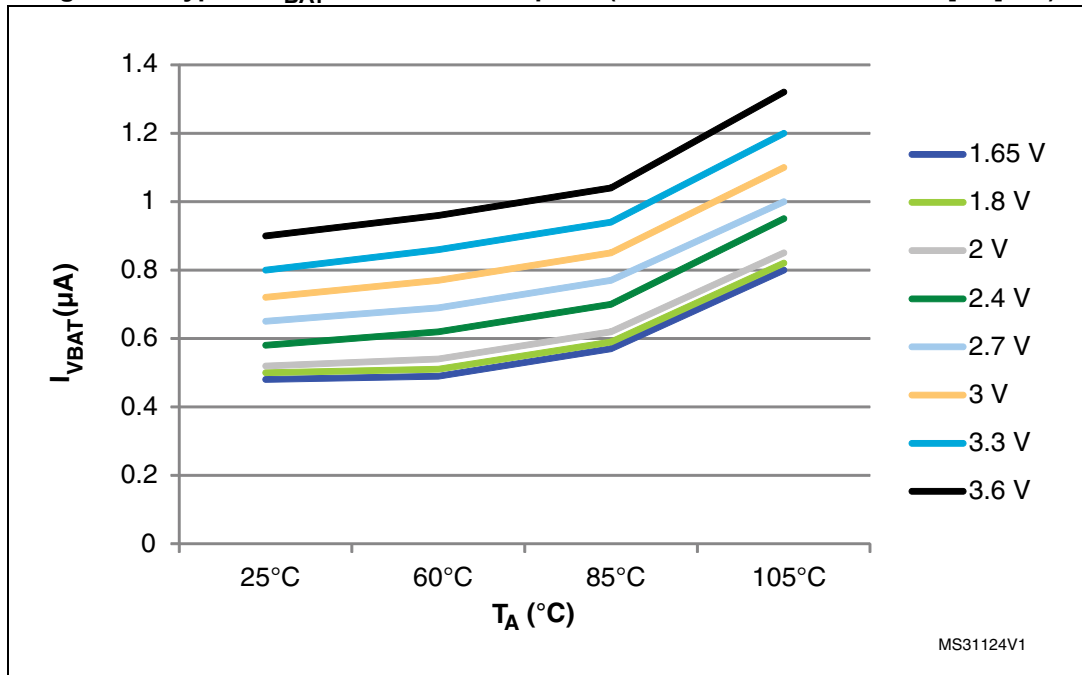
**Table 29. Typical and maximum current consumption from  $V_{BAT}$  supply**

| Symbol         | Parameter                    | Conditions <sup>(1)</sup>   | Typ @ $V_{BAT}$ |      |      |      |      |      |      |      | Max @ $V_{BAT} = 3.6\text{ V}^{(2)}$ |                          |                           | Unit          |
|----------------|------------------------------|---|-----------------|------|------|------|------|------|------|------|--------------------------------------|--------------------------|---------------------------|---------------|
|                |                              |   | 1.65V           | 1.8V | 2V   | 2.4V | 2.7V | 3V   | 3.3V | 3.6V | $T_A = 25^\circ\text{C}$             | $T_A = 85^\circ\text{C}$ | $T_A = 105^\circ\text{C}$ |               |
| $I_{DD\_VBAT}$ | Backup domain supply current | LSE & RTC ON; "Xtal mode" lower driving capability; LSEDRV[1:0] = '00'  | 0.48            | 0.50 | 0.52 | 0.58 | 0.65 | 0.72 | 0.80 | 0.90 | 1.1                                  | 1.5                      | 2.0                       | $\mu\text{A}$ |
|                |                              | LSE & RTC ON; "Xtal mode" higher driving capability; LSEDRV[1:0] = '11' | 0.83            | 0.86 | 0.90 | 0.98 | 1.03 | 1.10 | 1.20 | 1.30 | 1.5                                  | 2.2                      | 2.9                       |               |

1. Crystal used: Abracon ABS07-120-32.768 kHz-T with a CL of 6 pF for typical values.

2. Data based on characterization results, not tested in production.

Figure 14. Typical  $V_{BAT}$  current consumption (LSE and RTC ON/LSEDRV[1:0] 00')



**Typical current consumption**

The MCU is placed under the following conditions:

- $V_{DD} = V_{DDA} = 3.3 V$
- All I/O pins available on each package are in analog input configuration
- The Flash access time is adjusted to  $f_{HCLK}$  frequency (0 wait states from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states from 48 MHz to 72 MHz), and Flash prefetch is ON
- When the peripherals are enabled,  $f_{APB1} = f_{AHB}/2$ ,  $f_{APB2} = f_{AHB}$
- PLL is used for frequencies greater than 8 MHz
- AHB prescaler of 2, 4, 8, 16 and 64 is used for the frequencies 4 MHz, 2 MHz, 1 MHz, 500 kHz and 125 kHz respectively.

**Table 30. Typical current consumption in Run mode, code with data processing running from Flash**

| Symbol   | Parameter  | Conditions  | f <sub>HCLK</sub> | Typ                 |                      | Unit |
|--|--|---|-------------------|---------------------|----------------------|------|
|  |  |   |                   | Peripherals enabled | Peripherals disabled |      |
| I <sub>DD</sub>                                | Supply current in Run mode from V <sub>DD</sub> supply             | Running from HSE crystal clock 8 MHz, code executing from Flash | 72 MHz            | 60.7                | 27.3                 | mA   |
|  |  |   | 64 MHz            | 54.3                | 24.1                 |      |
|  |  |   | 48 MHz            | 42.1                | 19.4                 |      |
|  |  |   | 32 MHz            | 28.7                | 13.9                 |      |
|  |  |   | 24 MHz            | 22.2                | 11.0                 |      |
|  |  |   | 16 MHz            | 15.4                | 7.9                  |      |
|  |  |   | 8 MHz             | 8.3                 | 4.51                 |      |
|  |  |   | 4 MHz             | 5.14                | 3.02                 |      |
|  |  |   | 2 MHz             | 3.37                | 2.21                 |      |
|  |  |   | 1 MHz             | 2.49                | 1.80                 |      |
|  |  |   |                   | 500 kHz             | 2.04                 |      |
|  | 125 kHz  | 1.71  | 0.84              |                     |                      |      |
| I <sub>D<sub>DA</sub></sub> <sup>(1) (2)</sup> | Supply current in Run mode from V <sub>D<sub>DA</sub></sub> supply | Running from HSE crystal clock 8 MHz, code executing from Flash | 72 MHz            | 239.7               |                      | μA   |
|  |  |   | 64 MHz            | 210.5               |                      |      |
|  |  |   | 48 MHz            | 155.6               |                      |      |
|  |  |   | 32 MHz            | 105.5               |                      |      |
|  |  |   | 24 MHz            | 81.9                |                      |      |
|  |  |   | 16 MHz            | 58.6                |                      |      |
|  |  |   | 8 MHz             | 1.16                |                      |      |
|  |  |   | 4 MHz             | 1.16                |                      |      |
|  |  |   | 2 MHz             | 1.16                |                      |      |
|  |  |   | 1 MHz             | 1.16                |                      |      |
|  |  |   |                   | 500 kHz             | 1.16                 |      |
|  | 125 kHz  | 1.16  |                   |                     |                      |      |

1. V<sub>D<sub>DA</sub></sub> supervisor is OFF.
2. When peripherals are enabled, the power consumption of the analog part of peripherals such as ADC, DAC, Comparators, OpAmp is not included. Refer to the tables of characteristics in the subsequent sections.

**Table 31. Typical current consumption in Sleep mode, code running from Flash or RAM**

| Symbol                              | Parameter   | Conditions   | f <sub>HCLK</sub> | Typ                 |                      | Unit |
|-------------------------------------|---|--|-------------------|---------------------|----------------------|------|
|                                     |   |  |                   | Peripherals enabled | Peripherals disabled |      |
| I <sub>DD</sub>                     | Supply current in Sleep mode from V <sub>DD</sub> supply  | Running from HSE crystal clock 8 MHz, code executing from Flash or RAM | 72 MHz            | 43.0                | 7.4                  | mA   |
|                                     |   |  | 64 MHz            | 38.3                | 6.8                  |      |
|                                     |   |  | 48 MHz            | 29.0                | 5.29                 |      |
|                                     |   |  | 32 MHz            | 19.7                | 3.91                 |      |
|                                     |   |  | 24 MHz            | 15.2                | 3.19                 |      |
|                                     |   |  | 16 MHz            | 10.8                | 2.46                 |      |
|                                     |   |  | 8 MHz             | 5.85                | 1.55                 |      |
|                                     |   |  | 4 MHz             | 3.80                | 1.45                 |      |
|                                     |   |  | 2 MHz             | 2.67                | 1.32                 |      |
|                                     |   |  | 1 MHz             | 2.12                | 1.22                 |      |
|                                     |   |  | 500 kHz           | 1.83                | 1.19                 |      |
| 125 kHz                             | 1.60  | 0.83   |                   |                     |                      |      |
| I <sub>DDA</sub> <sup>(1) (2)</sup> | Supply current in Sleep mode from V <sub>DDA</sub> supply | Running from HSE crystal clock 8 MHz, code executing from Flash or RAM | 72 MHz            | 239.7               |                      | μA   |
|                                     |   |  | 64 MHz            | 210.5               |                      |      |
|                                     |   |  | 48 MHz            | 155.6               |                      |      |
|                                     |   |  | 32 MHz            | 105.5               |                      |      |
|                                     |   |  | 24 MHz            | 81.9                |                      |      |
|                                     |   |  | 16 MHz            | 58.6                |                      |      |
|                                     |   |  | 8 MHz             | 1.16                |                      |      |
|                                     |   |  | 4 MHz             | 1.16                |                      |      |
|                                     |   |  | 2 MHz             | 1.16                |                      |      |
|                                     |   |  | 1 MHz             | 1.16                |                      |      |
|                                     |   |  | 500 kHz           | 1.16                |                      |      |
| 125 kHz                             | 1.16  |  |                   |                     |                      |      |

1. V<sub>DDA</sub> supervisor is OFF.
2. When peripherals are enabled, the power consumption of the analog part of peripherals such as ADC, DAC, Comparators, OpAmp is not included. Refer to the tables of characteristics in the subsequent sections.

## I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

### I/O static current consumption

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in [Table 66: I/O static characteristics](#).

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

**Caution:** Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

### I/O dynamic current consumption

In addition to the internal peripheral current consumption (see [Table 33: Peripheral current consumption](#)), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the MCU supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DD} \times f_{SW} \times C$$

where:

$I_{SW}$  is the current sunk by a switching I/O to charge/discharge the capacitive load

$V_{DD}$  is the MCU supply voltage

$f_{SW}$  is the I/O switching frequency

$C$  is the total capacitance seen by the I/O pin:  $C = C_{INT} + C_{EXT} + C_S$

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

Table 32. Switching output I/O current consumption

| Symbol   | Parameter               | Conditions <sup>(1)</sup>  | I/O toggling frequency (f <sub>SW</sub> ) | Typ  | Unit |
|--|-------------------------|--|---|------|------|
| I <sub>sw</sub>  | I/O current consumption | $V_{DD} = 3.3\text{ V}$<br>$C_{ext} = 0\text{ pF}$<br>$C = C_{INT} + C_{EXT} + C_S$  | 2 MHz                                     | 0.90 | mA   |
|  |                         |  | 4 MHz                                     | 0.93 |      |
|  |                         |  | 8 MHz                                     | 1.16 |      |
|  |                         |  | 18 MHz                                    | 1.60 |      |
|  |                         |  | 36 MHz                                    | 2.51 |      |
|  |                         |  | 48 MHz                                    | 2.97 |      |
|  |                         | $V_{DD} = 3.3\text{ V}$<br>$C_{ext} = 10\text{ pF}$<br>$C = C_{INT} + C_{EXT} + C_S$ | 2 MHz                                     | 0.93 |      |
|  |                         |  | 4 MHz                                     | 1.06 |      |
|  |                         |  | 8 MHz                                     | 1.47 |      |
|  |                         |  | 18 MHz                                    | 2.26 |      |
|  |                         |  | 36 MHz                                    | 3.39 |      |
|  |                         |  | 48 MHz                                    | 5.99 |      |
|  |                         | $V_{DD} = 3.3\text{ V}$<br>$C_{ext} = 22\text{ pF}$<br>$C = C_{INT} + C_{EXT} + C_S$ | 2 MHz                                     | 1.03 |      |
|  |                         |  | 4 MHz                                     | 1.30 |      |
|  |                         |  | 8 MHz                                     | 1.79 |      |
|  |                         |  | 18 MHz                                    | 3.01 |      |
|  |                         |  | 36 MHz                                    | 5.99 |      |
|  |                         | $V_{DD} = 3.3\text{ V}$<br>$C_{ext} = 33\text{ pF}$<br>$C = C_{INT} + C_{EXT} + C_S$ | 2 MHz                                     | 1.10 |      |
|  |                         |  | 4 MHz                                     | 1.31 |      |
|  |                         |  | 8 MHz                                     | 2.06 |      |
| 18 MHz   | 3.47                    |  |   |      |      |
| $V_{DD} = 3.3\text{ V}$<br>$C_{ext} = 47\text{ pF}$<br>$C = C_{INT} + C_{EXT} + C_S$ | 36 MHz                  | 8.35   |   |      |      |
|  | 2 MHz                   | 1.20   |   |      |      |
|  | 4 MHz                   | 1.54   |   |      |      |
|  | 8 MHz                   | 2.46   |   |      |      |
|  |                         |  | 18 MHz                                    | 4.51 |      |
|  |                         |  | 36 MHz                                    | 9.98 |      |

1. CS = 5 pF (estimated value).

**On-chip peripheral current consumption**

The MCU is placed under the following conditions:

- all I/O pins are in analog input configuration
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
- ambient operating temperature at 25°C and  $V_{DD} = V_{DDA} = 3.3\text{ V}$ .

**Table 33. Peripheral current consumption**

| Peripheral                 | Typical consumption <sup>(1)</sup> | Unit   |
|----------------------------|------------------------------------|--------|
|                            | I <sub>DD</sub>                    |        |
| BusMatrix <sup>(2)</sup>   | 8.3                                | μA/MHz |
| DMA1                       | 7.0                                |        |
| DMA2                       | 5.4                                |        |
| FSMC                       | 35.0                               |        |
| CRC                        | 1.5                                |        |
| GPIOH                      | 1.3                                |        |
| GPIOA                      | 5.4                                |        |
| GPIOB                      | 5.3                                |        |
| GPIOC                      | 5.4                                |        |
| GIOD                       | 5.0                                |        |
| GPIOE                      | 5.4                                |        |
| GPIOF                      | 5.2                                |        |
| GPIOG                      | 5.0                                |        |
| TSC                        | 5.2                                |        |
| ADC1&2                     | 15.4                               |        |
| APB2-Bridge <sup>(3)</sup> | 3.1                                |        |
| SYSCFG                     | 4.0                                |        |
| TIM1                       | 26.0                               |        |
| USART1                     | 17.7                               |        |
| SPI4                       | 6.2                                |        |
| TIM15                      | 11.9                               |        |
| TIM16                      | 8.0                                |        |
| TIM17                      | 8.5                                |        |



**Table 33. Peripheral current consumption (continued)**

| Peripheral                 | Typical consumption <sup>(1)</sup> | Unit   |
|----------------------------|------------------------------------|--------|
|                            | I <sub>DD</sub>                    |        |
| APB1-Bridge <sup>(3)</sup> | 6.7                                | μA/MHz |
| TIM2                       | 39.2                               |        |
| TIM3                       | 30.8                               |        |
| TIM4                       | 31.3                               |        |
| TIM6                       | 4.3                                |        |
| WWDG                       | 1.3                                |        |
| SPI2                       | 33.6                               |        |
| SPI3                       | 33.9                               |        |
| USART2                     | 39.3                               |        |
| USART3                     | 39.3                               |        |
| UART4                      | 29.8                               |        |
| UART5                      | 27.0                               |        |
| I2C1                       | 6.7                                |        |
| I2C2                       | 6.4                                |        |
| USB                        | 14.7                               |        |
| CAN                        | 25.6                               |        |
| PWR                        | 3.7                                |        |
| DAC                        | 22.1                               |        |
| I2C3                       | 6.8                                |        |

1. The power consumption of the analog part (I<sub>DDA</sub>) of peripherals such as ADC, DAC, Comparators, OpAmp is not included. Refer to the tables of characteristics in the subsequent sections.
2. BusMatrix is automatically active when at least one master is ON (CPU, DMA1 or DMA2).
3. The APBx bridge is automatically active when at least one peripheral is ON on the same bus.

### 6.3.6 Wakeup time from low-power mode

The wakeup times given in [Table 34](#) are measured starting from the wakeup event trigger up to the first instruction executed by the CPU:

- For Stop or Sleep mode: the wakeup event is WFE.
- WKUP1 (PA0) pin is used to wake up from Standby, Stop and Sleep modes.

All timings are derived from tests performed under ambient temperature and  $V_{DD}$  supply voltage conditions summarized in [Table 19](#).

**Table 34. Low-power mode wakeup timings**

| Symbol                                | Parameter                | Conditions                  | Typ @V <sub>DD</sub> , V <sub>DD</sub> = V <sub>DDA</sub> |       |       |      |       |       | Max  | Unit             |
|---------------------------------------|--------------------------|-----------------------------|---|-------|-------|------|-------|-------|------|------------------|
|                                       |                          |                             | 2.0 V   | 2.4 V | 2.7 V | 3 V  | 3.3 V | 3.6 V |      |                  |
| t <sub>WUSTOP</sub>                   | Wakeup from Stop mode    | Regulator in run mode       | 5.4   | 5.2   | 5.2   | 5.1  | 5.0   | 4.9   | 5.6  | μs               |
|                                       |                          | Regulator in low power mode | 12.0  | 10.1  | 9.2   | 8.6  | 8.1   | 7.8   | 12.9 |                  |
| t <sub>WUSTANDBY</sub> <sup>(1)</sup> | Wakeup from Standby mode | LSI and IWDG OFF            | 91.0  | 77.1  | 71.7  | 68.0 | 65.1  | 63.1  | 139  |                  |
| t <sub>WUSLEEP</sub>                  | Wakeup from Sleep mode   | -                           | 6   |       |       |      |       |       | -    | CPU clock cycles |

1. Data based on characterization results, not tested in production.

**Table 35. Wakeup time using USART**

| Symbol               | Parameter  | Conditions                                      | Typ | Max    | Unit |
|----------------------|--|---|-----|--------|------|
| t <sub>WUUSART</sub> | Wakeup time needed to calculate the maximum USART baudrate allowing to wakeup up from stop mode when USART clock source is HSI | Stop mode with main regulator in low power mode | -   | 13.125 | μs   |
|                      |  | Stop mode with main regulator in run mode       | -   | 3.125  |      |

### 6.3.7 External clock source characteristics

#### High-speed external user clock generated from an external source

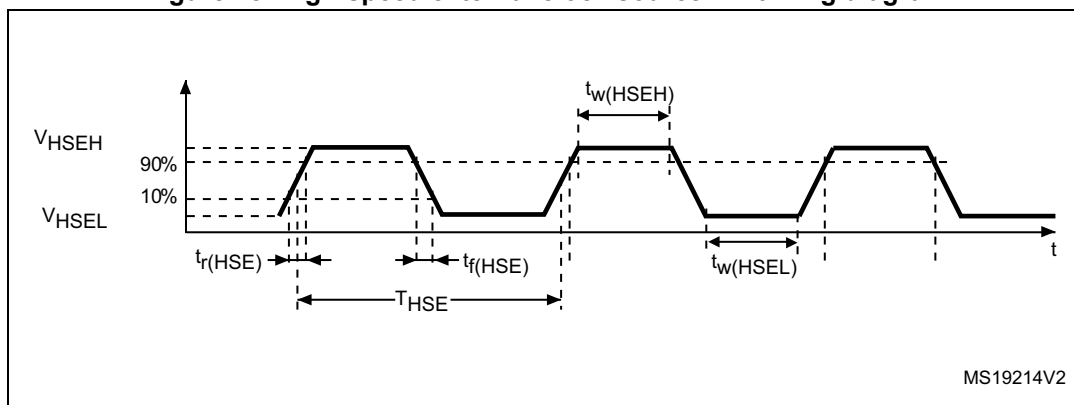
In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO. The external clock signal has to respect the I/O characteristics in [Section 6.3.15](#). However, the recommended clock input waveform is shown in [Figure 15](#).

**Table 36. High-speed external user clock characteristics**

| Symbol                         | Parameter   | Conditions | Min         | Typ | Max         | Unit |
|--------------------------------|---|------------|-------------|-----|-------------|------|
| $f_{HSE\_ext}$                 | User external clock source frequency <sup>(1)</sup> | -          | 1           | 8   | 32          | MHz  |
| $V_{HSEH}$                     | OSC_IN input pin high level voltage                 | -          | $0.7V_{DD}$ | -   | $V_{DD}$    | V    |
| $V_{HSEL}$                     | OSC_IN input pin low level voltage                  | -          | $V_{SS}$    | -   | $0.3V_{DD}$ |      |
| $t_{w(HSEH)}$<br>$t_{w(HSEL)}$ | OSC_IN high or low time <sup>(1)</sup>              | -          | 15          | -   | -           | ns   |
| $t_r(HSE)$<br>$t_f(HSE)$       | OSC_IN rise or fall time <sup>(1)</sup>             | -          | -           | -   | 20          |      |

1. Guaranteed by design, not tested in production.

**Figure 15. High-speed external clock source AC timing diagram**



#### Low-speed external user clock generated from an external source

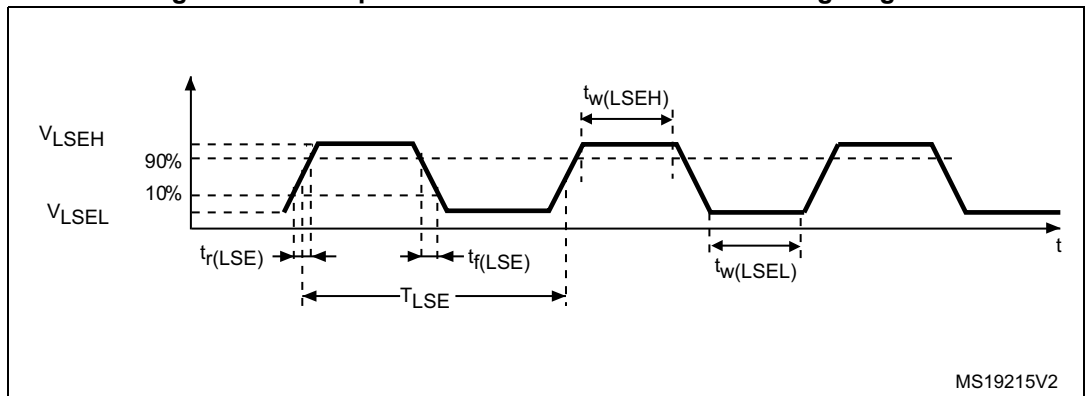
In bypass mode the LSE oscillator is switched off and the input pin is a standard GPIO. The external clock signal has to respect the I/O characteristics in [Section 6.3.15](#). However, the recommended clock input waveform is shown in [Figure 16](#).

Table 37. Low-speed external user clock characteristics

| Symbol                         | Parameter   | Conditions | Min         | Typ    | Max         | Unit |
|--------------------------------|---|------------|-------------|--------|-------------|------|
| $f_{LSE\_ext}$                 | User External clock source frequency <sup>(1)</sup> |            | -           | 32.768 | 1000        | kHz  |
| $V_{LSEH}$                     | OSC32_IN input pin high level voltage               | -          | $0.7V_{DD}$ | -      | $V_{DD}$    | V    |
| $V_{LSEL}$                     | OSC32_IN input pin low level voltage                |            | $V_{SS}$    | -      | $0.3V_{DD}$ |      |
| $t_{w(LSEH)}$<br>$t_{w(LSEL)}$ | OSC32_IN high or low time <sup>(1)</sup>            |            | 450         | -      | -           | ns   |
| $t_{r(LSE)}$<br>$t_{f(LSE)}$   | OSC32_IN rise or fall time <sup>(1)</sup>           | -          | -           | 50     |             |      |

1. Guaranteed by design, not tested in production.

Figure 16. Low-speed external clock source AC timing diagram



**High-speed external clock generated from a crystal/ceramic resonator**

The high-speed external (HSE) clock can be supplied with a 4 to 32 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in [Table 38](#). In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

**Table 38. HSE oscillator characteristics**

| Symbol                              | Parameter                   | Conditions <sup>(1)</sup>                                      | Min <sup>(2)</sup> | Typ | Max <sup>(2)</sup> | Unit |
|-------------------------------------|-----------------------------|--|--------------------|-----|--------------------|------|
| f <sub>OSC_IN</sub>                 | Oscillator frequency        | -  | 4                  | 8   | 32                 | MHz  |
| R <sub>F</sub>                      | Feedback resistor           | -  | -                  | 200 | -                  | kΩ   |
| I <sub>DD</sub>                     | HSE current consumption     | During startup <sup>(3)</sup>                                  | -                  | -   | 8.5                | mA   |
|                                     |                             | V <sub>DD</sub> = 3.3 V, R <sub>m</sub> = 30Ω, CL=10 pF@8 MHz  | -                  | 0.4 | -                  |      |
|                                     |                             | V <sub>DD</sub> = 3.3 V, R <sub>m</sub> = 45Ω, CL=10 pF@8 MHz  | -                  | 0.5 | -                  |      |
|                                     |                             | V <sub>DD</sub> = 3.3 V, R <sub>m</sub> = 30Ω, CL=5 pF@32 MHz  | -                  | 0.8 | -                  |      |
|                                     |                             | V <sub>DD</sub> = 3.3 V, R <sub>m</sub> = 30Ω, CL=10 pF@32 MHz | -                  | 1   | -                  |      |
|                                     |                             | V <sub>DD</sub> = 3.3 V, R <sub>m</sub> = 30Ω, CL=20 pF@32 MHz | -                  | 1.5 | -                  |      |
| g <sub>m</sub>                      | Oscillator transconductance | Startup  | 10                 | -   | -                  | mA/V |
| t <sub>SU(HSE)</sub> <sup>(4)</sup> | Startup time                | V <sub>DD</sub> is stabilized                                  | -                  | 2   | -                  | ms   |

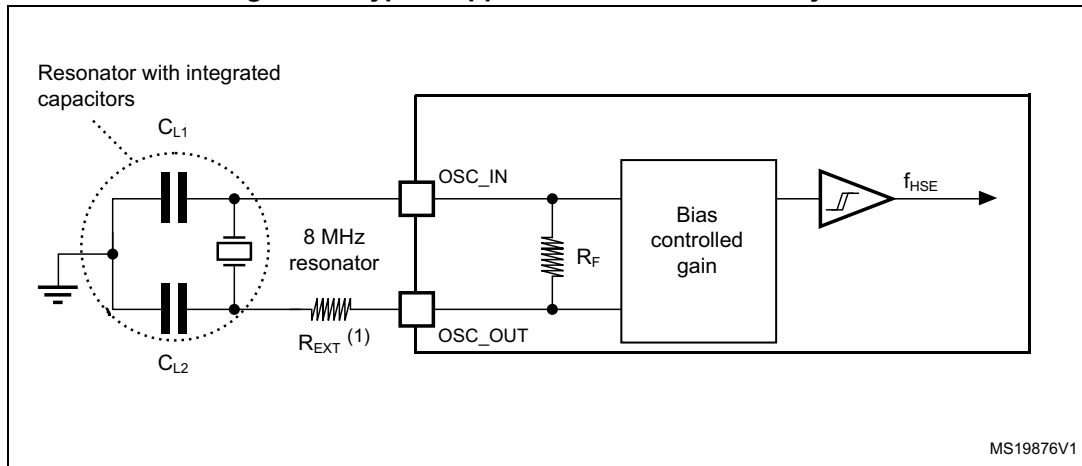
1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Guaranteed by design, not tested in production.
3. This consumption level occurs during the first 2/3 of the t<sub>SU(HSE)</sub> startup time.
4. t<sub>SU(HSE)</sub> is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

For C<sub>L1</sub> and C<sub>L2</sub>, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (Typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see [Figure 17](#)). C<sub>L1</sub> and C<sub>L2</sub> are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C<sub>L1</sub> and C<sub>L2</sub>. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C<sub>L1</sub> and C<sub>L2</sub>.

*Note:* For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website [www.st.com](http://www.st.com).



Figure 17. Typical application with an 8 MHz crystal



1.  $R_{EXT}$  value depends on the crystal characteristics.

**Low-speed external clock generated from a crystal/ceramic resonator**

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in Table 39. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

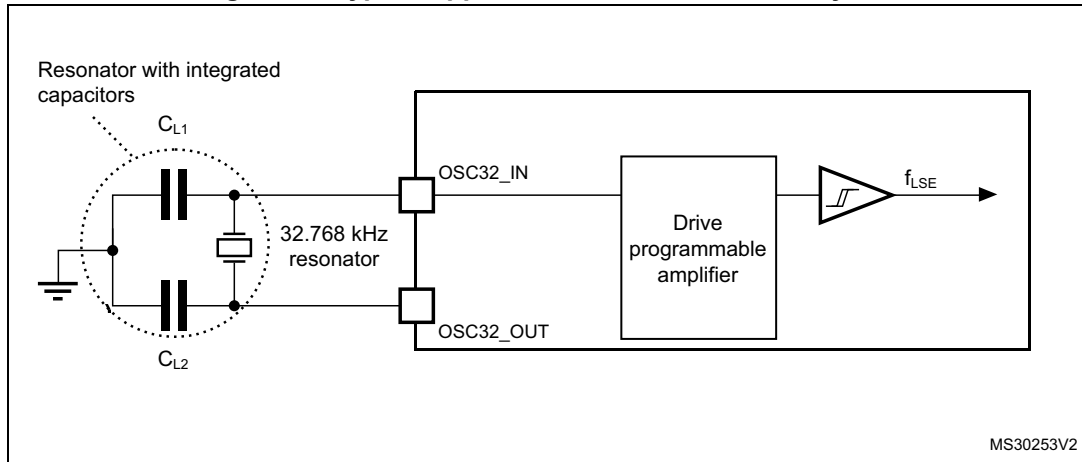
Table 39. LSE oscillator characteristics ( $f_{LSE} = 32.768$  kHz)

| Symbol                       | Parameter                   | Conditions <sup>(1)</sup>                        | Min <sup>(2)</sup> | Typ | Max <sup>(2)</sup> | Unit      |
|------------------------------|-----------------------------|--|--------------------|-----|--------------------|-----------|
| $I_{DD}$                     | LSE current consumption     | LSEDRV[1:0]=00<br>lower driving capability       | -                  | 0.5 | 0.9                | $\mu A$   |
|                              |                             | LSEDRV[1:0]=01<br>medium low driving capability  | -                  | -   | 1                  |           |
|                              |                             | LSEDRV[1:0]=10<br>medium high driving capability | -                  | -   | 1.3                |           |
|                              |                             | LSEDRV[1:0]=11<br>higher driving capability      | -                  | -   | 1.6                |           |
| $g_m$                        | Oscillator transconductance | LSEDRV[1:0]=00<br>lower driving capability       | 5                  | -   | -                  | $\mu A/V$ |
|                              |                             | LSEDRV[1:0]=01<br>medium low driving capability  | 8                  | -   | -                  |           |
|                              |                             | LSEDRV[1:0]=10<br>medium high driving capability | 15                 | -   | -                  |           |
|                              |                             | LSEDRV[1:0]=11<br>higher driving capability      | 25                 | -   | -                  |           |
| $t_{SU(LSE)}$ <sup>(3)</sup> | Startup time                | $V_{DD}$ is stabilized                           | -                  | 2   | -                  | s         |

1. Refer to the note and caution paragraphs below the table, and to the application note AN2867 "Oscillator design guide for ST microcontrollers".
2. Guaranteed by design, not tested in production.
3.  $t_{SU(LSE)}$  is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer.

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website [www.st.com](http://www.st.com).

Figure 18. Typical application with a 32.768 kHz crystal



Note: An external resistor is not required between OSC32\_IN and OSC32\_OUT and it is forbidden to add one.

### 6.3.8 Internal clock source characteristics

The parameters given in Table 40 are derived from tests performed under ambient temperature and supply voltage conditions summarized in Table 19.

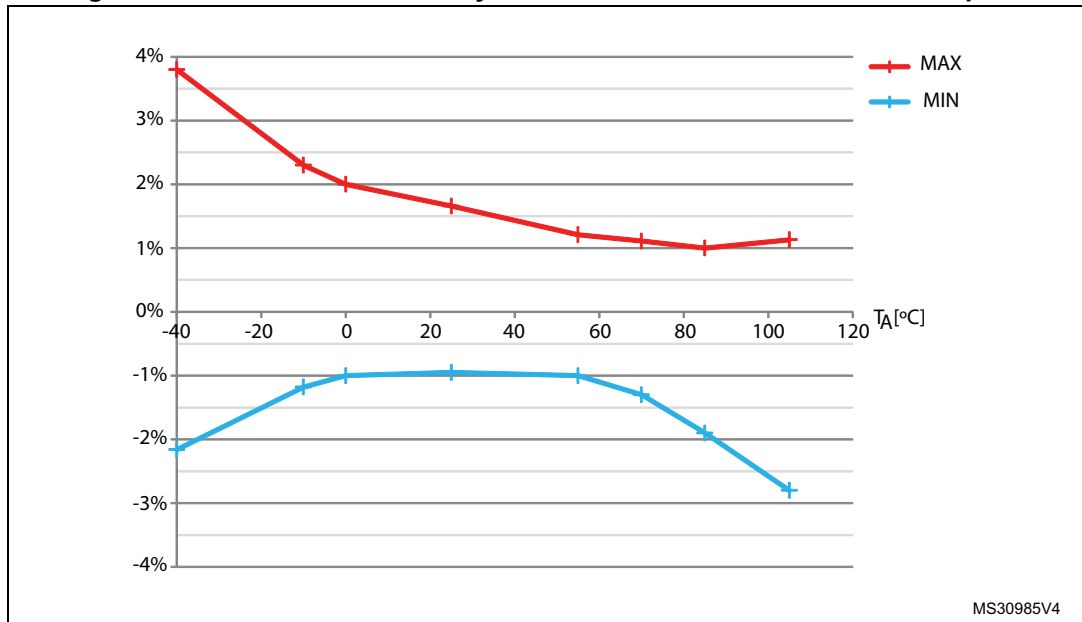
#### High-speed internal (HSI) RC oscillator

Table 40. HSI oscillator characteristics<sup>(1)</sup>

| Symbol                | Parameter                        | Conditions                                | Min                 | Typ | Max                | Unit          |
|-----------------------|----------------------------------|---|---------------------|-----|--------------------|---------------|
| $f_{\text{HSI}}$      | Frequency                        | -   | -                   | 8   | -                  | MHz           |
| TRIM                  | HSI user trimming step           | -   | -                   | -   | 1 <sup>(2)</sup>   | %             |
| DuCy <sub>(HSI)</sub> | Duty cycle                       | -   | 45 <sup>(2)</sup>   | -   | 55 <sup>(2)</sup>  | %             |
| ACC <sub>HSI</sub>    | Accuracy of the HSI oscillator   | $T_A = -40 \text{ to } 105^\circ\text{C}$ | -2.8 <sup>(3)</sup> | -   | 3.8 <sup>(3)</sup> | %             |
|                       |                                  | $T_A = -10 \text{ to } 85^\circ\text{C}$  | -1.9 <sup>(3)</sup> | -   | 2.3 <sup>(3)</sup> |               |
|                       |                                  | $T_A = 0 \text{ to } 85^\circ\text{C}$    | -1.9 <sup>(3)</sup> | -   | 2 <sup>(3)</sup>   |               |
|                       |                                  | $T_A = 0 \text{ to } 70^\circ\text{C}$    | -1.3 <sup>(3)</sup> | -   | 2 <sup>(3)</sup>   |               |
|                       |                                  | $T_A = 0 \text{ to } 55^\circ\text{C}$    | -1 <sup>(3)</sup>   | -   | 2 <sup>(3)</sup>   |               |
|                       |                                  | $T_A = 25^\circ\text{C}^{(4)}$            | -1                  | -   | 1                  |               |
| $t_{\text{SU(HSI)}}$  | HSI oscillator startup time      | -   | 1 <sup>(2)</sup>    | -   | 2 <sup>(2)</sup>   | $\mu\text{s}$ |
| $I_{\text{DDA(HSI)}}$ | HSI oscillator power consumption | -   | -                   | 80  | 100 <sup>(2)</sup> | $\mu\text{A}$ |

- $V_{\text{DDA}} = 3.3 \text{ V}$ ,  $T_A = -40 \text{ to } 105^\circ\text{C}$  unless otherwise specified.
- Guaranteed by design, not tested in production.
- Data based on characterization results, not tested in production.
- Factory calibrated, parts not soldered.

Figure 19. HSI oscillator accuracy characterization results for soldered parts



Low-speed internal (LSI) RC oscillator

Table 41. LSI oscillator characteristics<sup>(1)</sup>

| Symbol                              | Parameter                        | Min | Typ  | Max | Unit |
|-------------------------------------|----------------------------------|-----|------|-----|------|
| f <sub>LSI</sub>                    | Frequency                        | 30  | 40   | 50  | kHz  |
| t <sub>su(LSI)</sub> <sup>(2)</sup> | LSI oscillator startup time      | -   | -    | 85  | µs   |
| I <sub>DD(LSI)</sub> <sup>(2)</sup> | LSI oscillator power consumption | -   | 0.75 | 1.2 | µA   |

1. V<sub>DDA</sub> = 3.3 V, T<sub>A</sub> = -40 to 105 °C unless otherwise specified.
2. Guaranteed by design, not tested in production.

6.3.9 PLL characteristics

The parameters given in [Table 42](#) are derived from tests performed under ambient temperature and supply voltage conditions summarized in [Table 19](#).

Table 42. PLL characteristics

| Symbol               | Parameter                      | Value             |     |                    | Unit |
|----------------------|--------------------------------|-------------------|-----|--------------------|------|
|                      |                                | Min               | Typ | Max                |      |
| f <sub>PLL_IN</sub>  | PLL input clock <sup>(1)</sup> | 1 <sup>(2)</sup>  | -   | 24 <sup>(2)</sup>  | MHz  |
|                      | PLL input clock duty cycle     | 40 <sup>(2)</sup> | -   | 60 <sup>(2)</sup>  | %    |
| f <sub>PLL_OUT</sub> | PLL multiplier output clock    | 16 <sup>(2)</sup> | -   | 72                 | MHz  |
| t <sub>LOCK</sub>    | PLL lock time                  | -                 | -   | 200 <sup>(2)</sup> | µs   |
| Jitter               | Cycle-to-cycle jitter          | -                 | -   | 300 <sup>(2)</sup> | ps   |

1. Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by f<sub>PLL\_OUT</sub>.
2. Guaranteed by design, not tested in production.



### 6.3.10 Memory characteristics

#### Flash memory

The characteristics are given at  $T_A = -40$  to  $105$  °C unless otherwise specified.

**Table 43. Flash memory characteristics**

| Symbol             | Parameter               | Conditions               | Min | Typ  | Max <sup>(1)</sup> | Unit |
|--------------------|-------------------------|--------------------------|-----|------|--------------------|------|
| $t_{\text{prog}}$  | 16-bit programming time | $T_A = -40$ to $+105$ °C | 40  | 53.5 | 60                 | µs   |
| $t_{\text{ERASE}}$ | Page (2 KB) erase time  | $T_A = -40$ to $+105$ °C | 20  | -    | 40                 | ms   |
| $t_{\text{ME}}$    | Mass erase time         | $T_A = -40$ to $+105$ °C | 20  | -    | 40                 | ms   |
| $I_{\text{DD}}$    | Supply current          | Write mode               | -   | -    | 10                 | mA   |
|                    |                         | Erase mode               | -   | -    | 12                 | mA   |

1. Guaranteed by design, not tested in production.

**Table 44. Flash memory endurance and data retention**

| Symbol           | Parameter      | Conditions  | Value              | Unit    |
|------------------|----------------|---|--------------------|---------|
|                  |                |   | Min <sup>(1)</sup> |         |
| $N_{\text{END}}$ | Endurance      | $T_A = -40$ to $+85$ °C (6 suffix versions)<br>$T_A = -40$ to $+105$ °C (7 suffix versions) | 10                 | kcycles |
| $t_{\text{RET}}$ | Data retention | 1 kcycle <sup>(2)</sup> at $T_A = 85$ °C  | 30                 | Years   |
|                  |                | 1 kcycle <sup>(2)</sup> at $T_A = 105$ °C   | 10                 |         |
|                  |                | 10 kcycle <sup>(2)</sup> at $T_A = 55$ °C   | 20                 |         |

1. Data based on characterization results, not tested in production.

2. Cycling performed over the whole temperature range.

### 6.3.11 FSMC characteristics

Unless otherwise specified, the parameters given in [Table 45](#) to [Table 60](#) for the FSMC interface are derived from tests performed under the ambient temperature,  $f_{\text{HCLK}}$  frequency and  $V_{\text{DD}}$  supply voltage conditions summarized in [Table 19](#) with the following configuration:

- Output speed is set to  $\text{OSPEEDRy}[1:0] = 11$
- Capacitive load  $C = 30$  pF
- Measurement points are done at CMOS levels:  $0.5V_{\text{DD}}$

Refer to [Section 6.3.15: I/O port characteristics](#): for more details on the input/output characteristics.

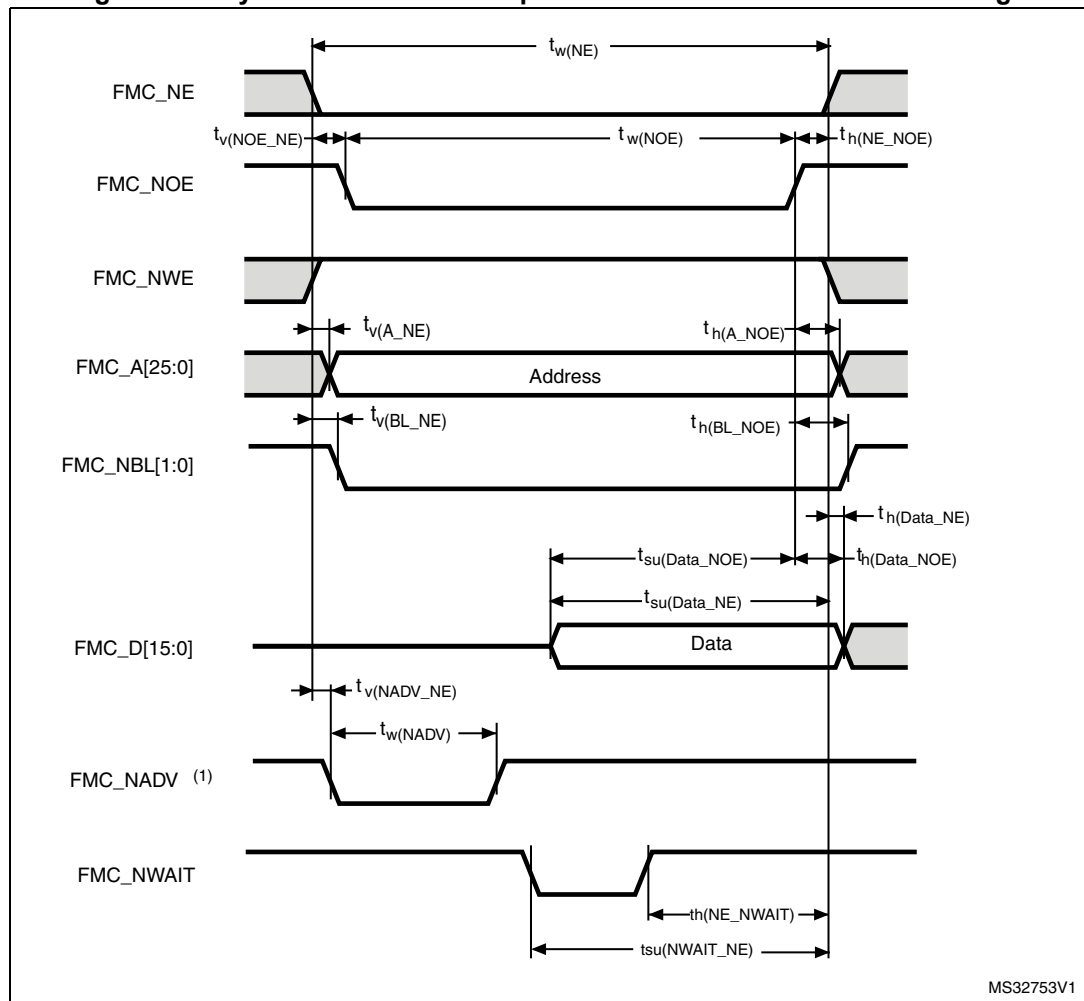
**Asynchronous waveforms and timings**

Figure 20 to Figure 23 represent asynchronous waveforms and Table 45 to Table 52 provide the corresponding timings. The results shown in these tables are obtained with the following FSMC configuration:

- AddressSetupTime = 0x1
- AddressHoldTime = 0x1
- DataSetupTime = 0x1 (except for asynchronous NWAIT mode, DataSetupTime = 0x5)
- BusTurnAroundDuration = 0x0
- NOR NWAIT pulse width= 1THCLK

In all the timing tables, the  $T_{HCLK}$  is the HCLK clock period.

**Figure 20. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings**



**Table 45. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings<sup>(1)</sup>**

| Symbol              | Parameter                             | Min       | Max         | Unit |
|---------------------|---------------------------------------|-----------|-------------|------|
| $t_{w(NE)}$         | FMC_NE low time                       | 2THCLK- 1 | 2THCLK+1    | ns   |
| $t_{v(NOE\_NE)}$    | FMC_NEx low to FMC_NOE low            | 0         | 1           |      |
| $t_{w(NOE)}$        | FMC_NOE low time                      | 2THCLK    | 2THCLK+ 1.5 |      |
| $t_{h(NE\_NOE)}$    | FMC_NOE high to FMC_NE high hold time | 0.5       | -           |      |
| $t_{v(A\_NE)}$      | FMC_NEx low to FMC_A valid            | -         | 3           |      |
| $t_{h(A\_NOE)}$     | Address hold time after FMC_NOE high  | 0         | -           |      |
| $t_{v(BL\_NE)}$     | FMC_NEx low to FMC_BL valid           | -         | 2 (NA)      |      |
| $t_{h(BL\_NOE)}$    | FMC_BL hold time after FMC_NOE high   | 0         | -           |      |
| $t_{su(Data\_NE)}$  | Data to FMC_NEx high setup time       | THCLK + 6 | -           |      |
| $t_{su(Data\_NOE)}$ | Data to FMC_NOEx high setup time      | THCLK + 7 | -           |      |
| $t_{h(Data\_NOE)}$  | Data hold time after FMC_NOE high     | 0         | -           |      |
| $t_{h(Data\_NE)}$   | Data hold time after FMC_NEx high     | 0         | -           |      |
| $t_{v(NADV\_NE)}$   | FMC_NEx low to FMC_NADV low           | -         | 2           |      |
| $t_{w(NADV)}$       | FMC_NADV low time                     | -         | THCLK +1.5  |      |

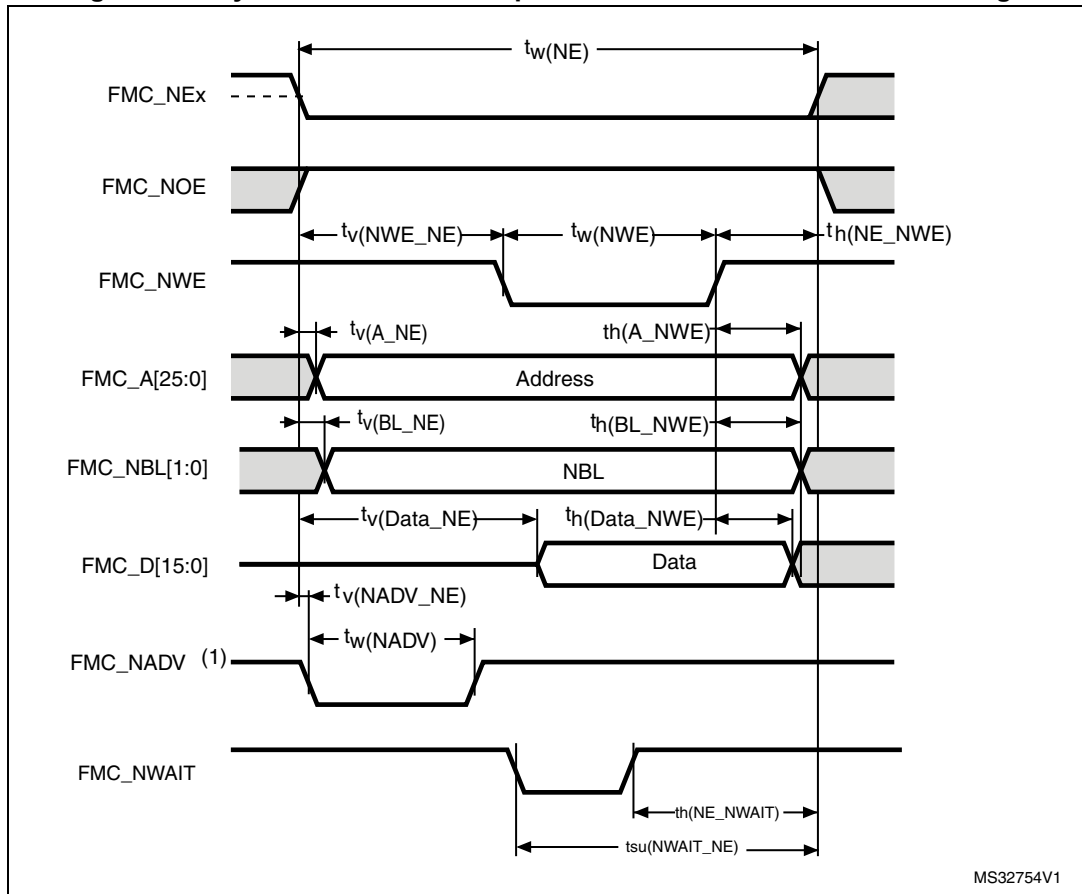
1. Based on characterization, not tested in production

**Table 46. Asynchronous non-multiplexed SRAM/PSRAM/NOR read-NWAIT timings<sup>(1)</sup>**

| Symbol              | Parameter                                 | Min         | Max       | Unit |
|---------------------|---|-------------|-----------|------|
| $t_{w(NE)}$         | FMC_NE low time                           | 7THCLK +0.5 | 7THCLK+ 1 | ns   |
| $t_{w(NOE)}$        | FMC_NWE low time                          | 6THCLK -1.5 | 6THCLK +2 |      |
| $t_{su(NWAIT\_NE)}$ | FMC_NWAIT valid before FMC_NEx high       | 4THCLK +5   | -         |      |
| $t_{h(NE\_NWAIT)}$  | FMC_NEx hold time after FMC_NWAIT invalid | 4THCLK-3    | -         |      |

1. Based on characterization, not tested in production.

Figure 21. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings



1. Mode 2/B, C and D only. In Mode 1, FMC\_NADV is not used.

Table 47. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings<sup>(1)</sup>

| Symbol             | Parameter                             | Min       | Max      | Unit |
|--------------------|---------------------------------------|-----------|----------|------|
| $t_{w(NE)}$        | FMC_NE low time                       | 3THCLK-1  | 3THCLK+2 | ns   |
| $t_{v(NWE\_NE)}$   | FMC_NEx low to FMC_NWE low            | THCLK+0.5 | THCLK+1  |      |
| $t_{w(NWE)}$       | FMC_NWE low time                      | THCLK-2   | THCLK+1  |      |
| $t_{h(NE\_NWE)}$   | FMC_NWE high to FMC_NE high hold time | THCLK-0.5 | -        |      |
| $t_{v(A\_NE)}$     | FMC_NEx low to FMC_A valid            | -         | 0        |      |
| $t_{h(A\_NWE)}$    | Address hold time after FMC_NWE high  | THCLK-1.5 | -        |      |
| $t_{v(BL\_NE)}$    | FMC_NEx low to FMC_BL valid           | -         | 1        |      |
| $t_{h(BL\_NWE)}$   | FMC_BL hold time after FMC_NWE high   | THCLK-0.5 | -        |      |
| $t_{v(Data\_NE)}$  | Data to FMC_NEx low to Data valid     | -         | THCLK+ 3 |      |
| $t_{h(Data\_NWE)}$ | Data hold time after FMC_NWE high     | THCLK+0.5 | -        |      |
| $t_{v(NADV\_NE)}$  | FMC_NEx low to FMC_NADV low           | -         | 2.5      |      |
| $t_{w(NADV)}$      | FMC_NADV low time                     | -         | THCLK+2  |      |

1. Based on characterization, not tested in production.

**Table 48. Asynchronous non-multiplexed SRAM/PSRAM/NOR write-NWAIT timings<sup>(1)</sup>**

| Symbol              | Parameter                                 | Min        | Max      | Unit |
|---------------------|---|------------|----------|------|
| $t_{w(NE)}$         | FMC_NE low time                           | 8THCLK+1   | 8THCLK+2 | ns   |
| $t_{w(NWE)}$        | FMC_NWE low time                          | 6THCLK-1   | 6THCLK+2 |      |
| $t_{su(NWAIT\_NE)}$ | FMC_NWAIT valid before FMC_NEx high       | 5THCLK-0.5 | -        |      |
| $t_h(NE\_NWAIT)$    | FMC_NEx hold time after FMC_NWAIT invalid | 4THCLK+2   | -        |      |

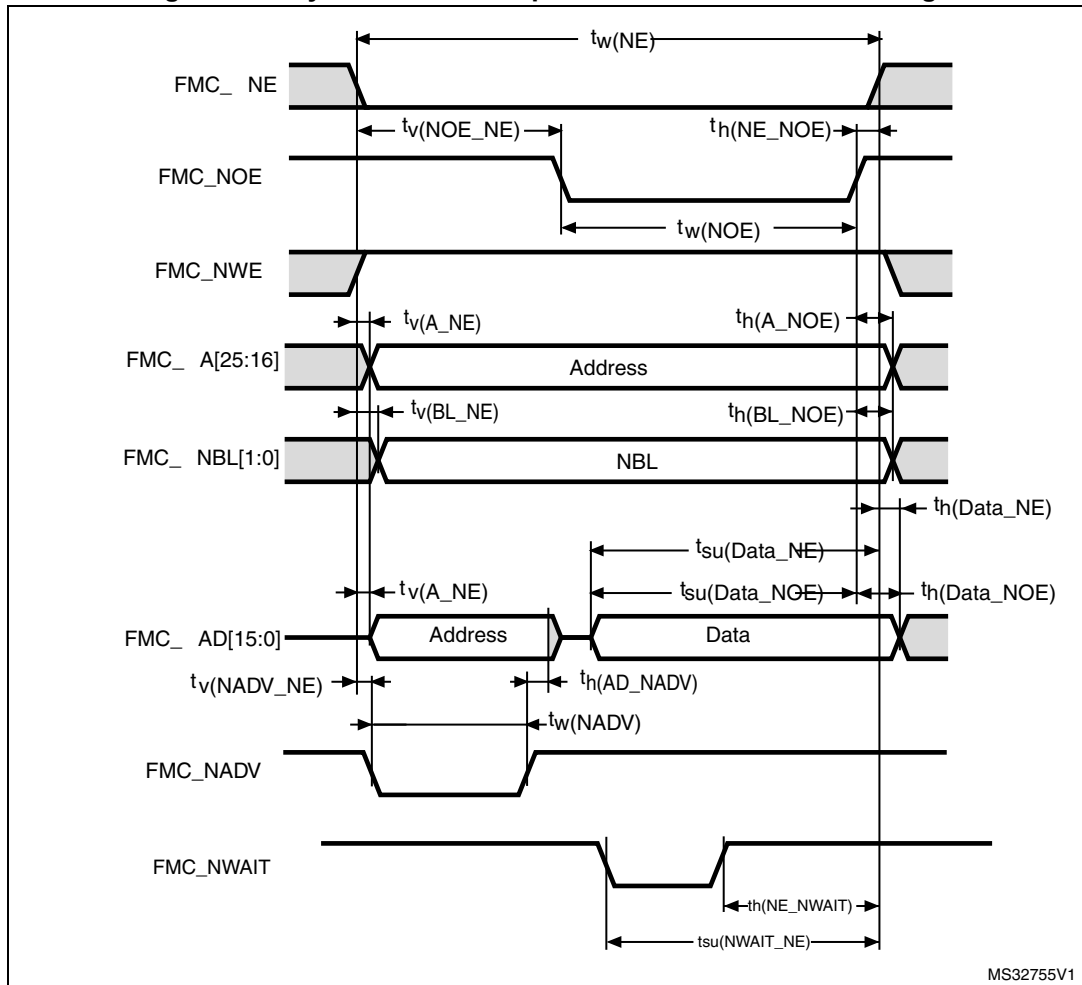
1. Based on characterization, not tested in production.

**Table 49. Asynchronous multiplexed PSRAM/NOR read-NWAIT timings<sup>(1)</sup>**

| Symbol              | Parameter                                 | Min      | Max        | Unit |
|---------------------|---|----------|------------|------|
| $t_{w(NE)}$         | FMC_NE low time                           | 8THCLK+2 | 8THCLK+2   | ns   |
| $t_{w(NOE)}$        | FMC_NWE low time                          | 6THCLK-1 | 6THCLK+1.5 |      |
| $t_{su(NWAIT\_NE)}$ | FMC_NWAIT valid before FMC_NEx high       | 4THCLK+6 | -          |      |
| $t_h(NE\_NWAIT)$    | FMC_NEx hold time after FMC_NWAIT invalid | 4THCLK-4 | -          |      |

1. Based on characterization, not tested in production.

Figure 22. Asynchronous multiplexed PSRAM/NOR read timings



MS32755V1

Table 50. Asynchronous multiplexed PSRAM/NOR read timings<sup>(1)</sup>

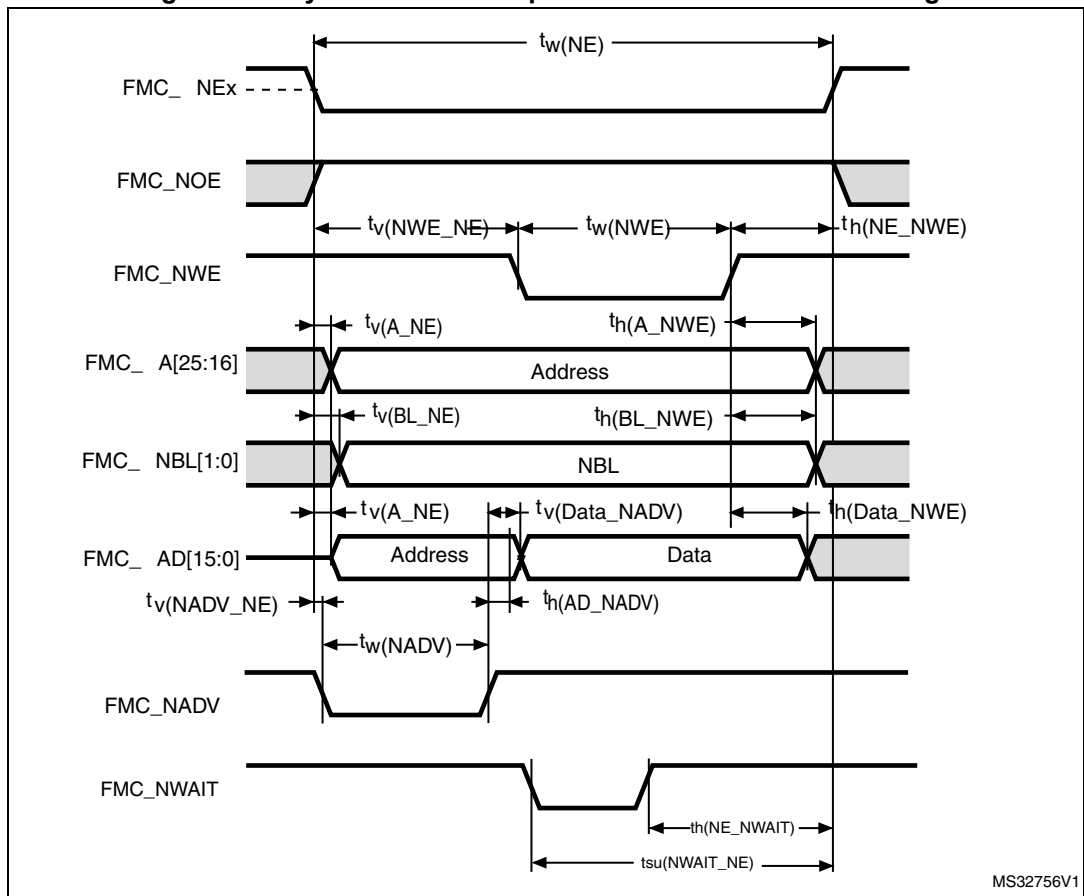
| Symbol            | Parameter   | Min        | Max      | Unit |
|-------------------|---|------------|----------|------|
| $t_{w(NE)}$       | FMC_NE low time                                     | 3THCLK-0.5 | 3THCLK+1 | ns   |
| $t_{v(NOE\_NE)}$  | FMC_NEx low to FMC_NOE low                          | 2THCLK     | 2THCLK+1 |      |
| $t_{w(NOE)}$      | FMC_NOE low time                                    | THCLK-2    | THCLK+2  |      |
| $t_{h(NE\_NOE)}$  | FMC_NOE high to FMC_NE high hold time               | 0          | -        |      |
| $t_{v(A\_NE)}$    | FMC_NEx low to FMC_A valid                          | -          | 1.5      |      |
| $t_{v(NADV\_NE)}$ | FMC_NEx low to FMC_NADV low                         | 0          | 2        |      |
| $t_{w(NADV)}$     | FMC_NADV low time                                   | THCLK-2    | THCLK+2  |      |
| $t_{h(AD\_NADV)}$ | FMC_AD(address) valid hold time after FMC_NADV high | 0          | -        |      |
| $t_{h(A\_NOE)}$   | Address hold time after FMC_NOE high                | THCLK-0.5  | -        |      |
| $t_{h(BL\_NOE)}$  | FMC_BL time after FMC_NOE high                      | 0          | -        |      |

**Table 50. Asynchronous multiplexed PSRAM/NOR read timings<sup>(1)</sup> (continued)**

| Symbol              | Parameter                         | Min     | Max | Unit |
|---------------------|-----------------------------------|---------|-----|------|
| $t_{v(BL\_NE)}$     | FMC_NEx low to FMC_BL valid       | -       | 2   | ns   |
| $t_{su(Data\_NE)}$  | Data to FMC_NEx high setup time   | THCLK   | -   |      |
| $t_{su(Data\_NOE)}$ | Data to FMC_NOE high setup time   | THCLK+1 | -   |      |
| $t_h(Data\_NE)$     | Data hold time after FMC_NEx high | 0       | -   |      |
| $t_h(Data\_NOE)$    | Data hold time after FMC_NOE high | 0       | -   |      |

1. Based on characterization, not tested in production.

**Figure 23. Asynchronous multiplexed PSRAM/NOR write timings**



MS32756V1

**Table 51. Asynchronous multiplexed PSRAM/NOR write timings<sup>(1)</sup>**

| Symbol              | Parameter   | Min        | Max        | Unit |
|---------------------|---|------------|------------|------|
| $t_{w(NE)}$         | FMC_NE low time                                     | 4THCLK-1   | 4THCLK+1   | ns   |
| $t_{v(NWE\_NE)}$    | FMC_NEx low to FMC_NWE low                          | THCLK      | THCLK+0.5  |      |
| $t_{w(NWE)}$        | FMC_NWE low time                                    | 2THCLK-0.5 | 2THCLK+1   |      |
| $t_{h(NE\_NWE)}$    | FMC_NWE high to FMC_NE high hold time               | THCLK-0.5  | -          |      |
| $t_{v(A\_NE)}$      | FMC_NEx low to FMC_A valid                          | -          | 5          |      |
| $t_{v(NADV\_NE)}$   | FMC_NEx low to FMC_NADV low                         | 1          | 2.5        |      |
| $t_{w(NADV)}$       | FMC_NADV low time                                   | THCLK-2    | THCLK+2    |      |
| $t_{h(AD\_NADV)}$   | FMC_AD(adress) valid hold time after FMC_NADV high) | THCLK-2    | -          |      |
| $t_{h(A\_NWE)}$     | Address hold time after FMC_NWE high                | THCLK-1    | -          |      |
| $t_{h(BL\_NWE)}$    | FMC_BL hold time after FMC_NWE high                 | THCLK-0.5  | -          |      |
| $t_{v(BL\_NE)}$     | FMC_NEx low to FMC_BL valid                         | -          | 1          |      |
| $t_{v(Data\_NADV)}$ | FMC_NADV high to Data valid                         | -          | THCLK +3.5 |      |
| $t_{h(Data\_NWE)}$  | Data hold time after FMC_NWE high                   | THCLK +0.5 | -          |      |

1. Based on characterization, not tested in production.

**Table 52. Asynchronous multiplexed PSRAM/NOR write-NWAIT timings<sup>(1)</sup>**

| Symbol              | Parameter                                 | Min      | Max        | Unit |
|---------------------|---|----------|------------|------|
| $t_{w(NE)}$         | FMC_NE low time                           | 9THCLK   | 9THCLK+0.5 | ns   |
| $t_{w(NWE)}$        | FMC_NWE low time                          | 6THCLK   | 6THCLK+2   |      |
| $t_{su(NWAIT\_NE)}$ | FMC_NWAIT valid before FMC_NEx high       | 5THCLK+6 | -          |      |
| $t_{h(NE\_NWAIT)}$  | FMC_NEx hold time after FMC_NWAIT invalid | 5THCLK-5 | -          |      |

1. Based on characterization, not tested in production.

**Synchronous waveforms and timings**

Figure 24 and Figure 27 present the synchronous waveforms and Table 53 to Table 56 provide the corresponding timings. The results shown in these tables are obtained with the following FSMC configuration:

- BurstAccessMode = FMC\_BurstAccessMode\_Enable;
- MemoryType = FMC\_MemoryType\_CRAM;
- WriteBurst = FMC\_WriteBurst\_Enable;
- CLKDivision = 1;
- DataLatency = 2 for NOR Flash; DataLatency = 0 for PSRAM

In all timing tables, the THCLK is the HCLK clock period (with maximum FMC\_CLK = 36 MHz).





Figure 24. Synchronous multiplexed NOR/PSRAM read timings

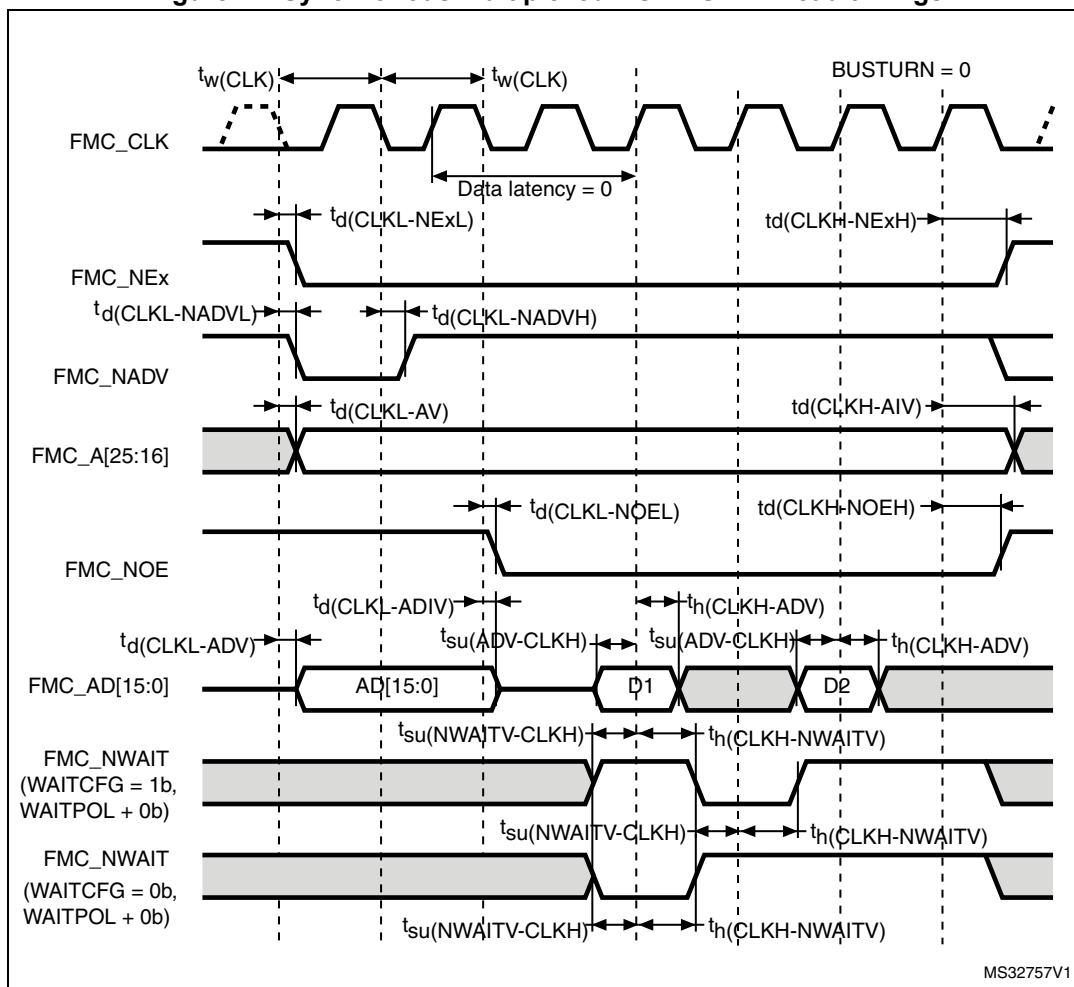


Table 53. Synchronous multiplexed NOR/PSRAM read timings<sup>(1)</sup>

| Symbol                   | Parameter                                  | Min     | Max | Unit |
|--------------------------|--|---------|-----|------|
| $t_w(\text{CLK})$        | FMC_CLK period                             | 2THCLK  | -   | ns   |
| $t_d(\text{CLKL-NExL})$  | FMC_CLK low to FMC_NEx low (x=0..2)        | -       | 5   |      |
| $t_d(\text{CLKH-NExH})$  | FMC_CLK high to FMC_NEx high (x=0..2)      | THCLK+1 | -   |      |
| $t_d(\text{CLKL-NADV})$  | FMC_CLK low to FMC_NADV low                | -       | 7   |      |
| $t_d(\text{CLKL-NADVH})$ | FMC_CLK low to FMC_NADV high               | 2.5     | -   |      |
| $t_d(\text{CLKL-AV})$    | FMC_CLK low to FMC_Ax valid (x=16...25)    | -       | 3   |      |
| $t_d(\text{CLKH-AIV})$   | FMC_CLK high to FMC_Ax invalid (x=16...25) | 0       | -   |      |
| $t_d(\text{CLKL-NOEL})$  | FMC_CLK low to FMC_NOE low                 | -       | 6   |      |
| $t_d(\text{CLKH-NOEH})$  | FMC_CLK high to FMC_NOE high               | THCLK+1 | -   |      |
| $t_d(\text{CLKL-ADV})$   | FMC_CLK low to FMC_AD[15:0] valid          | -       | 2   |      |

**Table 53. Synchronous multiplexed NOR/PSRAM read timings<sup>(1)</sup> (continued)**

| Symbol               | Parameter                                    | Min | Max | Unit |
|----------------------|--|-----|-----|------|
| $t_{d(CLKL-ADIV)}$   | FMC_CLK low to FMC_AD[15:0] invalid          | 0   | -   | ns   |
| $t_{su(ADV-CLKH)}$   | FMC_A/D[15:0] valid data before FMC_CLK high | 4   | -   |      |
| $t_{h(CLKH-ADV)}$    | FMC_A/D[15:0] valid data after FMC_CLK high  | 6   | -   |      |
| $t_{su(NWAIT-CLKH)}$ | FMC_NWAIT valid before FMC_CLK high          | 3   | -   |      |
| $t_{h(CLKH-NWAIT)}$  | FMC_NWAIT valid after FMC_CLK high           | 4   | -   |      |

1. Based on characterization, not tested in production.

**Figure 25. Synchronous multiplexed PSRAM write timings**

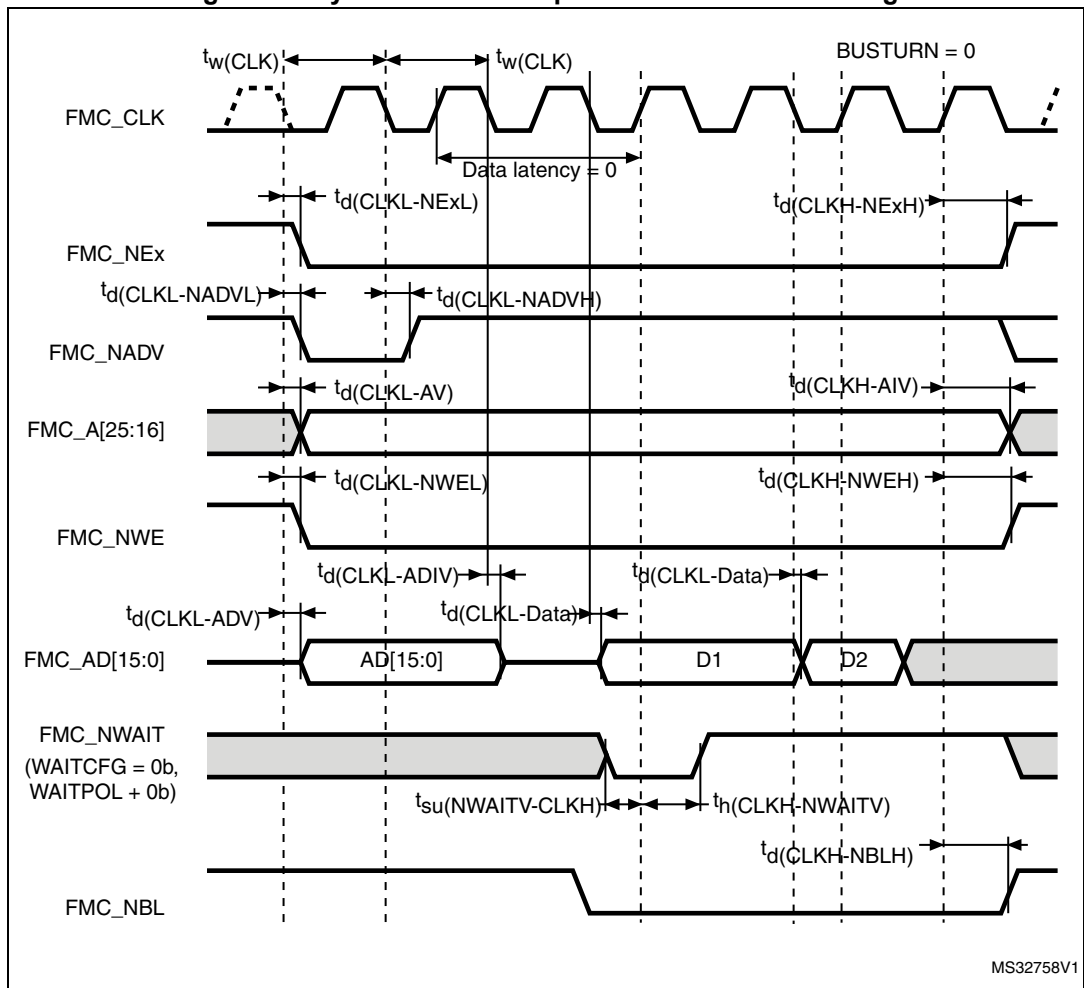
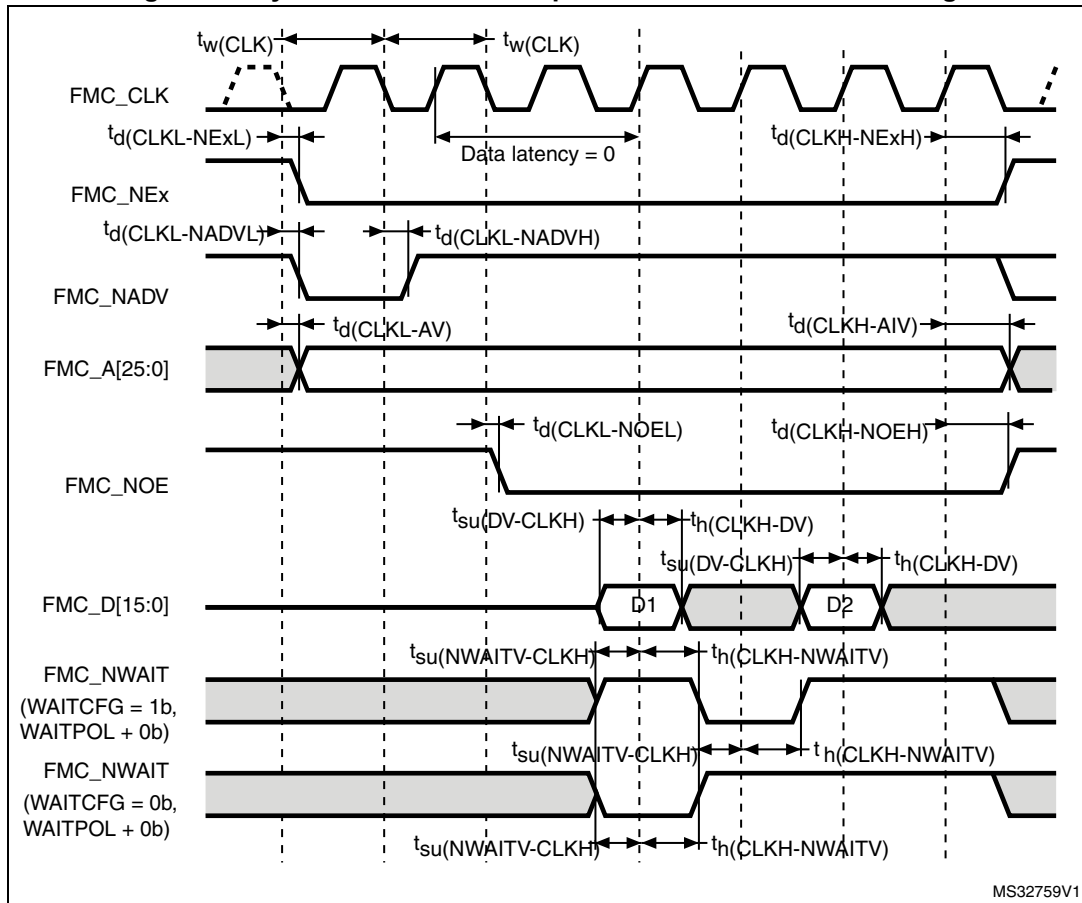


Table 54. Synchronous multiplexed PSRAM write timings<sup>(1) (2)</sup>

| Symbol                      | Parameter                                  | Min      | Max | Unit |
|-----------------------------|--|----------|-----|------|
| $t_{w(\text{CLK})}$         | FMC_CLK period, VDD range= 2.7 to 3.6 V    | 2THCLK-1 | -   | ns   |
| $t_{d(\text{CLKL-NExL})}$   | FMC_CLK low to FMC_NEx low (x=0..2)        | -        | 5.5 |      |
| $t_{d(\text{CLKH-NExH})}$   | FMC_CLK high to FMC_NEx high (x=0..2)      | THCLK+1  | -   |      |
| $t_{d(\text{CLKL-NADV})}$   | FMC_CLK low to FMC_NADV low                | -        | 7   |      |
| $t_{d(\text{CLKL-NADVH})}$  | FMC_CLK low to FMC_NADV high               | 2        | -   |      |
| $t_{d(\text{CLKL-AV})}$     | FMC_CLK low to FMC_Ax valid (x=16...25)    | -        | 0   |      |
| $t_{d(\text{CLKH-AIV})}$    | FMC_CLK high to FMC_Ax invalid (x=16...25) | 0        | -   |      |
| $t_{d(\text{CLKL-NWEL})}$   | FMC_CLK low to FMC_NWE low                 | -        | 5.5 |      |
| $t_{d(\text{CLKH-NWEH})}$   | FMC_CLK high to FMC_NWE high               | THCLK+1  | -   |      |
| $t_{d(\text{CLKL-ADV})}$    | FMC_CLK low to FMC_AD[15:0] valid          | -        | 7.5 |      |
| $t_{d(\text{CLKL-ADIV})}$   | FMC_CLK low to FMC_AD[15:0] invalid        | 0        | -   |      |
| $t_{d(\text{CLKL-DATA})}$   | FMC_A/D[15:0] valid data after FMC_CLK low | -        | 8   |      |
| $t_{d(\text{CLKL-NBLL})}$   | FMC_CLK low to FMC_NBL low                 | -        | 6   |      |
| $t_{d(\text{CLKH-NBLH})}$   | FMC_CLK high to FMC_NBL high               | THCLK+1  | -   |      |
| $t_{su(\text{NWAIT-CLKH})}$ | FMC_NWAIT valid before FMC_CLK high        | 3        | -   |      |
| $t_h(\text{CLKH-NWAIT})$    | FMC_NWAIT valid after FMC_CLK high         | 5        | -   |      |

1. Based on characterization, not tested in production.
2.  $C_L = 30$  pF.

Figure 26. Synchronous non-multiplexed NOR/PSRAM read timings



MS32759V1

Table 55. Synchronous non-multiplexed NOR/PSRAM read timings<sup>(1)</sup>

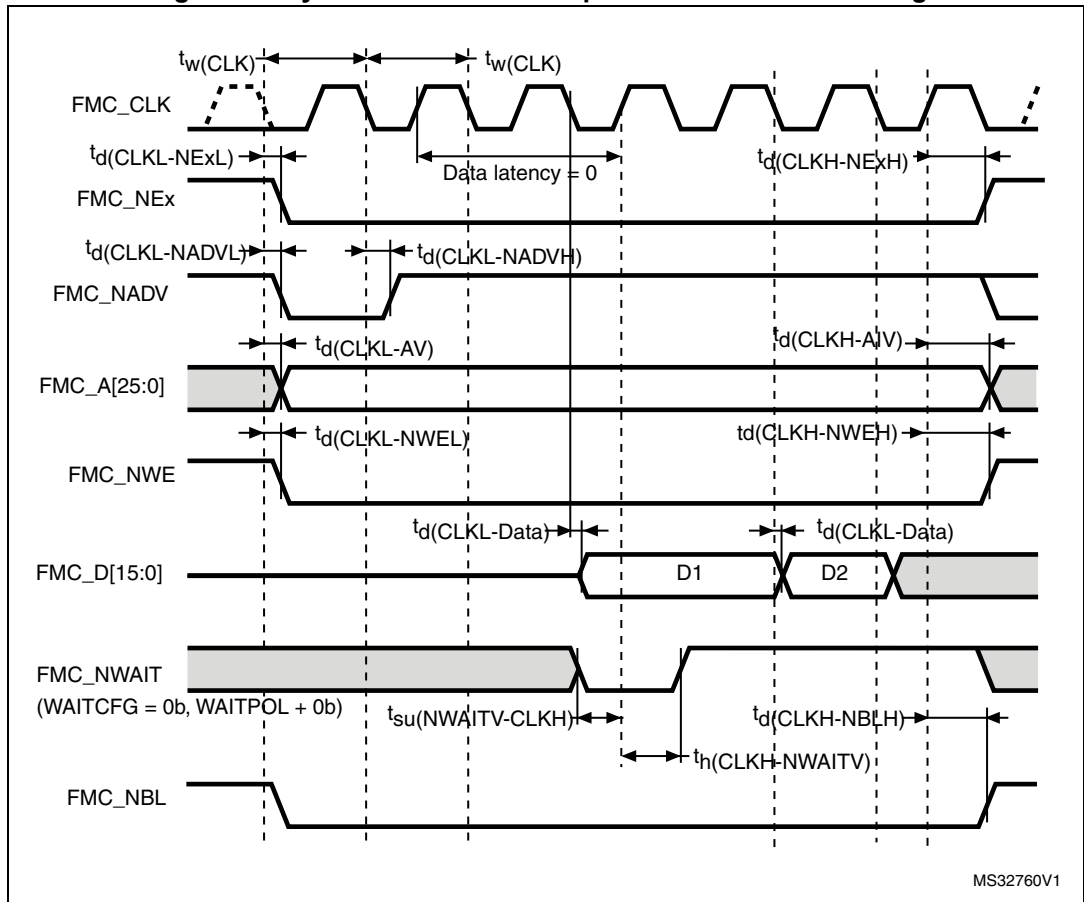
| Symbol              | Parameter                                  | Min      | Max | Unit |
|---------------------|--|----------|-----|------|
| $t_{w(CLK)}$        | FMC_CLK period                             | 2THCLK-1 | -   | ns   |
| $t_{d(CLKL-NExL)}$  | FMC_CLK low to FMC_NEx low (x=0..2)        | -        | 5   |      |
| $t_{d(CLKH-NExH)}$  | FMC_CLK high to FMC_NEx high (x= 0..2)     | THCLK+1  | -   |      |
| $t_{d(CLKL-NADV)}$  | FMC_CLK low to FMC_NADV low                | -        | 7   |      |
| $t_{d(CLKL-NADVH)}$ | FMC_CLK low to FMC_NADV high               | 2.5      | -   |      |
| $t_{d(CLKL-AV)}$    | FMC_CLK low to FMC_Ax valid (x=16...25)    | -        | 7   |      |
| $t_{d(CLKH-AIV)}$   | FMC_CLK high to FMC_Ax invalid (x=16...25) | THCLK    | -   |      |
| $t_{d(CLKL-NOEL)}$  | FMC_CLK low to FMC_NOE low                 | -        | 6   |      |
| $t_{d(CLKH-NOEH)}$  | FMC_CLK high to FMC_NOE high               | THCLK+1  | -   |      |
| $t_{su(DV-CLKH)}$   | FMC_D[15:0] valid data before FMC_CLK high | 3.5      | -   |      |

**Table 55. Synchronous non-multiplexed NOR/PSRAM read timings<sup>(1)</sup> (continued)**

| Symbol               | Parameter                                 | Min | Max | Unit |
|----------------------|---|-----|-----|------|
| $t_{h(CLKH-DV)}$     | FMC_D[15:0] valid data after FMC_CLK high | 5   | -   | ns   |
| $t_{su(NWAIT-CLKH)}$ | FMC_NWAIT valid before FMC_CLK high       | 2   | -   |      |
| $t_{h(CLKH-NWAIT)}$  | FMC_NWAIT valid after FMC_CLK high        | 4   | -   |      |

1. Based on characterization, not tested in production.

**Figure 27. Synchronous non-multiplexed PSRAM write timings**



**Table 56. Synchronous non-multiplexed PSRAM write timings<sup>(1)</sup>**

| Symbol                      | Parameter                                  | Min       | Max | Unit |
|-----------------------------|--|-----------|-----|------|
| $t_{w(\text{CLK})}$         | FMC_CLK period                             | 2THCLK-1  | -   | ns   |
| $t_{d(\text{CLKL-NExL})}$   | FMC_CLK low to FMC_NEx low (x=0..2)        | -         | 6   |      |
| $t_{d(\text{CLKH-NExH})}$   | FMC_CLK high to FMC_NEx high (x= 0..2)     | THCLK+1.5 | -   |      |
| $t_{d(\text{CLKL-NADV})}$   | FMC_CLK low to FMC_NADV low                | -         | 7.5 |      |
| $t_{d(\text{CLKL-NADVH})}$  | FMC_CLK low to FMC_NADV high               | 0         | -   |      |
| $t_{d(\text{CLKL-AV})}$     | FMC_CLK low to FMC_Ax valid (x=16...25)    | -         | 6.5 |      |
| $t_{d(\text{CLKH-AIV})}$    | FMC_CLK high to FMC_Ax invalid (x=16...25) | 0         | -   |      |
| $t_{d(\text{CLKL-NWEL})}$   | FMC_CLK low to FMC_NWE low                 | -         | 0   |      |
| $t_{d(\text{CLKH-NWEH})}$   | FMC_CLK high to FMC_NWE high               | THCLK+2   | -   |      |
| $t_{d(\text{CLKL-Data})}$   | FMC_D[15:0] valid data after FMC_CLK low   | -         | 7.5 |      |
| $t_{d(\text{CLKL-NBLL})}$   | FMC_CLK low to FMC_NBL low                 | -         | 7   |      |
| $t_{d(\text{CLKH-NBLH})}$   | FMC_CLK high to FMC_NBL high               | THCLK+0.5 | -   |      |
| $t_{su(\text{NWAIT-CLKH})}$ | FMC_NWAIT valid before FMC_CLK high        | 2         | -   |      |
| $t_h(\text{CLKH-NWAIT})$    | FMC_NWAIT valid after FMC_CLK high         | 4         | -   |      |

1. Based on characterization, not tested in production.

### PC Card/CompactFlash controller waveforms and timings

[Figure 28](#) to [Figure 33](#) present the PC Card/Compact Flash controller waveforms, and [Table 57](#) to [Table 58](#) provide the corresponding timings. The results shown in this table are obtained with the following FSMC configuration:

- COM.FMC\_SetupTime = 0x04;
- COM.FMC\_WaitSetupTime = 0x07;
- COM.FMC\_HoldSetupTime = 0x04;
- COM.FMC\_HiZSetupTime = 0x05;
- ATT.FMC\_SetupTime = 0x04;
- ATT.FMC\_WaitSetupTime = 0x07;
- ATT.FMC\_HoldSetupTime = 0x04;
- ATT.FMC\_HiZSetupTime = 0x05;
- IO.FMC\_SetupTime = 0x04;
- IO.FMC\_WaitSetupTime = 0x07;
- IO.FMC\_HoldSetupTime = 0x04;
- IO.FMC\_HiZSetupTime = 0x05;
- TCLRSetupTime = 0;
- TARSetupTime = 0.

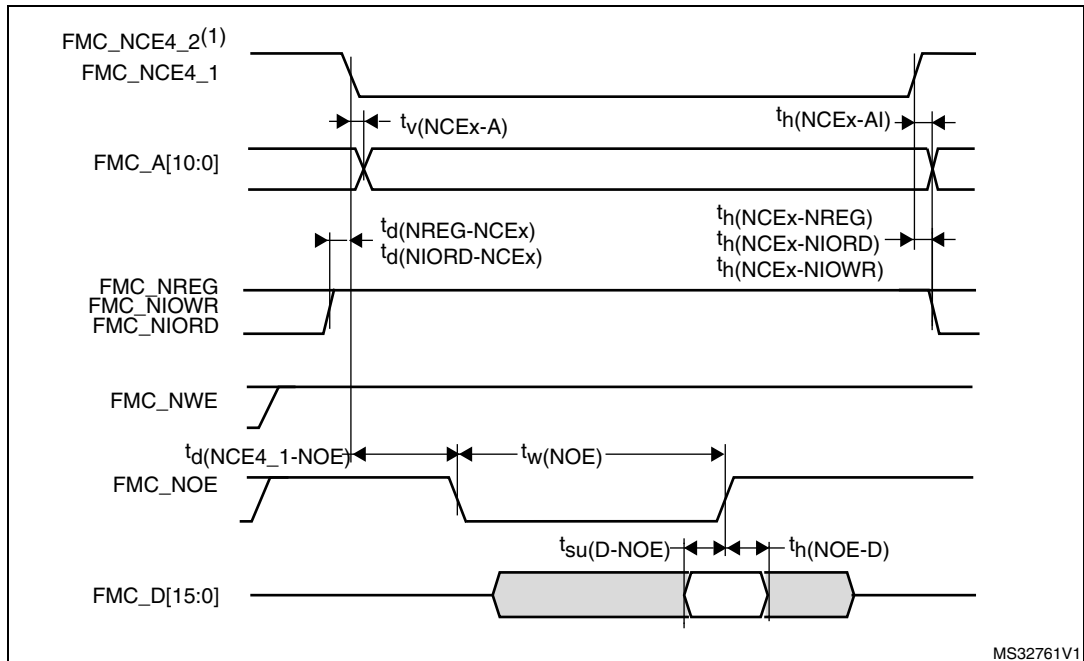
In all timing tables, the THCLK is the HCLK clock period.

**Table 57. Switching characteristics for PC Card/CF read and write cycles in attribute/common space<sup>(1)</sup>**

| Symbol             | Parameter                                  | Min       | Max        | Unit |
|--------------------|--|-----------|------------|------|
| $t_{v(NCEx-A)}$    | FMC_Ncex low to FMC_Ay valid               | -         | 0          | ns   |
| $t_{h(NCEx\_AI)}$  | FMC_NCEX high to FMC_Ax invalid            | 2.5       | -          |      |
| $t_{d(NREG-NCEX)}$ | FMC_NCEX low to FMC_NREG valid             | -         | 2          |      |
| $t_{h(NCEX-NREG)}$ | FMC_NCEX high to FMC_NREG invalid          | 0         | -          |      |
| $t_{d(NCEX-NWE)}$  | FMC_NCEX low to FMC_NWE low                | -         | 5THCLK+2   |      |
| $t_{w(NWE)}$       | FMC_NWE low width                          | 8THCLK    | 8THCLK+0.5 |      |
| $t_{d(NWE\_NCEX)}$ | FMC_NWE high to FMC_NCEX high              | 5THCLK-1  | -          |      |
| $t_{v(NWE-D)}$     | FMC_NWE low to FMC_D[15:0] valid           | -         | 5          |      |
| $t_{h(NWE-D)}$     | FMC_NWE high to FMC_D[15:0] invalid        | 4THCLK-1  | -          |      |
| $t_{d(D-NWE)}$     | FMC_D[15:0] valid before FMC_NWE high      | 13THCLK-3 | -          |      |
| $t_{d(NCEX-NOE)}$  | FMC_NCEX low to FMC_NOE low                | -         | 5THCLK+2   |      |
| $t_{w(NOE)}$       | FMC_NOE low width                          | 8THCLK-1  | 8THCLK+2   |      |
| $t_{d(NOE\_NCEX)}$ | FMC_NOE high to FMC_NCEX high              | 5THCLK-1  | -          |      |
| $t_{su(D-NOE)}$    | FMC_D[15:0] valid data before FMC_NOE high | THCLK+2   | -          |      |
| $t_{h(NOE-D)}$     | FMC_NOE high to FMC_D[15:0] invalid        | 0         | -          |      |

1. Based on characterization, not tested in production.

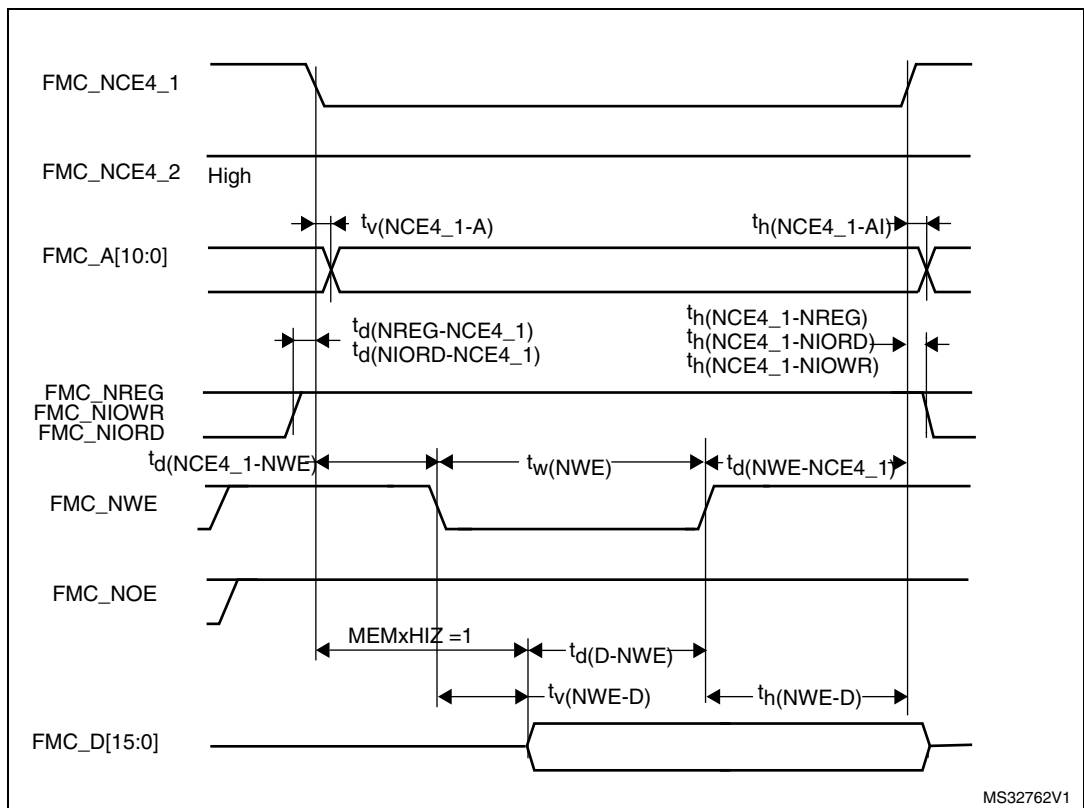
Figure 28. PC Card/CompactFlash controller waveforms for common memory read access



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1. FMC\_NCE4\_2 remains high (inactive during 8-bit access).

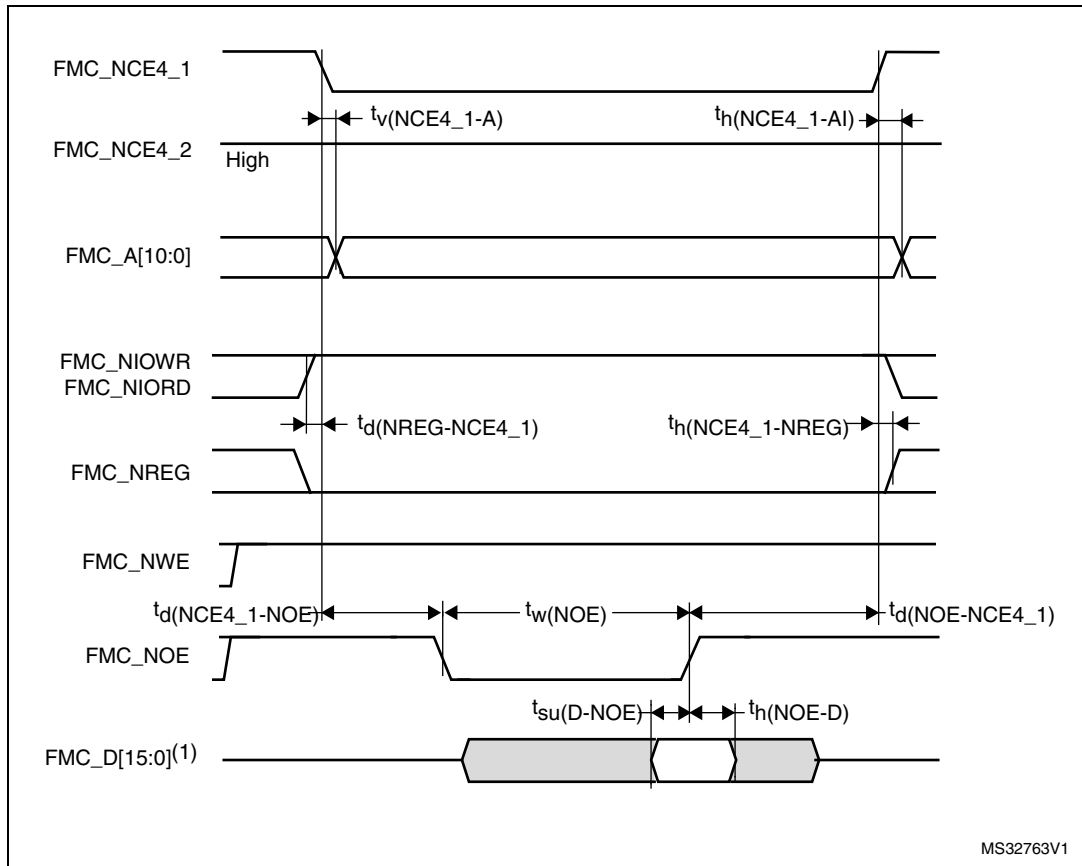
Figure 29. PC Card/CompactFlash controller waveforms for common memory write access



MS32762V1

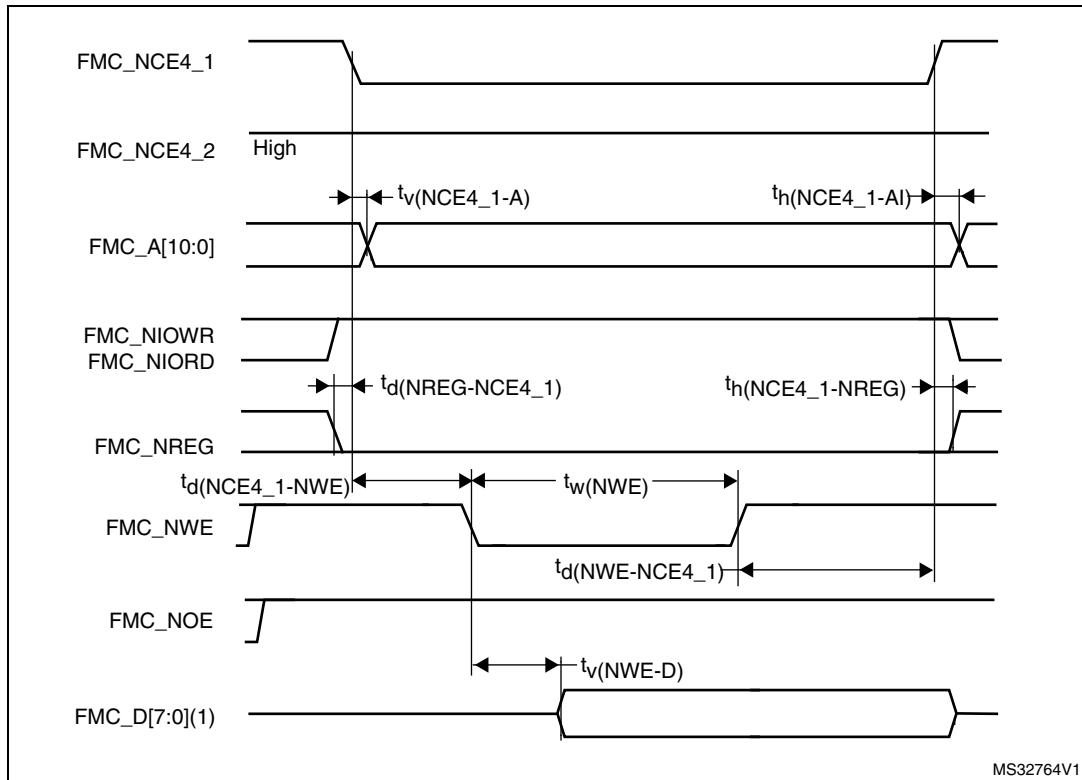


Figure 30. PC Card/CompactFlash controller waveforms for attribute memory read access



1. Only data bits 0...7 are read (bits 8...15 are disregarded).

**Figure 31. PC Card/CompactFlash controller waveforms for attribute memory write access**



1. Only data bits 0...7 are driven (bits 8...15 remains Hi-Z).

**Table 58. Switching characteristics for PC Card/CF read and write cycles in I/O space<sup>(1)</sup>**

| Symbol              | Parameter                               | Min        | Max      | Unit |
|---------------------|---|------------|----------|------|
| $t_w(NIOWR)$        | FMC_NIOWR low width                     | 8THCLK-0.5 | -        | ns   |
| $t_v(NIOWR-D)$      | FMC_NIOWR low to FMC_D[15:0] valid      | -          | 5.5      |      |
| $t_h(NIOWR-D)$      | FMC_NIOWR high to FMC_D[15:0] invalid   | 4THCLK-0.5 | -        |      |
| $t_d(NCE4_1-NIOWR)$ | FMC_NCE4_1 low to FMC_NIOWR valid       | -          | 5THCLK+1 |      |
| $t_h(NCEx-NIOWR)$   | FMC_NCEx high to FMC_NIOWR invalid      | 4THCLK+0.5 | -        |      |
| $t_d(NIORD-NCEx)$   | FMC_NCEx low to FMC_NIORD valid         | -          | 5THCLK   |      |
| $t_h(NCEx-NIORD)$   | FMC_NCEx high to FMC_NIORD) valid       | 6THCLK+2   | -        |      |
| $t_w(NIORD)$        | FMC_NIORD low width                     | 8THCLK-1   | 8THCLK+1 |      |
| $t_{su}(D-NIORD)$   | FMC_D[15:0] valid before FMC_NIORD high | THCLK+2    | -        |      |
| $t_d(NIORD-D)$      | FMC_D[15:0] valid after FMC_NIORD high  | 0          | -        |      |

1. Based on characterization, not tested in production.

Figure 32. PC Card/CompactFlash controller waveforms for I/O space read access

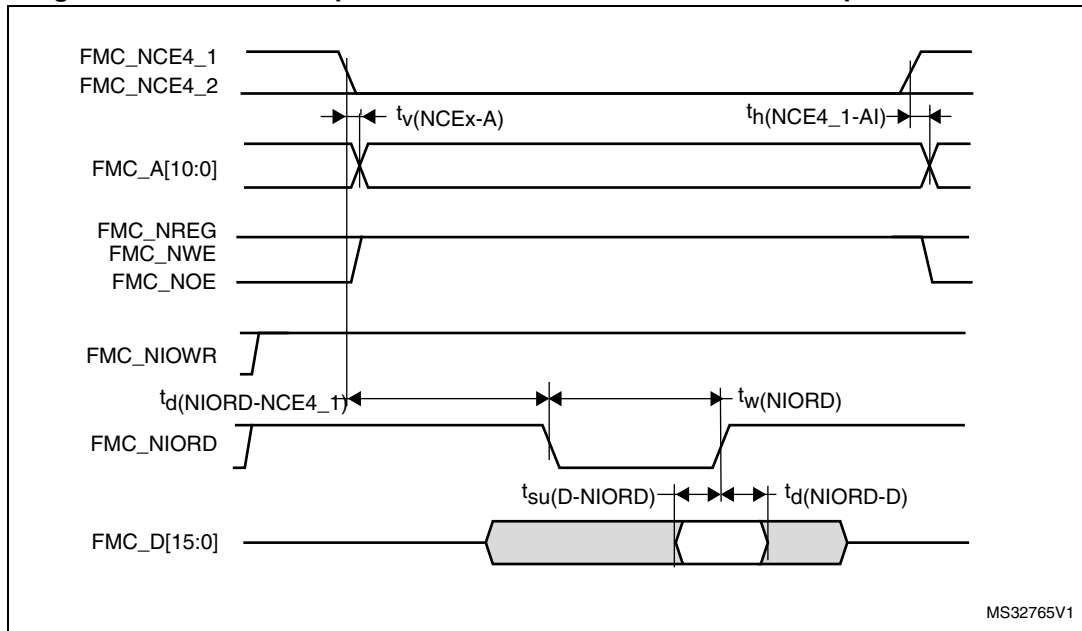
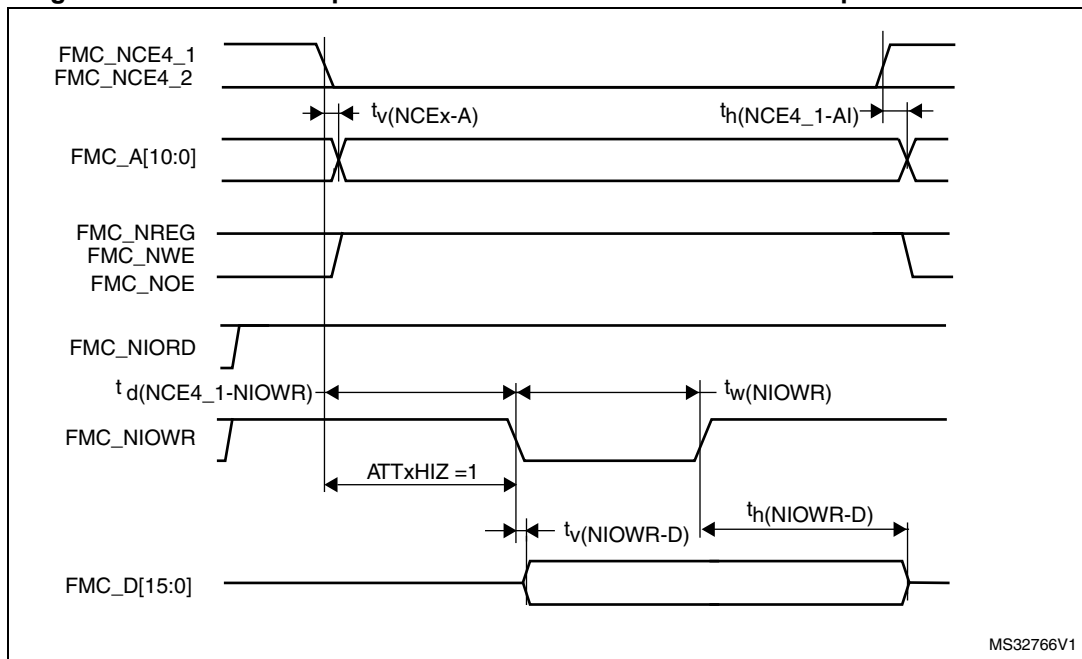


Figure 33. PC Card/CompactFlash controller waveforms for I/O space write access



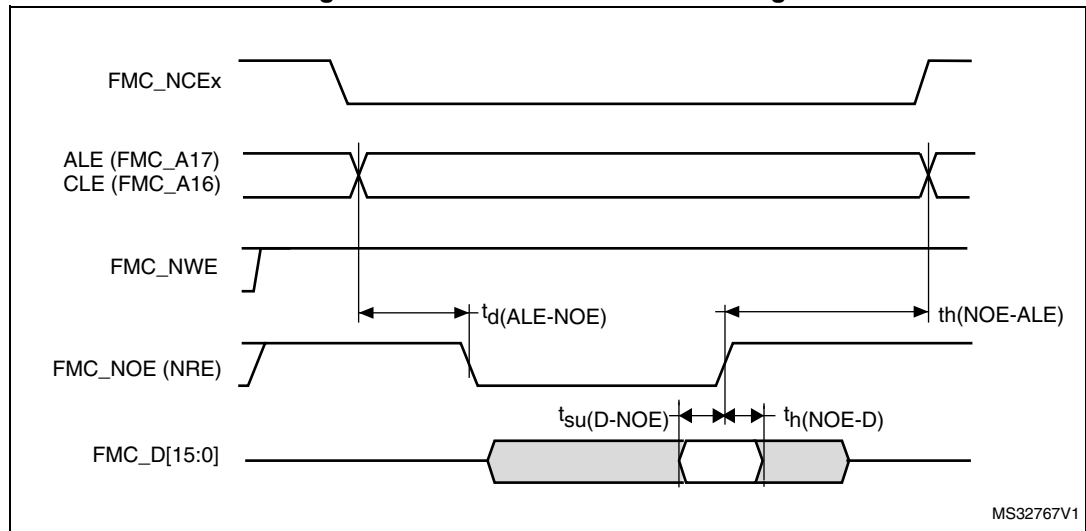
**NAND controller waveforms and timings**

Figure 34 and Figure 35 present the NAND controller synchronous waveforms, and Table 59 and Table 60 provide the corresponding timings. The results shown in this table are obtained with the following FSMC configuration:

- COM.FMC\_SetupTime = 0x01;
- COM.FMC\_WaitSetupTime = 0x03;
- COM.FMC\_HoldSetupTime = 0x02;
- COM.FMC\_HiZSetupTime = 0x03;
- ATT.FMC\_SetupTime = 0x01;
- ATT.FMC\_WaitSetupTime = 0x03;
- ATT.FMC\_HoldSetupTime = 0x02;
- ATT.FMC\_HiZSetupTime = 0x03;
- Bank = FMC\_Bank\_NAND;
- MemoryDataWidth = FMC\_MemoryDataWidth\_16b;
- ECC = FMC\_ECC\_Enable;
- ECCPageSize = FMC\_ECCPageSize\_512Bytes;
- TCLRSetupTime = 0;
- TARSetupTime = 0.

In all timing tables, the THCLK is the HCLK clock period.

**Figure 34. NAND controller read timings**



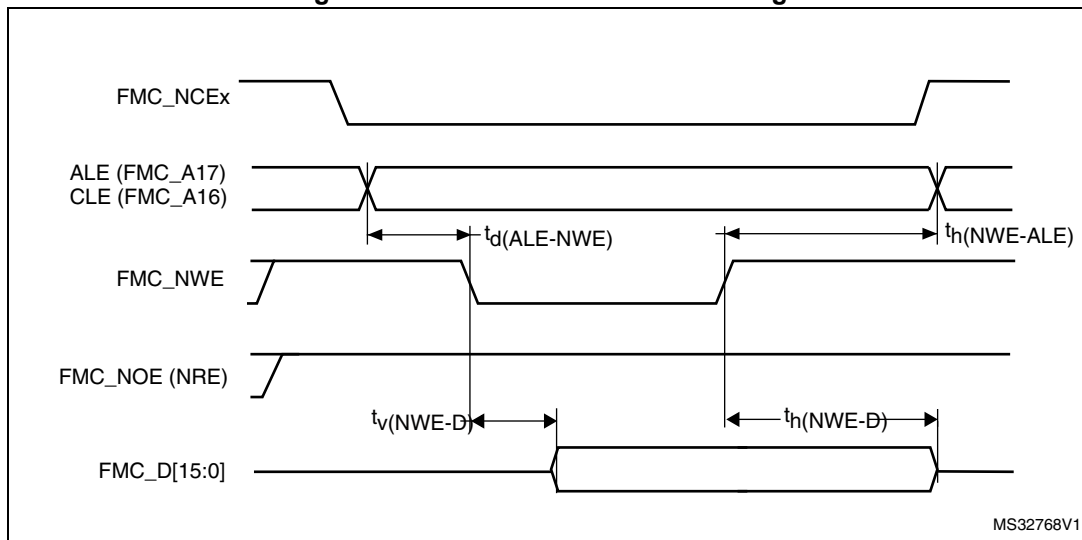
MS32767V1

**Table 59. Switching characteristics for NAND Flash read cycles<sup>(1) (2)</sup>**

| Symbol           | Parameter                                  | Min      | Max         | Unit |
|------------------|--|----------|-------------|------|
| $t_{w(NOE)}$     | FMC_NOE low width                          | 6THCLK   | 6THCLK + 2  | ns   |
| $t_{su(D-NOE)}$  | FMC_D[15-0] valid data before FMC_NOE high | THCLK+5  | -           |      |
| $t_{h(NOE-D)}$   | FMC_D[15-0] valid data after FMC_NOE high  | 0        | -           |      |
| $t_{d(ALE-NOE)}$ | FMC_ALE valid before FMC_NOE low           | -        | 6THCLK -0.5 |      |
| $t_{h(NOE-ALE)}$ | FMC_NWE high to FMC_ALE invalid            | 6THCLK-1 | -           |      |

1. Based on characterization, not tested in production.
2. CL = 30 pF

**Figure 35. NAND controller write timings**



**Table 60. Switching characteristics for NAND Flash write cycles<sup>(1)</sup>**

| Symbol            | Parameter                             | Min         | Max          | Unit |
|-------------------|---------------------------------------|-------------|--------------|------|
| $t_{w(NWE)}$      | FMC_NWE low width                     | 4THCLK-0.5  | 4THCLK + 1.5 | ns   |
| $t_{v(NWE-D)}$    | FMC_NWE low to FMC_D[15-0] valid      | -           | 3.5          |      |
| $t_{h(NWE-D)}$    | FMC_NWE high to FMC_D[15-0] invalid   | 3THCLK -1.5 | -            |      |
| $t_{d(D-NWE)}$    | FMC_D[15-0] valid before FMC_NWE high | 5THCLK - 3  | -            |      |
| $t_{d(ALE\_NWE)}$ | FMC_ALE valid before FMC_NWE low      | -           | 4THCLK+2     |      |
| $t_{h(NWE-ALE)}$  | FMC_NWE high to FMC_ALE invalid       | 2THCLK-1    | -            |      |

1. Based on characterization, not tested in production.

### 6.3.12 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

#### Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling two LEDs through I/O ports), the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to  $V_{DD}$  and  $V_{SS}$  through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in [Table 61](#). They are based on the EMS levels and classes defined in application note AN1709.

**Table 61. EMS characteristics**

| Symbol     | Parameter   | Conditions  | Level/Class |
|------------|---|---|-------------|
| $V_{FESD}$ | Voltage limits to be applied on any I/O pin to induce a functional disturbance  | $V_{DD} = 3.3\text{ V}$ , LQFP144, $T_A = +25^\circ\text{C}$ ,<br>$f_{HCLK} = 72\text{ MHz}$<br>conforms to IEC 61000-4-2 | 2B          |
| $V_{EFTB}$ | Fast transient voltage burst limits to be applied through 100 pF on $V_{DD}$ and $V_{SS}$ pins to induce a functional disturbance | $V_{DD} = 3.3\text{ V}$ , LQFP144, $T_A = +25^\circ\text{C}$ ,<br>$f_{HCLK} = 72\text{ MHz}$<br>conforms to IEC 61000-4-4 | 4A          |

#### Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and pre qualification tests in relation with the EMC level requested for his application.

#### Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

**Pre qualification trials**

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

**Electromagnetic Interference (EMI)**

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

**Table 62. EMI characteristics**

| Symbol           | Parameter  | Conditions  | Monitored frequency band | Max vs. [f <sub>HSE</sub> /f <sub>HCLK</sub> ] | Unit |
|------------------|------------|---|--------------------------|--|------|
|                  |            |   |                          | 8/72 MHz                                       |      |
| S <sub>EMI</sub> | Peak level | V <sub>DD</sub> = 3.6 V, T <sub>A</sub> = 25 °C, LQFP144 package compliant with IEC 61967-2 | 0.1 to 30 MHz            | 7  | dBμV |
|                  |            |   | 30 to 130 MHz            | 15   |      |
|                  |            |   | 130 MHz to 1GHz          | 31   |      |
|                  |            |   | SAE EMI Level            | 4  | -    |

**6.3.13 Electrical sensitivity characteristics**

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed to determine its performance in terms of electrical sensitivity.

**Electrostatic discharge (ESD)**

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the ANSI/JEDEC standard.

**Table 63. ESD absolute maximum ratings**

| Symbol                | Ratings   | Conditions   | Class | Maximum value <sup>(1)</sup> | Unit |
|-----------------------|---|--|-------|------------------------------|------|
| V <sub>ESD(HBM)</sub> | Electrostatic discharge voltage (human body model)    | T <sub>A</sub> = +25 °C, conforming to ANSI/JEDEC JS-001 | 2     | 2000                         | V    |
| V <sub>ESD(CDM)</sub> | Electrostatic discharge voltage (charge device model) | T <sub>A</sub> = +25 °C, conforming to ANSI/ESD STM5.3.1 | C3    | 250                          |      |

1. Data based on characterization results, not tested in production.

### Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latch-up standard.

**Table 64. Electrical sensitivities**

| Symbol | Parameter             | Conditions                                     | Class      |
|--------|-----------------------|--|------------|
| LU     | Static latch-up class | T <sub>A</sub> = +105 °C conforming to JESD78A | II Level A |

### 6.3.14 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V<sub>SS</sub> or above V<sub>DD</sub> (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

#### Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of -5 µA/+0 µA range), or other functional failure (for example reset occurrence or oscillator frequency deviation).

The test results are given in [Table 65](#).

**Table 65. I/O current injection susceptibility**

| Symbol           | Description   | Functional susceptibility |                    | Unit |
|------------------|---|---------------------------|--------------------|------|
|                  |   | Negative injection        | Positive injection |      |
| I <sub>INJ</sub> | Injected current on BOOT0   | -0                        | NA                 | mA   |
|                  | Injected current on PF3, PC1, PC2, PA1, PA2, PA3, PA4, PA5, PA6, PA7, PB0, PB1, PE8, PE9, PE10, PE11, PE12, PE13, PE14, PE15, PB13, PB14, PB15, PD8, PD9, PD10, PD11, PD12, PD13, PD14 pins with induced leakage current on adjacent pins less than -50 µA or more than +400 µA | -5                        | +5                 |      |
|                  | Injected current on PF2, PF4, PC0, PC1, PC2, PC3, PA0, PA1, PA2, PA3, PA4, PA5, PA6, PA7, PC4, PC5, PB2, PB11 with induced leakage current on other pins from this group less than -50 µA or more than +400 µA  | -5                        | +5                 |      |



**Table 65. I/O current injection susceptibility (continued)**

| Symbol           | Description   | Functional susceptibility |                    | Unit |
|------------------|---|---------------------------|--------------------|------|
|                  |   | Negative injection        | Positive injection |      |
| I <sub>INJ</sub> | Injected current on PB0, PB1, PE7, PE8, PE9, PE10, PE11, PE12, PE13, PE14, PE15, PB12, PB13, PB14, P15, PD8, PD9, PD10, PD11, PD12, PD13, PD14 with induced leakage current on other pins from this group less than -50 µA or more than +400 µA | -5                        | +5                 | mA   |
|                  | Injected current on any other FT and FTf pins   | -5                        | NA                 |      |
|                  | Injected current on any other pins  | -5                        | +5                 |      |

*Note:* It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.

### 6.3.15 I/O port characteristics

#### General input/output characteristics

Unless otherwise specified, the parameters given in [Table 66](#) are derived from tests performed under the conditions summarized in [Table 19](#). All I/Os are CMOS and TTL compliant.

**Table 66. I/O static characteristics**

| Symbol           | Parameter                  | Conditions            | Min   | Typ                | Max                                       | Unit |
|------------------|----------------------------|-----------------------|---|--------------------|---|------|
| V <sub>IL</sub>  | Low level input voltage    | TC and TTa I/O        | -   | -                  | 0.3 V <sub>DD</sub> +0.07 <sup>(1)</sup>  | V    |
|                  |                            | FT and FTf I/O        | -   | -                  | 0.475 V <sub>DD</sub> -0.2 <sup>(1)</sup> |      |
|                  |                            | BOOT0                 | -   | -                  | 0.3 V <sub>DD</sub> -0.3 <sup>(1)</sup>   |      |
|                  |                            | All I/Os except BOOT0 | -   | -                  | 0.3 V <sub>DD</sub> <sup>(2)</sup>        |      |
| V <sub>IH</sub>  | High level input voltage   | TC and TTa I/O        | 0.445 V <sub>DD</sub> +0.398 <sup>(1)</sup> | -                  | -   | V    |
|                  |                            | FT and FTf I/O        | 0.5 V <sub>DD</sub> +0.2 <sup>(1)</sup>     | -                  | -   |      |
|                  |                            | BOOT0                 | 0.2 V <sub>DD</sub> +0.95 <sup>(1)</sup>    | -                  | -   |      |
|                  |                            | All I/Os except BOOT0 | 0.7 V <sub>DD</sub> <sup>(2)</sup>          | -                  | -   |      |
| V <sub>hys</sub> | Schmitt trigger hysteresis | TC and TTa I/O        | -   | 200 <sup>(1)</sup> | -   | mV   |
|                  |                            | FT and FTf I/O        | -   | 100 <sup>(1)</sup> | -   |      |
|                  |                            | BOOT0                 | -   | 300 <sup>(1)</sup> | -   |      |

Table 66. I/O static characteristics (continued)

| Symbol    | Parameter   | Conditions  | Min | Typ | Max  | Unit |
|-----------|---|---|-----|-----|------|------|
| $I_{lkg}$ | Input leakage current <sup>(3)</sup>              | TC, FT and FTf I/O<br>TTa I/O in digital mode<br>$V_{SS} \leq V_{IN} \leq V_{DD}$ | -   | -   | ±0.1 | µA   |
|           |   | TTa I/O in digital mode<br>$V_{DD} \leq V_{IN} \leq V_{DDA}$                      | -   | -   | 1    |      |
|           |   | TTa I/O in analog mode<br>$V_{SS} \leq V_{IN} \leq V_{DDA}$                       | -   | -   | ±0.2 |      |
|           |   | FT and FTf I/O <sup>(4)</sup><br>$V_{DD} \leq V_{IN} \leq 5\text{ V}$             | -   | -   | 10   |      |
| $R_{PU}$  | Weak pull-up equivalent resistor <sup>(5)</sup>   | $V_{IN} = V_{SS}$   | 25  | 40  | 55   | kΩ   |
| $R_{PD}$  | Weak pull-down equivalent resistor <sup>(5)</sup> | $V_{IN} = V_{DD}$   | 25  | 40  | 55   | kΩ   |
| $C_{IO}$  | I/O pin capacitance                               | -   | -   | 5   | -    | pF   |

1. Data based on design simulation.
2. Tested in production.
3. Leakage could be higher than the maximum value, if negative current is injected on adjacent pins. Refer to [Table 65: I/O current injection susceptibility](#).
4. To sustain a voltage higher than  $V_{DD} + 0.3\text{ V}$ , the internal pull-up/pull-down resistors must be disabled.
5. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimum (~10% order).

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in [Figure 36](#) and [Figure 37](#) for standard I/Os.

Figure 36. TC and TTa I/O input characteristics - CMOS port

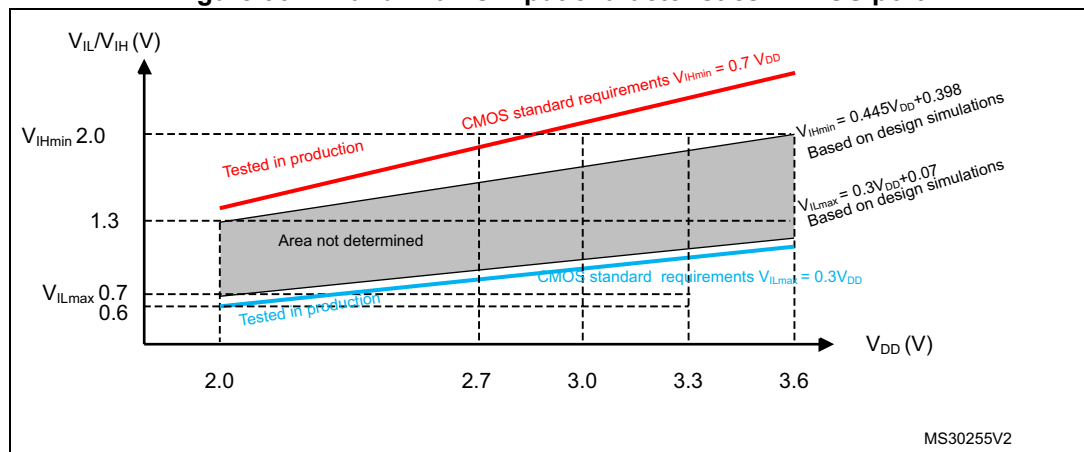


Figure 37. TC and TTa I/O input characteristics - TTL port

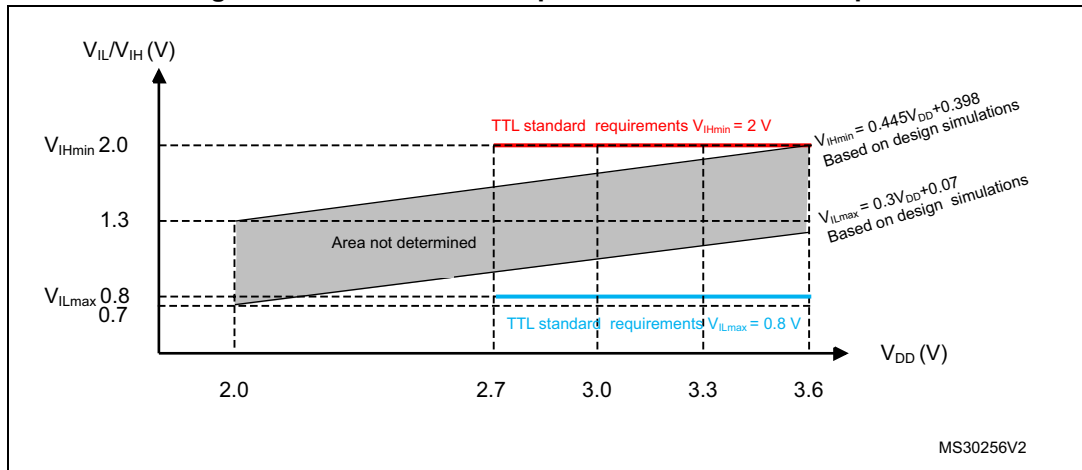


Figure 38. Five volt tolerant (FT and FTf) I/O input characteristics - CMOS port

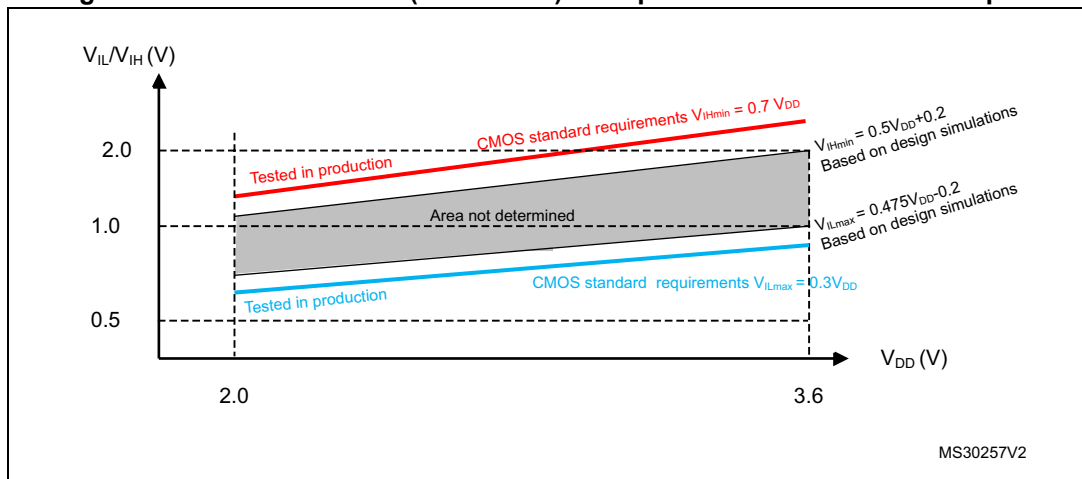
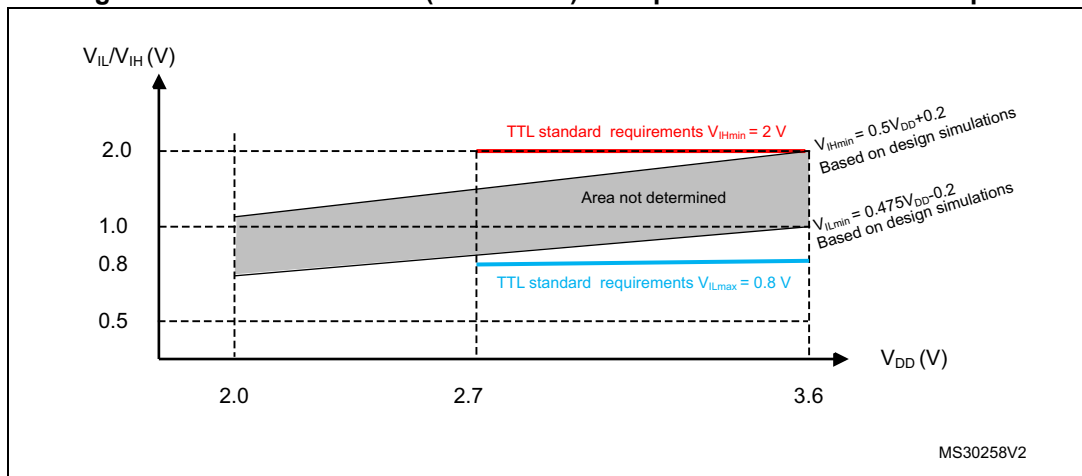


Figure 39. Five volt tolerant (FT and FTf) I/O input characteristics - TTL port



### Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to +/-8 mA, and sink or source up to +/- 20 mA (with a relaxed  $V_{OL}/V_{OH}$ ).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in [Section 6.2](#):

- The sum of the currents sourced by all the I/Os on  $V_{DD}$ , plus the maximum Run consumption of the MCU sourced on  $V_{DD}$ , cannot exceed the absolute maximum rating  $\Sigma I_{VDD}$  (see [Table 17](#)).
- The sum of the currents sunk by all the I/Os on  $V_{SS}$  plus the maximum Run consumption of the MCU sunk on  $V_{SS}$  cannot exceed the absolute maximum rating  $\Sigma I_{VSS}$  (see [Table 17](#)).

### Output voltage levels

Unless otherwise specified, the parameters given in [Table 67](#) are derived from tests performed under ambient temperature and  $V_{DD}$  supply voltage conditions summarized in [Table 19](#). All I/Os (FT, TTA and TC unless otherwise specified) are CMOS and TTL compliant.

**Table 67. Output voltage characteristics**

| Symbol               | Parameter   | Conditions  | Min          | Max | Unit |
|----------------------|---|---|--------------|-----|------|
| $V_{OL}^{(1)}$       | Output low level voltage for an I/O pin                 | CMOS port <sup>(2)</sup><br>$I_{IO} = +48 \text{ mA}$<br>$2.7 \text{ V} < V_{DD} < 3.6 \text{ V}$ | -            | 0.4 | V    |
| $V_{OH}^{(3)}$       | Output high level voltage for an I/O pin                |   | $V_{DD}-0.4$ | -   |      |
| $V_{OL}^{(1)}$       | Output low level voltage for an I/O pin                 | TTL port <sup>(2)</sup><br>$I_{IO} = +8 \text{ mA}$<br>$2.7 \text{ V} < V_{DD} < 3.6 \text{ V}$   | -            | 0.4 |      |
| $V_{OH}^{(3)}$       | Output high level voltage for an I/O pin                |   | 2.4          | -   |      |
| $V_{OL}^{(1)(4)}$    | Output low level voltage for an I/O pin                 | $I_{IO} = +20 \text{ mA}$<br>$2.7 \text{ V} < V_{DD} < 3.6 \text{ V}$                             | -            | 1.3 |      |
| $V_{OH}^{(3)(4)}$    | Output high level voltage for an I/O pin                |   | $V_{DD}-1.3$ | -   |      |
| $V_{OL}^{(1)(4)}$    | Output low level voltage for an I/O pin                 | $I_{IO} = +6 \text{ mA}$<br>$2 \text{ V} < V_{DD} < 2.7 \text{ V}$                                | -            | 0.4 |      |
| $V_{OH}^{(3)(4)}$    | Output high level voltage for an I/O pin                |   | $V_{DD}-0.4$ | -   |      |
| $V_{OLFM+}^{(4)(4)}$ | Output low level voltage for an FTf I/O pin in FM+ mode | $I_{IO} = +20 \text{ mA}$<br>$2.7 \text{ V} < V_{DD} < 3.6 \text{ V}$                             | -            | 0.4 |      |

1. The  $I_{IO}$  current sunk by the device must always respect the absolute maximum rating specified in [Table 17](#) and the sum of  $I_{IO}$  (I/O ports and control pins) must not exceed  $\Sigma I_{IO(PIN)}$ .
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. The  $I_{IO}$  current sourced by the device must always respect the absolute maximum rating specified in [Table 17](#) and the sum of  $I_{IO}$  (I/O ports and control pins) must not exceed  $\Sigma I_{IO(PIN)}$ .
4. Data based on design simulation.

**Input/output AC characteristics**

The definition and values of input/output AC characteristics are given in [Figure 40](#) and [Table 68](#), respectively.

Unless otherwise specified, the parameters given are derived from tests performed under ambient temperature and  $V_{DD}$  supply voltage conditions summarized in [Table 19](#).

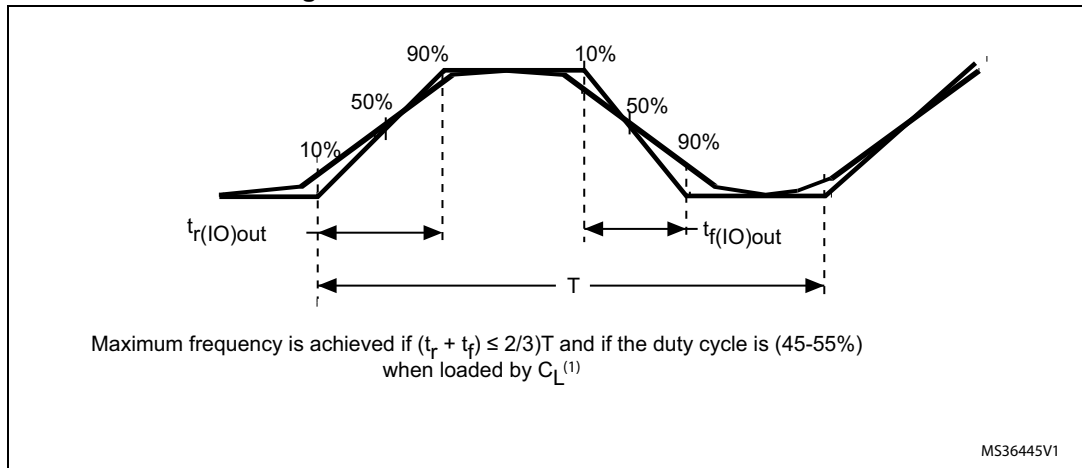
**Table 68. I/O AC characteristics<sup>(1)</sup>**

| OSPEEDRx [1:0] value <sup>(1)</sup> | Symbol           | Parameter   | Conditions  | Min        | Max         | Unit |
|-------------------------------------|------------------|---|---|------------|-------------|------|
| x0                                  | $f_{max(IO)out}$ | Maximum frequency <sup>(2)</sup>                                | $C_L = 50 \text{ pF}, V_{DD} = 2 \text{ V to } 3.6 \text{ V}$   | -          | $2^{(3)}$   | MHz  |
|                                     | $t_{f(IO)out}$   | Output high to low level fall time                              | $C_L = 50 \text{ pF}, V_{DD} = 2 \text{ V to } 3.6 \text{ V}$   | -          | $125^{(3)}$ | ns   |
|                                     | $t_{r(IO)out}$   | Output low to high level rise time                              |   | -          | $125^{(3)}$ |      |
| 01                                  | $f_{max(IO)out}$ | Maximum frequency <sup>(2)</sup>                                | $C_L = 50 \text{ pF}, V_{DD} = 2 \text{ V to } 3.6 \text{ V}$   | -          | $10^{(3)}$  | MHz  |
|                                     | $t_{f(IO)out}$   | Output high to low level fall time                              | $C_L = 50 \text{ pF}, V_{DD} = 2 \text{ V to } 3.6 \text{ V}$   | -          | $25^{(3)}$  | ns   |
|                                     | $t_{r(IO)out}$   | Output low to high level rise time                              |   | -          | $25^{(3)}$  |      |
| 11                                  | $f_{max(IO)out}$ | Maximum frequency <sup>(2)</sup>                                | $C_L = 30 \text{ pF}, V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$ | -          | $50^{(3)}$  | MHz  |
|                                     |                  |   | $C_L = 50 \text{ pF}, V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$ | -          | $30^{(3)}$  |      |
|                                     |                  |   | $C_L = 50 \text{ pF}, V_{DD} = 2 \text{ V to } 2.7 \text{ V}$   | -          | $20^{(3)}$  |      |
|                                     | $t_{f(IO)out}$   | Output high to low level fall time                              | $C_L = 30 \text{ pF}, V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$ | -          | $5^{(3)}$   | ns   |
|                                     |                  |   | $C_L = 50 \text{ pF}, V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$ | -          | $8^{(3)}$   |      |
|                                     |                  |   | $C_L = 50 \text{ pF}, V_{DD} = 2 \text{ V to } 2.7 \text{ V}$   | -          | $12^{(3)}$  |      |
|                                     | $t_{r(IO)out}$   | Output low to high level rise time                              | $C_L = 30 \text{ pF}, V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$ | -          | $5^{(3)}$   |      |
|                                     |                  |   | $C_L = 50 \text{ pF}, V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$ | -          | $8^{(3)}$   |      |
|                                     |                  |   | $C_L = 50 \text{ pF}, V_{DD} = 2 \text{ V to } 2.7 \text{ V}$   | -          | $12^{(3)}$  |      |
| FM+ configuration <sup>(4)</sup>    | $f_{max(IO)out}$ | Maximum frequency <sup>(2)</sup>                                | $C_L = 50 \text{ pF}, V_{DD} = 2 \text{ to } 3.6 \text{ V}$     | -          | $2^{(4)}$   | MHz  |
|                                     | $t_{f(IO)out}$   | Output high to low level fall time                              |   | -          | $12^{(4)}$  | ns   |
|                                     | $t_{r(IO)out}$   | Output low to high level rise time                              |   | -          | $34^{(4)}$  |      |
| -                                   | $t_{EXTIpw}$     | Pulse width of external signals detected by the EXTI controller | -   | $10^{(3)}$ | -           | ns   |

1. The I/O speed is configured using the OSPEEDRx[1:0] bits. Refer to the RM0365 reference manual for a description of GPIO Port configuration register.
2. The maximum frequency is defined in [Figure 40](#).
3. Guaranteed by design, not tested in production.
4. The I/O speed configuration is bypassed in FM+ I/O mode. Refer to the reference manual RM0365 for a description of FM+ I/O mode configuration.



Figure 40. I/O AC characteristics definition



1. See [Table 68: I/O AC characteristics](#).

### 6.3.16 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor,  $R_{PU}$  (see [Table 66](#)).

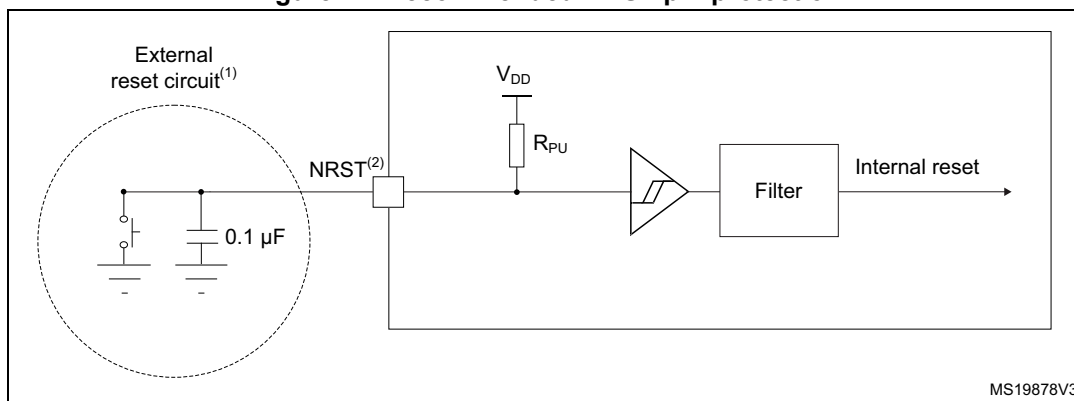
Unless otherwise specified, the parameters given in [Table 69](#) are derived from tests performed under ambient temperature and  $V_{DD}$  supply voltage conditions summarized in [Table 19](#).

Table 69. NRST pin characteristics

| Symbol               | Parameter                                       | Conditions        | Min                         | Typ | Max                      | Unit       |
|----------------------|---|-------------------|-----------------------------|-----|--------------------------|------------|
| $V_{IL(NRST)}^{(1)}$ | NRST Input low level voltage                    | -                 | -                           | -   | $0.3V_{DD} + 0.07^{(1)}$ | V          |
| $V_{IH(NRST)}^{(1)}$ | NRST Input high level voltage                   | -                 | $0.445V_{DD} + 0.398^{(1)}$ | -   | -                        |            |
| $V_{hys(NRST)}$      | NRST Schmitt trigger voltage hysteresis         | -                 | -                           | 200 | -                        | mV         |
| $R_{PU}$             | Weak pull-up equivalent resistor <sup>(2)</sup> | $V_{IN} = V_{SS}$ | 25                          | 40  | 55                       | k $\Omega$ |
| $V_{F(NRST)}^{(1)}$  | NRST Input filtered pulse                       | -                 | -                           | -   | $100^{(1)}$              | ns         |
| $V_{NF(NRST)}^{(1)}$ | NRST Input not filtered pulse                   | -                 | $500^{(1)}$                 | -   | -                        | ns         |

1. Guaranteed by design, not tested in production.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).

Figure 41. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the  $V_{IL(NRST)}$  max level specified in Table 69. Otherwise the reset is not taken into account by the device.
3. Place the external capacitor 0.1u F on NRST as close as possible to the chip.

### 6.3.17 Timer characteristics

The parameters given in Table 70 are guaranteed by design.

Refer to Section 6.3.15: I/O port characteristics for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 70. TIMx<sup>(1)(2)</sup> characteristics

| Symbol             | Parameter                                    | Conditions                      | Min    | Max                  | Unit          |
|--------------------|--|---------------------------------|--------|----------------------|---------------|
| $t_{res(TIM)}$     | Timer resolution time                        | -                               | 1      | -                    | $t_{TIMxCLK}$ |
|                    |  | $f_{TIMxCLK} = 72 \text{ MHz}$  | 13.9   | -                    | ns            |
|                    |  | $f_{TIMxCLK} = 144 \text{ MHz}$ | 6.95   | -                    | ns            |
| $f_{EXT}$          | Timer external clock frequency on CH1 to CH4 | -                               | 0      | $f_{TIMxCLK}/2$      | MHz           |
|                    |  | $f_{TIMxCLK} = 72 \text{ MHz}$  | 0      | 36                   | MHz           |
| Res <sub>TIM</sub> | Timer resolution                             | TIMx (except TIM2)              | -      | 16                   | bit           |
|                    |  | TIM2                            | -      | 32                   |               |
| $t_{COUNTER}$      | 16-bit counter clock period                  | -                               | 1      | 65536                | $t_{TIMxCLK}$ |
|                    |  | $f_{TIMxCLK} = 72 \text{ MHz}$  | 0.0139 | 910                  | μs            |
|                    |  | $f_{TIMxCLK} = 144 \text{ MHz}$ | 0.0069 | 455                  | μs            |
| $t_{MAX\_COUNT}$   | Maximum possible count with 32-bit counter   | -                               | -      | $65536 \times 65536$ | $t_{TIMxCLK}$ |
|                    |  | $f_{TIMxCLK} = 72 \text{ MHz}$  | -      | 59.65                | s             |
|                    |  | $f_{TIMxCLK} = 144 \text{ MHz}$ | -      | 29.825               | s             |

1. TIMx is used as a general term to refer to the TIM1, TIM2, TIM3, TIM4, TIM15, TIM16 and TIM17 timers.
2. Guaranteed by design, not tested in production.

Table 71. IWDG min/max timeout period at 40 kHz (LSI) <sup>(1)</sup>

| Prescaler divider | PR[2:0] bits | Min timeout (ms) RL[11:0]=<br>0x000 | Max timeout (ms) RL[11:0]=<br>0xFFFF |
|-------------------|--------------|-------------------------------------|--------------------------------------|
| /4                | 0            | 0.1                                 | 409.6                                |
| /8                | 1            | 0.2                                 | 819.2                                |
| /16               | 2            | 0.4                                 | 1638.4                               |
| /32               | 3            | 0.8                                 | 3276.8                               |
| /64               | 4            | 1.6                                 | 6553.6                               |
| /128              | 5            | 3.2                                 | 13107.2                              |
| /256              | 7            | 6.4                                 | 26214.4                              |

1. These timings are given for a 40 kHz clock but the microcontroller internal RC frequency can vary from 30 to 60 kHz. Moreover, given an exact RC oscillator frequency, the exact timings still depend on the phasing of the APB interface clock versus the LSI clock so that there is always a full RC period of uncertainty.

Table 72. WWDG min-max timeout value @72 MHz (PCLK)<sup>(1)</sup>

| Prescaler | WDGTB | Min timeout value | Max timeout value |
|-----------|-------|-------------------|-------------------|
| 1         | 0     | 0.05687           | 3.6409            |
| 2         | 1     | 0.1137            | 7.2817            |
| 4         | 2     | 0.2275            | 14.564            |
| 8         | 3     | 0.4551            | 29.127            |

1. Guaranteed by design, not tested in production.

### 6.3.18 Communications interfaces

#### I<sup>2</sup>C interface characteristics

The I<sup>2</sup>C interface meets the timings requirements of the I<sup>2</sup>C-bus specification and user manual rev.03 for:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+): with a bit rate up to 1Mbits/s

The I<sup>2</sup>C timings requirements are guaranteed by design when the I<sup>2</sup>C peripheral is properly configured (refer to Reference manual).

The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and VDDIOx is disabled, but is still present. Only FtI I/O pins support Fm+ low level output current maximum requirement. Refer to [Section 6.3.15: I/O port characteristics](#).

All I<sup>2</sup>C I/Os embed an analog filter, refer to the [Table 73: I2C analog filter characteristics](#).



**Table 73. I2C analog filter characteristics<sup>(1)</sup>**

| Symbol   | Parameter  | Min | Max | Unit |
|----------|--|-----|-----|------|
| $t_{AF}$ | Pulse width of spikes that are suppressed by the analog filter | 50  | 260 | ns   |

1. Guaranteed by design, not tested in production.

**SPI/I<sup>2</sup>S characteristics**

Unless otherwise specified, the parameters given in [Table 74](#) for SPI or in [Table 75](#) for I<sup>2</sup>S are derived from tests performed under ambient temperature,  $f_{PCLKX}$  frequency and  $V_{DD}$  supply voltage conditions summarized in [Table 19](#).

Refer to [Section 6.3.15: I/O port characteristics](#) for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI and WS, CK, SD for I<sup>2</sup>S).

**Table 74. SPI characteristics<sup>(1)</sup>**

| Symbol                      | Parameter                         | Conditions  | Min           | Typ.       | Max                 | Unit |
|-----------------------------|-----------------------------------|---|---------------|------------|---------------------|------|
| $f_{SCK}$<br>$1/t_{c(SCK)}$ | SPI clock frequency               | Master mode 2.7 V < $V_{DD}$ < 3.6 V, SPI1/4                          | -             | -          | 24                  | MHz  |
|                             |                                   | Master mode 2 V < $V_{DD}$ < 3.6 V, SPI1/2/3/4                        |               |            | 18                  |      |
|                             |                                   | Slave mode 2 V < $V_{DD}$ < 3.6 V, SPI1/4                             |               |            | 24                  |      |
|                             |                                   | Slave mode 2 V < $V_{DD}$ < 3.6 V, SPI1/2/3/4                         |               |            | 18                  |      |
|                             |                                   | Slave mode transmitter/full duplex 2 V < $V_{DD}$ < 3.6 V, SPI1/2/3/4 |               |            | 16.5 <sup>(2)</sup> |      |
|                             |                                   | Slave mode transmitter/full duplex 2.7 V < $V_{DD}$ < 3.6 V, SPI1/4   |               |            | 22.5 <sup>(2)</sup> | -    |
| Duty <sub>(SCK)</sub>       | Duty cycle of SPI clock frequency | Slave mode  | 30            | 50         | 70                  | %    |
| $t_{su(NSS)}$               | NSS setup time                    | Slave mode, SPI presc = 2   | 4* $T_{pclk}$ | -          | -                   |      |
| $t_h(NSS)$                  | NSS hold time                     | Slave mode, SPI presc = 2   | 2* $T_{pclk}$ | -          | -                   |      |
| $t_w(SCKH)$<br>$t_w(SCKL)$  | SCK high and low time             | Master mode   | $T_{pclk}-2$  | $T_{pclk}$ | $T_{pclk}+2$        |      |
| $t_{su(MI)}$                | Data input setup time             | Master mode   | 3             | -          | -                   |      |
| $t_{su(SI)}$                |                                   | Slave mode  | 3             | -          | -                   |      |
| $t_h(MI)$                   | Data input hold time              | Master mode   | 6.5           | -          | -                   |      |
| $t_h(SI)$                   |                                   | Slave mode  | 4.5           | -          | -                   |      |
| $t_a(SO)$                   | Data output access time           | Slave mode  | 10            | -          | 30                  |      |
| $t_{dis(SO)}$               | Data output disable time          | Slave mode  | 8             | -          | 7                   |      |

Table 74. SPI characteristics<sup>(1)</sup> (continued)

| Symbol      | Parameter              | Conditions                          | Min | Typ. | Max | Unit |
|-------------|------------------------|-------------------------------------|-----|------|-----|------|
| $t_{v(SO)}$ | Data output valid time | Slave mode $2.7 V < V_{DD} < 3.6 V$ | -   | 15   | 22  |      |
|             |                        | Slave mode $2 V < V_{DD} < 3.6 V$   | -   | 15   | 30  |      |
| $t_{v(MO)}$ |                        | Master mode                         | -   | 2    | 4.5 |      |
| $t_{h(SO)}$ | Data output hold time  | Slave mode                          | 9   | -    | -   |      |
|             |                        | Master mode                         | 0   | -    | -   |      |
| $t_{h(MO)}$ |                        |                                     |     |      |     |      |

1. Data based on characterization results, not tested in production.
2. The maximum frequency in Slave transmitter mode is determined by the sum of  $t_{v(SO)}$  and  $t_{su(MI)}$  which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having  $t_{su(MI)} = 0$  while  $Duty_{(SCK)} = 50\%$ .

Figure 42. SPI timing diagram - slave mode and CPHA = 0

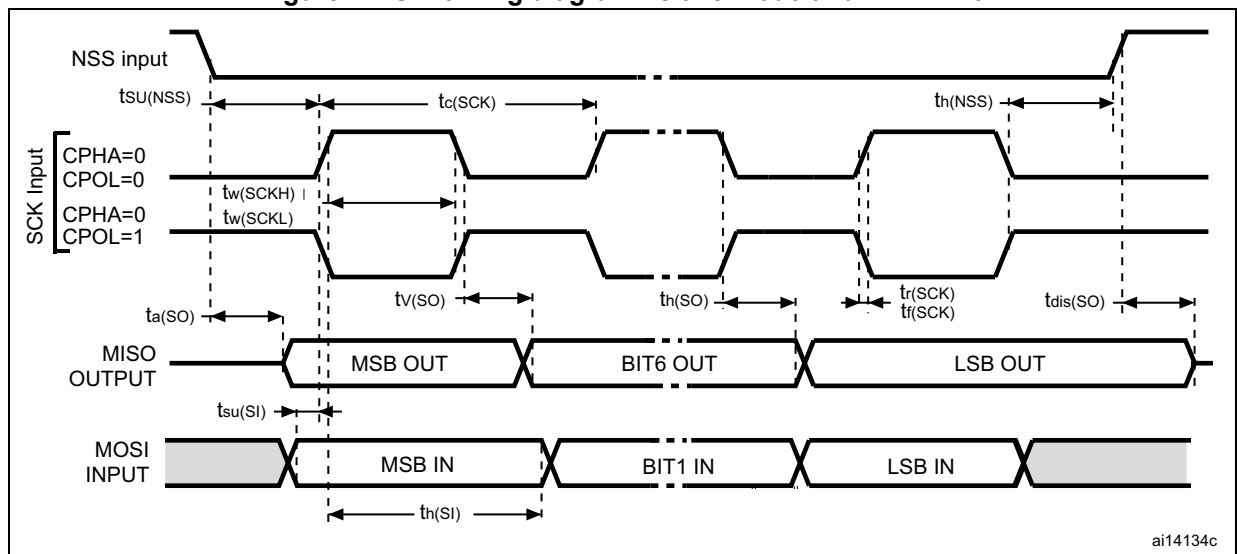
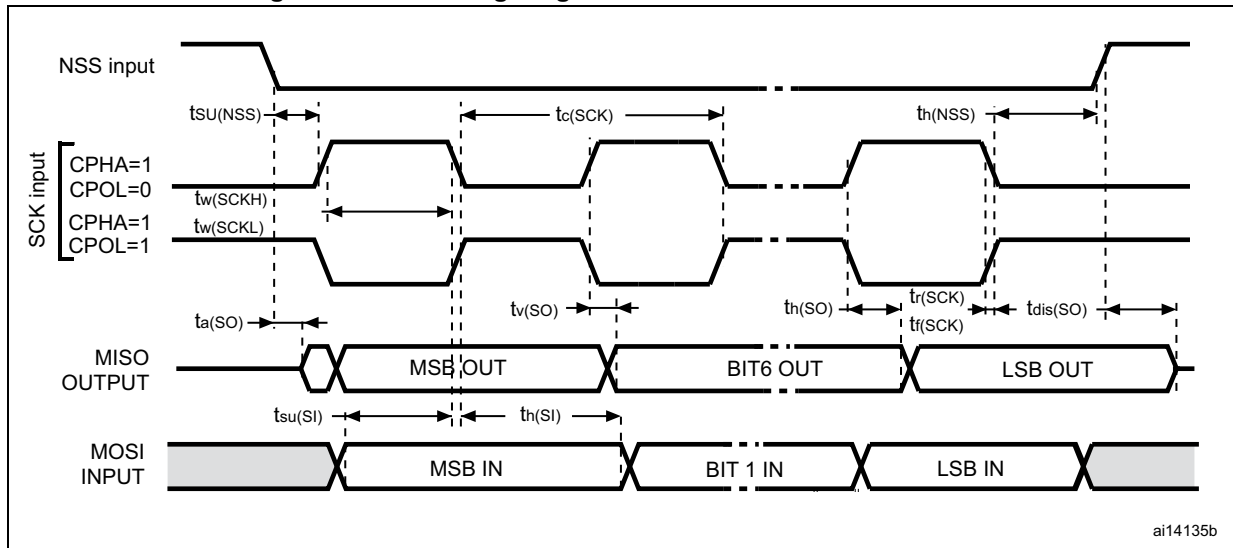
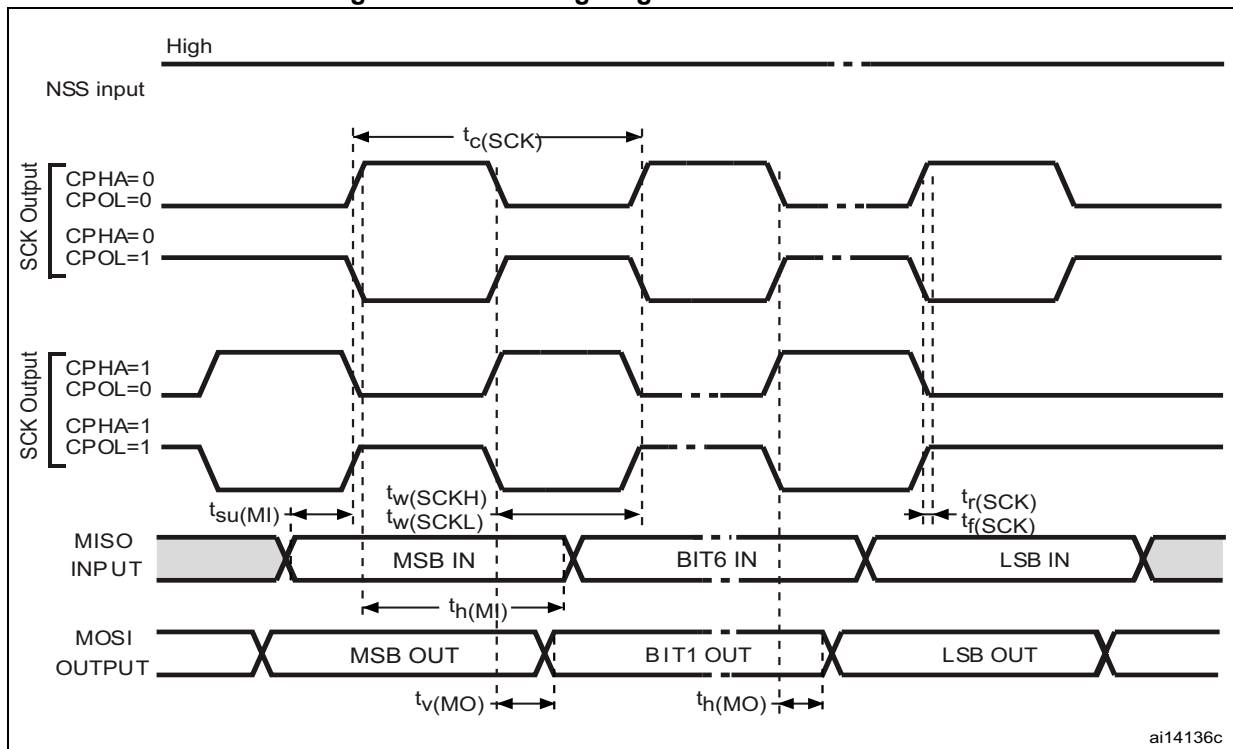


Figure 43. SPI timing diagram - slave mode and CPHA = 1<sup>(1)</sup>



1. Measurement points are done at  $0.5V_{DD}$  and with external  $C_L = 30$  pF.

Figure 44. SPI timing diagram - master mode<sup>(1)</sup>



1. Measurement points are done at  $0.5V_{DD}$  and with external  $C_L = 30$  pF.

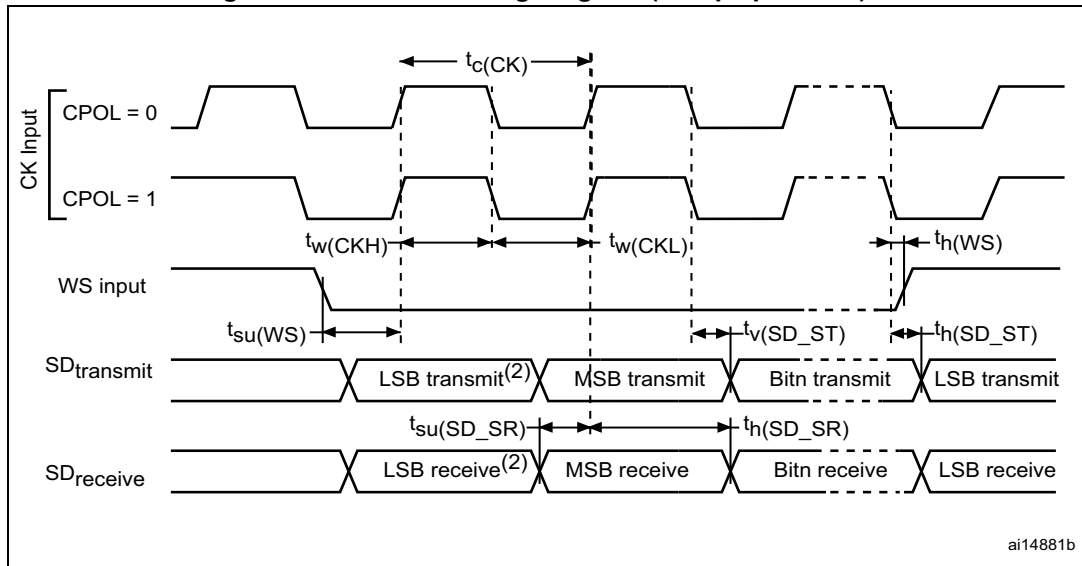
Table 75. I<sup>2</sup>S characteristics<sup>(1)</sup>

| Symbol                 | Parameter                      | Conditions                             | Min      | Max                   | Unit |
|------------------------|--------------------------------|--|----------|-----------------------|------|
| f <sub>MCK</sub>       | I2S Main clock output          | -                                      | 256 x 8K | 256xFs <sup>(2)</sup> | MHz  |
| f <sub>CK</sub>        | I2S clock frequency            | Master data: 32 bits                   | -        | 64xFs                 | MHz  |
|                        |                                | Slave data: 32 bits                    | -        | 64xFs                 | -    |
| D <sub>CK</sub>        | I2S clock frequency duty cycle | Slave receiver                         | 30       | 70                    | %    |
| t <sub>v(WS)</sub>     | WS valid time                  | Master mode                            | -        | 20                    | ns   |
| t <sub>h(WS)</sub>     | WS hold time                   | Master mode                            | 2        | -                     |      |
| t <sub>su(WS)</sub>    | WS setup time                  | Slave mode                             | 0        | -                     |      |
| t <sub>h(WS)</sub>     | WS hold time                   | Slave mode                             | 4        | -                     |      |
| t <sub>su(SD_MR)</sub> | Data input setup time          | Master receiver                        | 1        | -                     |      |
| t <sub>su(SD_SR)</sub> |                                | Slave receiver                         | 1        | -                     |      |
| t <sub>h(SD_MR)</sub>  | Data input hold time           | Master receiver                        | 8        | -                     |      |
| t <sub>h(SD_SR)</sub>  |                                | Slave receiver                         | 2.5      | -                     |      |
| t <sub>v(SD_ST)</sub>  | Data output valid time         | Slave transmitter (after enable edge)  | -        | 50                    |      |
| t <sub>v(SD_MT)</sub>  |                                | Master transmitter (after enable edge) | -        | 22                    |      |
| t <sub>h(SD_ST)</sub>  | Data output hold time          | Slave transmitter (after enable edge)  | 8        | -                     |      |
| t <sub>h(SD_MT)</sub>  |                                | Master transmitter (after enable edge) | 1        | -                     |      |

1. Data based on characterization results, not tested in production.
2. 256xFs maximum is 36 MHz (APB1 Maximum frequency)

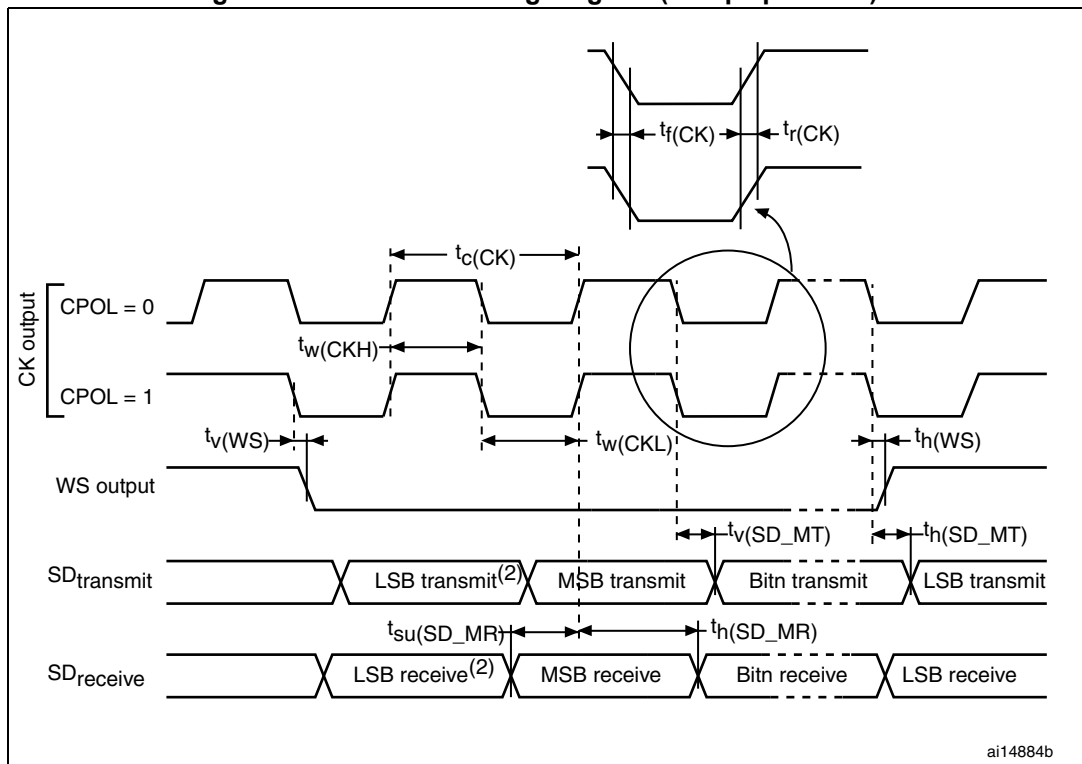
**Note:** Refer to the I<sup>2</sup>S section in RM0365 Reference Manual for more details about the sampling frequency (Fs), f<sub>MCK</sub>, f<sub>CK</sub>, DCK values reflect only the digital peripheral behavior, source clock precision might slightly change the values DCK depends mainly on ODD bit value. Digital contribution leads to a min of (I2SDIV/(2\*I2SDIV+ODD)) and a max of (I2SDIV+ODD)/(2\*I2SDIV+ODD) and Fs max supported for each mode/condition.

Figure 45. I<sup>2</sup>S slave timing diagram (Philips protocol)<sup>(1)</sup>



1. Measurement points are done at 0.5V<sub>DD</sub> and with external C<sub>L</sub>=30 pF.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 46. I<sup>2</sup>S master timing diagram (Philips protocol)<sup>(1)</sup>



1. Measurement points are done at 0.5V<sub>DD</sub> and with external C<sub>L</sub>=30 pF.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

USB characteristics

Table 76. USB startup time

| Symbol              | Parameter                    | Max | Unit    |
|---------------------|------------------------------|-----|---------|
| $t_{STARTUP}^{(1)}$ | USB transceiver startup time | 1   | $\mu s$ |

1. Guaranteed by design, not tested in production.

Table 77. USB DC electrical characteristics

| Symbol               | Parameter                            | Conditions                                      | Min. <sup>(1)</sup> | Max. <sup>(1)</sup> | Unit |
|----------------------|--------------------------------------|---|---------------------|---------------------|------|
| <b>Input levels</b>  |                                      |   |                     |                     |      |
| $V_{DD}$             | USB operating voltage <sup>(2)</sup> | -   | 3.0 <sup>(3)</sup>  | 3.6                 | V    |
| $V_{DI}^{(4)}$       | Differential input sensitivity       | I(USB_DP, USB_DM)                               | 0.2                 | -                   | V    |
| $V_{CM}^{(4)}$       | Differential common mode range       | Includes $V_{DI}$ range                         | 0.8                 | 2.5                 |      |
| $V_{SE}^{(4)}$       | Single ended receiver threshold      | -   | 1.3                 | 2.0                 |      |
| <b>Output levels</b> |                                      |   |                     |                     |      |
| $V_{OL}$             | Static output level low              | $R_L$ of 1.5 k $\Omega$ to 3.6 V <sup>(5)</sup> | -                   | 0.3                 | V    |
| $V_{OH}$             | Static output level high             | $R_L$ of 15 k $\Omega$ to $V_{SS}^{(5)}$        | 2.8                 | 3.6                 |      |

- All the voltages are measured from the local ground potential.
- To be compliant with the USB 2.0 full-speed electrical specification, the USB\_DP (D+) pin should be pulled up with a 1.5 k $\Omega$  resistor to a 3.0-to-3.6 V voltage range.
- The STM32F302xD/E USB functionality is ensured down to 2.7 V but not the full USB electrical characteristics which are degraded in the 2.7-to-3.0 V  $V_{DD}$  voltage range.
- Guaranteed by design, not tested in production.
- $R_L$  is the load connected on the USB drivers.

Figure 47. USB timings: definition of data signal rise and fall time

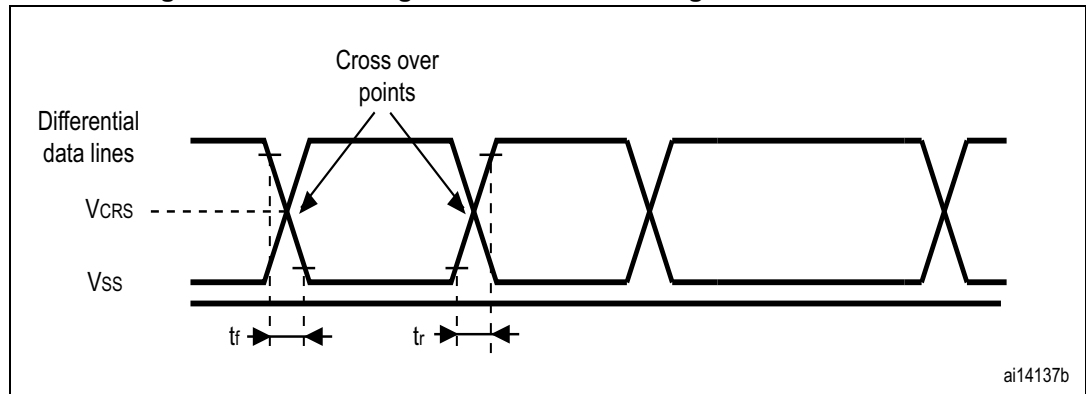


Table 78. USB: full-speed electrical characteristics<sup>(1)</sup>

| Symbol                        | Parameter                | Conditions    | Min | Typ | Max | Unit |
|-------------------------------|--------------------------|---------------|-----|-----|-----|------|
| <b>Driver characteristics</b> |                          |               |     |     |     |      |
| $t_r$                         | Rise time <sup>(2)</sup> | $C_L = 50$ pF | 4   | -   | 20  | ns   |
| $t_f$                         | Fall time <sup>(2)</sup> | $C_L = 50$ pF | 4   | -   | 20  | ns   |

**Table 78. USB: full-speed electrical characteristics<sup>(1)</sup> (continued)**

| Symbol                                 | Parameter                       | Conditions           | Min | Typ | Max | Unit     |
|--|---------------------------------|----------------------|-----|-----|-----|----------|
| $t_{rfm}$                              | Rise/ fall time matching        | $t_r/t_f$            | 90  | -   | 110 | %        |
| $V_{CRS}$                              | Output signal crossover voltage | -                    | 1.3 | -   | 2.0 | V        |
| Output driver Impedance <sup>(3)</sup> | $Z_{DRV}$                       | driving high and low | 28  | 40  | 44  | $\Omega$ |

1. Guaranteed by design, not tested in production.
2. Measured from 10% to 90% of the data signal. For more detailed information, refer to USB Specification - Chapter 7 (version 2.0).
3. No external termination series resistors are required on USB\_DP (D+) and USB\_DM (D-), the matching impedance is already included in the embedded driver.

**CAN (controller area network) interface**

Refer to [Section 6.3.15: I/O port characteristics](#) for more details on the input/output alternate function characteristics (CAN\_TX and CAN\_RX).

**6.3.19 ADC characteristics**

Unless otherwise specified, the parameters given in [Table 79](#) to [Table 82](#) are guaranteed by design, with conditions summarized in [Table 19](#).

**Table 79. ADC characteristics**

| Symbol    | Parameter  | Conditions                  | Min | Typ   | Max   | Unit    |
|-----------|--|-----------------------------|-----|-------|-------|---------|
| $V_{DDA}$ | Analog supply voltage for ADC                        | -                           | 2.0 | -     | 3.6   | V       |
| $I_{DDA}$ | Current on VDDA pin (see <a href="#">Figure 48</a> ) | Single-ended mode, 5 MSPS   | -   | 907   | 1033  | $\mu A$ |
|           |  | Single-ended mode, 1 MSPS   | -   | 194   | 285.5 |         |
|           |  | Single-ended mode, 200 KSPS | -   | 51.5  | 70    |         |
|           |  | Differential mode, 5 MSPS   | -   | 887.5 | 1009  |         |
|           |  | Differential mode, 1 MSPS   | -   | 212   | 285   |         |
|           |  | Differential mode, 200 KSPS | -   | 51    | 69.5  |         |

Table 79. ADC characteristics (continued)

| Symbol                              | Parameter  | Conditions  | Min    | Typ  | Max               | Unit               |
|-------------------------------------|--|---|--------|------|-------------------|--------------------|
| I <sub>REF</sub>                    | Current on VREF+ pin<br>(see <a href="#">Figure 49</a> )                                   | Single-ended mode,<br>5 MSPS                      | -      | 104  | 139               | μA                 |
|                                     |  | Single-ended mode,<br>1 MSPS                      | -      | 20.4 | 37                |                    |
|                                     |  | Single-ended mode,<br>200 KSPS                    | -      | 3.3  | 11.3              |                    |
|                                     |  | Differential mode,<br>5 MSPS                      | -      | 174  | 235               |                    |
|                                     |  | Differential mode,<br>1 MSPS                      | -      | 34.6 | 52.6              |                    |
|                                     |  | Differential mode,<br>200 KSPS                    | -      | 6    | 13.6              |                    |
| V <sub>REF+</sub>                   | Positive reference voltage   | -   | 2      | -    | V <sub>DDA</sub>  | V                  |
| f <sub>ADC</sub>                    | ADC clock frequency  | -   | 0.14   | -    | 72                | MHz                |
| f <sub>S</sub> <sup>(1)</sup>       | Sampling rate  | Resolution = 12 bits,<br>Fast Channel             | 0.01   | -    | 5.14              | MSPS               |
|                                     |  | Resolution = 10 bits,<br>Fast Channel             | 0.012  | -    | 6                 |                    |
|                                     |  | Resolution = 8 bits,<br>Fast Channel              | 0.014  | -    | 7.2               |                    |
|                                     |  | Resolution = 6 bits,<br>Fast Channel              | 0.0175 | -    | 9                 |                    |
| f <sub>TRIG</sub> <sup>(1)</sup>    | External trigger frequency   | f <sub>ADC</sub> = 72 MHz<br>Resolution = 12 bits | -      | -    | 5.14              | MHz                |
|                                     |  | Resolution = 12 bits                              | -      | -    | 14                | 1/f <sub>ADC</sub> |
| V <sub>AIN</sub>                    | Conversion voltage range <sup>(2)</sup>  | -   | 0      | -    | V <sub>REF+</sub> | V                  |
| R <sub>AIN</sub> <sup>(1)</sup>     | External input impedance   | -   | -      | -    | 100               | kΩ                 |
| C <sub>ADC</sub> <sup>(1)</sup>     | Internal sample and hold capacitor   | -   | -      | 5    | -                 | pF                 |
| t <sub>STAB</sub> <sup>(1)</sup>    | Power-up time  | -   | 0      | 0    | 1                 | μs                 |
| t <sub>CAL</sub> <sup>(1)</sup>     | Calibration time   | f <sub>ADC</sub> = 72 MHz                         | 1.56   |      |                   | μs                 |
|                                     |  | -   | 112    |      |                   | 1/f <sub>ADC</sub> |
| t <sub>latr</sub> <sup>(1)</sup>    | Trigger conversion latency<br>Regular and injected<br>channels without conversion<br>abort | CKMODE = 00                                       | 1.5    | 2    | 2.5               | 1/f <sub>ADC</sub> |
|                                     |  | CKMODE = 01                                       | -      | -    | 2                 | 1/f <sub>ADC</sub> |
|                                     |  | CKMODE = 10                                       | -      | -    | 2.25              | 1/f <sub>ADC</sub> |
|                                     |  | CKMODE = 11                                       | -      | -    | 2.125             | 1/f <sub>ADC</sub> |
| t <sub>latrinj</sub> <sup>(1)</sup> | Trigger conversion latency<br>Injected channels aborting a<br>regular conversion           | CKMODE = 00                                       | 2.5    | 3    | 3.5               | 1/f <sub>ADC</sub> |
|                                     |  | CKMODE = 01                                       | -      | -    | 3                 | 1/f <sub>ADC</sub> |
|                                     |  | CKMODE = 10                                       | -      | -    | 3.25              | 1/f <sub>ADC</sub> |
|                                     |  | CKMODE = 11                                       | -      | -    | 3.125             | 1/f <sub>ADC</sub> |



Table 79. ADC characteristics (continued)

| Symbol                    | Parameter                                       | Conditions   | Min   | Typ                      | Max                             | Unit          |
|---------------------------|---|--|---|--------------------------|---------------------------------|---------------|
| $t_S^{(1)}$               | Sampling time                                   | $f_{ADC} = 72 \text{ MHz}$                         | 0.021   | -                        | 8.35                            | $\mu\text{s}$ |
|                           |   | -  | 1.5   | -                        | 601.5                           | $1/f_{ADC}$   |
| $T_{ADCVREG\_STUP}^{(1)}$ | ADC Voltage Regulator Start-up time             | -  | -   | -                        | 10                              | $\mu\text{s}$ |
| $t_{CONV}^{(1)}$          | Total conversion time (including sampling time) | $f_{ADC} = 72 \text{ MHz}$<br>Resolution = 12 bits | 0.19  | -                        | 8.52                            | $\mu\text{s}$ |
|                           |   | Resolution = 12 bits                               | 14 to 614 ( $t_S$ for sampling + 12.5 for successive approximation) |                          |                                 | $1/f_{ADC}$   |
| CMIR                      | Common Mode Input signal range                  | ADC differential mode                              | $(V_{SSA} + V_{REF+})/2 - 0.18$                                     | $(V_{SSA} + V_{REF+})/2$ | $(V_{SSA} + V_{REF+})/2 + 0.18$ | V             |

1. Data guaranteed by design, not tested in Production.
2.  $V_{REF+}$  can be internally connected to  $V_{DDA}$  and  $V_{REF-}$  can be internally connected to  $V_{SSA}$ , depending on the package. Refer to [Section 4: Pinout and pin description](#) for further details.

Figure 48. ADC typical current consumption on VDDA pin

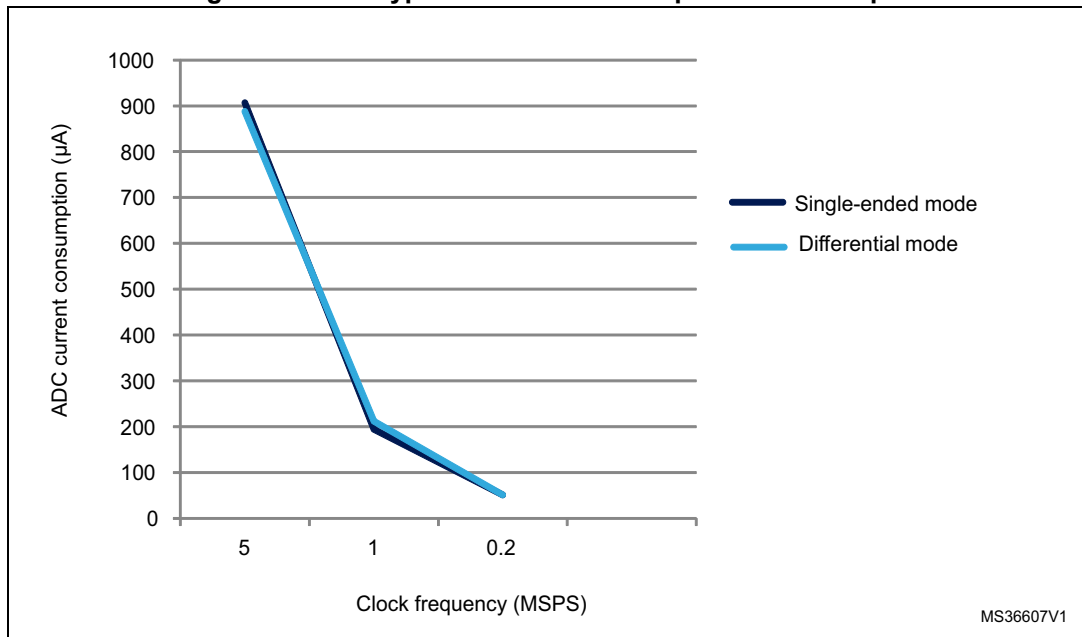
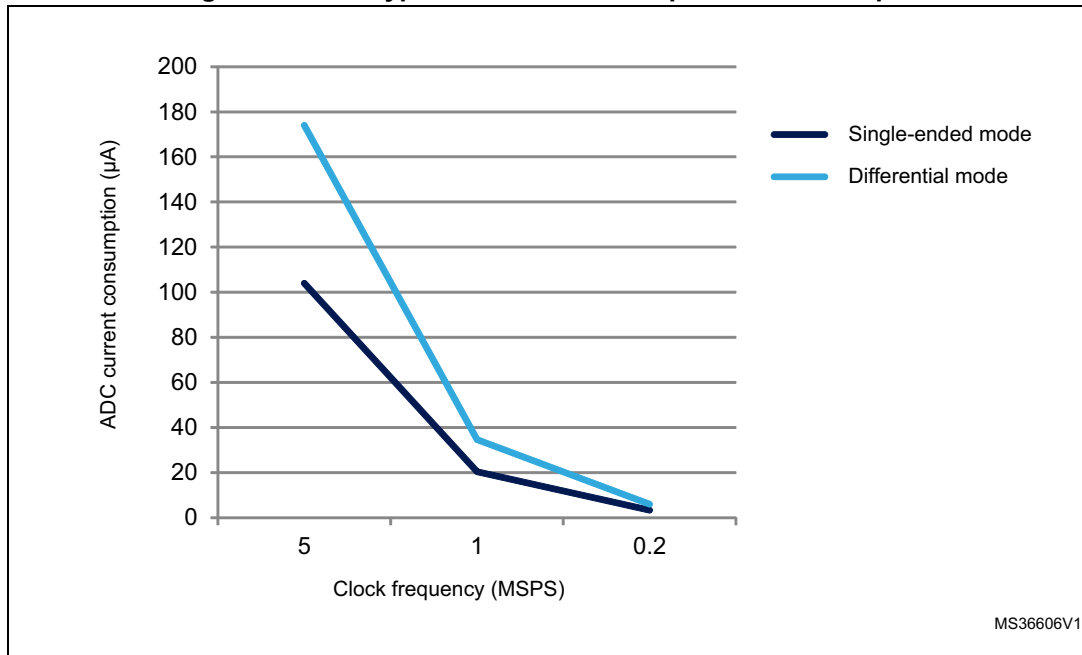


Figure 49. ADC typical current consumption on VREF+ pin



MS36606V1

Table 80. Maximum ADC  $R_{AIN}$  <sup>(1)</sup>

| Resolution | Sampling cycle @ 72 MHz | Sampling time [ns] @ 72 MHz | $R_{AIN}$ max (kΩ)           |               |                               |
|------------|-------------------------|-----------------------------|------------------------------|---------------|-------------------------------|
|            |                         |                             | Fast channels <sup>(2)</sup> | Slow channels | Other channels <sup>(3)</sup> |
| 12 bits    | 1.5                     | 20.83                       | 0.018                        | NA            | NA                            |
|            | 2.5                     | 34.72                       | 0.150                        | NA            | 0.022                         |
|            | 4.5                     | 62.50                       | 0.470                        | 0.220         | 0.180                         |
|            | 7.5                     | 104.17                      | 0.820                        | 0.560         | 0.470                         |
|            | 19.5                    | 270.83                      | 2.70                         | 1.80          | 1.50                          |
|            | 61.5                    | 854.17                      | 8.20                         | 6.80          | 4.70                          |
|            | 181.5                   | 2520.83                     | 22.0                         | 18.0          | 15.0                          |
|            | 601.5                   | 8354.17                     | 82.0                         | 68.0          | 47.0                          |
| 10 bits    | 1.5                     | 20.83                       | 0.082                        | NA            | NA                            |
|            | 2.5                     | 34.72                       | 0.270                        | 0.082         | 0.100                         |
|            | 4.5                     | 62.50                       | 0.560                        | 0.390         | 0.330                         |
|            | 7.5                     | 104.17                      | 1.20                         | 0.82          | 0.68                          |
|            | 19.5                    | 270.83                      | 3.30                         | 2.70          | 2.20                          |
|            | 61.5                    | 854.17                      | 10.0                         | 8.2           | 6.8                           |
|            | 181.5                   | 2520.83                     | 33.0                         | 27.0          | 22.0                          |
|            | 601.5                   | 8354.17                     | 100.0                        | 82.0          | 68.0                          |

Table 80. Maximum ADC  $R_{AIN}^{(1)}$  (continued)

| Resolution | Sampling cycle @ 72 MHz | Sampling time [ns] @ 72 MHz | $R_{AIN} \text{ max (k}\Omega\text{)}$ |               |                               |
|------------|-------------------------|-----------------------------|--|---------------|-------------------------------|
|            |                         |                             | Fast channels <sup>(2)</sup>           | Slow channels | Other channels <sup>(3)</sup> |
| 8 bits     | 1.5                     | 20.83                       | 0.150                                  | NA            | 0.039                         |
|            | 2.5                     | 34.72                       | 0.390                                  | 0.180         | 0.180                         |
|            | 4.5                     | 62.50                       | 0.820                                  | 0.560         | 0.470                         |
|            | 7.5                     | 104.17                      | 1.50                                   | 1.20          | 1.00                          |
|            | 19.5                    | 270.83                      | 3.90                                   | 3.30          | 2.70                          |
|            | 61.5                    | 854.17                      | 12.00                                  | 12.00         | 8.20                          |
|            | 181.5                   | 2520.83                     | 39.00                                  | 33.00         | 27.00                         |
|            | 601.5                   | 8354.17                     | 100.00                                 | 100.00        | 82.00                         |
| 6 bits     | 1.5                     | 20.83                       | 0.270                                  | 0.100         | 0.150                         |
|            | 2.5                     | 34.72                       | 0.560                                  | 0.390         | 0.330                         |
|            | 4.5                     | 62.50                       | 1.200                                  | 0.820         | 0.820                         |
|            | 7.5                     | 104.17                      | 2.20                                   | 1.80          | 1.50                          |
|            | 19.5                    | 270.83                      | 5.60                                   | 4.70          | 3.90                          |
|            | 61.5                    | 854.17                      | 18.0                                   | 15.0          | 12.0                          |
|            | 181.5                   | 2520.83                     | 56.0                                   | 47.0          | 39.0                          |
|            | 601.5                   | 8354.17                     | 100.00                                 | 100.0         | 100.0                         |

1. Data based on characterization results, not tested in production.
2. All fast channels, except channels on PA2, PA6.
3. Fast channels available on PA2, PA6.

Table 81. ADC accuracy - limited test conditions, 100-/144-pin packages <sup>(1)(2)</sup>

| Symbol               | Parameter                            | Conditions   |              | Min<br>(3)          | Typ  | Max<br>(3) | Unit |      |
|----------------------|--------------------------------------|--|--------------|---------------------|------|------------|------|------|
| ET                   | Total unadjusted error               |  | Single ended | Fast channel 5.1 Ms | -    | ±3.5       | ±4.5 | LSB  |
|                      |                                      |  |              | Slow channel 4.8 Ms | -    | ±4         | ±4.5 |      |
|                      |                                      |  | Differential | Fast channel 5.1 Ms | -    | ±3         | ±3   |      |
|                      |                                      |  |              | Slow channel 4.8 Ms | -    | ±3         | ±3   |      |
| EO                   | Offset error                         |  | Single ended | Fast channel 5.1 Ms | -    | ±1         | ±1.5 |      |
|                      |                                      |  |              | Slow channel 4.8 Ms | -    | ±1         | ±2.5 |      |
|                      |                                      |  | Differential | Fast channel 5.1 Ms | -    | ±1         | ±1.5 |      |
|                      |                                      |  |              | Slow channel 4.8 Ms | -    | ±1         | ±1.5 |      |
| EG                   | Gain error                           |  | Single ended | Fast channel 5.1 Ms | -    | ±3         | ±4   |      |
|                      |                                      |  |              | Slow channel 4.8 Ms | -    | ±3.5       | ±4   |      |
|                      |                                      |  | Differential | Fast channel 5.1 Ms | -    | ±1.5       | ±2.5 |      |
|                      |                                      |  |              | Slow channel 4.8 Ms | -    | ±2         | ±2.5 |      |
| ED                   | Differential linearity error         | ADC clock freq. ≤ 72 MHz<br>Sampling freq. ≤ 5 Msps<br>V <sub>DDA</sub> = V <sub>REF+</sub> = 3.3 V<br>25°C<br>100-pin/144-pin package | Single ended | Fast channel 5.1 Ms | -    | ±1         | ±1.5 |      |
|                      |                                      |  |              | Slow channel 4.8 Ms | -    | ±1         | ±1.5 |      |
|                      |                                      |  | Differential | Fast channel 5.1 Ms | -    | ±1         | ±1   |      |
|                      |                                      |  |              | Slow channel 4.8 Ms | -    | ±1         | ±1   |      |
| EL                   | Integral linearity error             |  | Single ended | Fast channel 5.1 Ms | -    | ±1.5       | ±2   |      |
|                      |                                      |  |              | Slow channel 4.8 Ms | -    | ±1.5       | ±3   |      |
|                      |                                      |  | Differential | Fast channel 5.1 Ms | -    | ±1         | ±1.5 |      |
|                      |                                      |  |              | Slow channel 4.8 Ms | -    | ±1         | ±1.5 |      |
| ENOB <sup>(4)</sup>  | Effective number of bits             |  | Single ended | Fast channel 5.1 Ms | 10.7 | 10.8       | -    | bits |
|                      |                                      |  |              | Slow channel 4.8 Ms | 10.7 | 10.8       | -    |      |
|                      |                                      |  | Differential | Fast channel 5.1 Ms | 11.2 | 11.3       | -    |      |
|                      |                                      |  |              | Slow channel 4.8 Ms | 11.1 | 11.3       | -    |      |
| SINAD <sup>(4)</sup> | Signal-to-noise and distortion ratio |  | Single ended | Fast channel 5.1 Ms | 66   | 67         | -    | dB   |
|                      |                                      |  |              | Slow channel 4.8 Ms | 66   | 67         | -    |      |
|                      |                                      |  | Differential | Fast channel 5.1 Ms | 69   | 70         | -    |      |
|                      |                                      |  |              | Slow channel 4.8 Ms | 69   | 70         | -    |      |

**Table 81. ADC accuracy - limited test conditions, 100-/144-pin packages <sup>(1)(2)</sup> (continued)**

| Symbol             | Parameter                 | Conditions   |              | Min <sup>(3)</sup>  | Typ | Max <sup>(3)</sup> | Unit |    |
|--------------------|---------------------------|--|--------------|---------------------|-----|--------------------|------|----|
| SNR <sup>(4)</sup> | Signal-to-noise ratio     | ADC clock freq. ≤ 72 MHz<br>Sampling freq ≤ 5 Msps<br>$V_{DDA} = V_{REF+} = 3.3\text{ V}$<br>25°C<br>100-pin/144-pin package | Single ended | Fast channel 5.1 Ms | 66  | 67                 | -    | dB |
|                    |                           |  |              | Slow channel 4.8 Ms | 66  | 67                 | -    |    |
|                    |                           |  | Differential | Fast channel 5.1 Ms | 69  | 70                 | -    |    |
|                    |                           |  |              | Slow channel 4.8 Ms | 69  | 70                 | -    |    |
| THD <sup>(4)</sup> | Total harmonic distortion |  | Single ended | Fast channel 5.1 Ms | -   | -76                | -76  |    |
|                    |                           |  |              | Slow channel 4.8 Ms | -   | -76                | -76  |    |
|                    |                           |  | Differential | Fast channel 5.1 Ms | -   | -80                | -80  |    |
|                    |                           |  |              | Slow channel 4.8 Ms | -   | -80                | -80  |    |

1. ADC DC accuracy values are measured after internal calibration.
2. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current. Any positive injection current within the limits specified for  $I_{INJ(PIN)}$  and  $\Sigma I_{INJ(PIN)}$  in [Section 6.3.15](#) does not affect the ADC accuracy.
3. Data based on characterization results, not tested in production.
4. Value measured with a -0.5 dB full scale 50 kHz sine wave input signal.

**Table 82. ADC accuracy, 100-pin/144-pin packages <sup>(1)(2)(3)</sup>**

| Symbol | Parameter                    | Conditions   |                     | Min <sup>(4)</sup>  | Max <sup>(4)</sup> | Unit |     |
|--------|------------------------------|--|---------------------|---------------------|--------------------|------|-----|
| ET     | Total unadjusted error       | ADC clock freq. ≤ 72 MHz,<br>Sampling freq. ≤ 5 Msps<br>$2.0\text{ V} \leq V_{DDA}, V_{REF+} \leq 3.6\text{ V}$<br>100-pin/144-pin package | Single Ended        | Fast channel 5.1 Ms | -                  | ±6.5 | LSB |
|        |                              |  |                     | Slow channel 4.8 Ms | -                  | ±6.5 |     |
|        |                              |  | Differential        | Fast channel 5.1 Ms | -                  | ±4   |     |
|        |                              |  |                     | Slow channel 4.8 Ms | -                  | ±4   |     |
| EO     | Offset error                 |  | Single Ended        | Fast channel 5.1 Ms | -                  | ±3   |     |
|        |                              |  |                     | Slow channel 4.8 Ms | -                  | ±3   |     |
|        |                              |  | Differential        | Fast channel 5.1 Ms | -                  | ±2   |     |
|        |                              |  |                     | Slow channel 4.8 Ms | -                  | ±2   |     |
| EG     | Gain error                   | Single Ended   | Fast channel 5.1 Ms | -                   | ±6                 |      |     |
|        |                              |  | Slow channel 4.8 Ms | -                   | ±6                 |      |     |
|        |                              | Differential   | Fast channel 5.1 Ms | -                   | ±3                 |      |     |
|        |                              |  | Slow channel 4.8 Ms | -                   | ±3                 |      |     |
| ED     | Differential linearity error | Single Ended   | Fast channel 5.1 Ms | -                   | ±1.5               |      |     |
|        |                              |  | Slow channel 4.8 Ms | -                   | ±1.5               |      |     |
|        |                              | Differential   | Fast channel 5.1 Ms | -                   | ±1.5               |      |     |
|        |                              |  | Slow channel 4.8 Ms | -                   | ±1.5               |      |     |

Table 82. ADC accuracy, 100-pin/144-pin packages<sup>(1)(2)(3)</sup> (continued)

| Symbol               | Parameter                            | Conditions   |                     | Min <sup>(4)</sup>  | Max <sup>(4)</sup> | Unit |      |
|----------------------|--------------------------------------|--|---------------------|---------------------|--------------------|------|------|
| EL                   | Integral linearity error             | ADC clock freq. ≤ 72 MHz,<br>Sampling freq. ≤ 5 Msps,<br>2.0 V ≤ V <sub>DDA</sub> , V <sub>REF+</sub> ≤ 3.6 V<br>100-pin/144-pin package | Single Ended        | Fast channel 5.1 Ms | -                  | ±2   | LSB  |
|                      |                                      |  |                     | Slow channel 4.8 Ms | -                  | ±3   |      |
|                      |                                      |  | Differential        | Fast channel 5.1 Ms | -                  | ±2   |      |
|                      |                                      |  |                     | Slow channel 4.8 Ms | -                  | ±2   |      |
| ENOB <sup>(5)</sup>  | Effective number of bits             |  | Single Ended        | Fast channel 5.1 Ms | 10.4               | -    | bits |
|                      |                                      |  |                     | Slow channel 4.8 Ms | 10.2               | -    |      |
|                      |                                      |  | Differential        | Fast channel 5.1 Ms | 10.8               | -    |      |
|                      |                                      |  |                     | Slow channel 4.8 Ms | 10.8               | -    |      |
| SINAD <sup>(5)</sup> | Signal-to-noise and distortion ratio | Single Ended   | Fast channel 5.1 Ms | 64                  | -                  | dB   |      |
|                      |                                      |  | Slow channel 4.8 Ms | 63                  | -                  |      |      |
|                      |                                      | Differential   | Fast channel 5.1 Ms | 67                  | -                  |      |      |
|                      |                                      |  | Slow channel 4.8 Ms | 67                  | -                  |      |      |
| SNR <sup>(5)</sup>   | Signal-to-noise ratio                | Single Ended   | Fast channel 5.1 Ms | 64                  | -                  |      |      |
|                      |                                      |  | Slow channel 4.8 Ms | 64                  | -                  |      |      |
|                      |                                      | Differential   | Fast channel 5.1 Ms | 67                  | -                  |      |      |
|                      |                                      |  | Slow channel 4.8 Ms | 67                  | -                  |      |      |
| THD <sup>(5)</sup>   | Total harmonic distortion            | Single Ended   | Fast channel 5.1 Ms | -                   | 74                 |      |      |
|                      |                                      |  | Slow channel 4.8 Ms | -                   | -74                |      |      |
|                      |                                      | Differential   | Fast channel 5.1 Ms | -                   | -78                |      |      |
|                      |                                      |  | Slow channel 4.8 Ms | -                   | -76                |      |      |

1. ADC DC accuracy values are measured after internal calibration.
2. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current. Any positive injection current within the limits specified for I<sub>INJ(PIN)</sub> and ΣI<sub>INJ(PIN)</sub> in [Section 6.3.15](#) does not affect the ADC accuracy.
3. Better performance may be achieved in restricted V<sub>DDA</sub>, frequency and temperature ranges.
4. Data based on characterization results, not tested in production.
5. Value measured with a -0.5 dB full scale 50 kHz sine wave input signal.

Table 83. ADC accuracy - limited test conditions, 64-pin packages<sup>(1)(2)</sup>

| Symbol               | Parameter                            | Conditions  |              |                     | Min<br>(3) | Typ  | Max<br>(3) | Unit |
|----------------------|--------------------------------------|---|--------------|---------------------|------------|------|------------|------|
| ET                   | Total unadjusted error               | ADC clock freq. ≤ 72 MHz<br>Sampling freq. ≤ 5 Msps<br>V <sub>DDA</sub> = 3.3 V<br>25°C<br>64-pin package | Single ended | Fast channel 5.1 Ms | -          | ±4   | ±4.5       | LSB  |
|                      |                                      |   |              | Slow channel 4.8 Ms | -          | ±5.5 | ±6         |      |
|                      |                                      |   | Differential | Fast channel 5.1 Ms | -          | ±3.5 | ±4         |      |
|                      |                                      |   |              | Slow channel 4.8 Ms | -          | ±3.5 | ±4         |      |
| EO                   | Offset error                         | ADC clock freq. ≤ 72 MHz<br>Sampling freq. ≤ 5 Msps<br>V <sub>DDA</sub> = 3.3 V<br>25°C<br>64-pin package | Single ended | Fast channel 5.1 Ms | -          | ±2   | ±2         |      |
|                      |                                      |   |              | Slow channel 4.8 Ms | -          | ±1.5 | ±2         |      |
|                      |                                      |   | Differential | Fast channel 5.1 Ms | -          | ±1.5 | ±2         |      |
|                      |                                      |   |              | Slow channel 4.8 Ms | -          | ±1.5 | ±2         |      |
| EG                   | Gain error                           | ADC clock freq. ≤ 72 MHz<br>Sampling freq. ≤ 5 Msps<br>V <sub>DDA</sub> = 3.3 V<br>25°C<br>64-pin package | Single ended | Fast channel 5.1 Ms | -          | ±3   | ±4         |      |
|                      |                                      |   |              | Slow channel 4.8 Ms | -          | ±5   | ±5.5       |      |
|                      |                                      |   | Differential | Fast channel 5.1 Ms | -          | ±3   | ±3         |      |
|                      |                                      |   |              | Slow channel 4.8 Ms | -          | ±3   | ±3.5       |      |
| ED                   | Differential linearity error         | ADC clock freq. ≤ 72 MHz<br>Sampling freq. ≤ 5 Msps<br>V <sub>DDA</sub> = 3.3 V<br>25°C<br>64-pin package | Single ended | Fast channel 5.1 Ms | -          | ±1   | ±1         |      |
|                      |                                      |   |              | Slow channel 4.8 Ms | -          | ±1   | ±1         |      |
|                      |                                      |   | Differential | Fast channel 5.1 Ms | -          | ±1   | ±1         |      |
|                      |                                      |   |              | Slow channel 4.8 Ms | -          | ±1   | ±1         |      |
| EL                   | Integral linearity error             | ADC clock freq. ≤ 72 MHz<br>Sampling freq. ≤ 5 Msps<br>V <sub>DDA</sub> = 3.3 V<br>25°C<br>64-pin package | Single ended | Fast channel 5.1 Ms | -          | ±1.5 | ±2         |      |
|                      |                                      |   |              | Slow channel 4.8 Ms | -          | ±2   | ±3         |      |
|                      |                                      |   | Differential | Fast channel 5.1 Ms | -          | ±1.5 | ±1.5       |      |
|                      |                                      |   |              | Slow channel 4.8 Ms | -          | ±1.5 | ±2         |      |
| ENOB <sup>(4)</sup>  | Effective number of bits             | ADC clock freq. ≤ 72 MHz<br>Sampling freq. ≤ 5 Msps<br>V <sub>DDA</sub> = 3.3 V<br>25°C<br>64-pin package | Single ended | Fast channel 5.1 Ms | 10.8       | 10.8 | -          | bit  |
|                      |                                      |   |              | Slow channel 4.8 Ms | 10.8       | 10.8 | -          |      |
|                      |                                      |   | Differential | Fast channel 5.1 Ms | 11.2       | 11.3 | -          |      |
|                      |                                      |   |              | Slow channel 4.8 Ms | 11.2       | 11.3 | -          |      |
| SINAD <sup>(4)</sup> | Signal-to-noise and distortion ratio | ADC clock freq. ≤ 72 MHz<br>Sampling freq. ≤ 5 Msps<br>V <sub>DDA</sub> = 3.3 V<br>25°C<br>64-pin package | Single ended | Fast channel 5.1 Ms | 66         | 67   | -          | dB   |
|                      |                                      |   |              | Slow channel 4.8 Ms | 66         | 67   | -          |      |
|                      |                                      |   | Differential | Fast channel 5.1 Ms | 69         | 70   | -          |      |
|                      |                                      |   |              | Slow channel 4.8 Ms | 69         | 70   | -          |      |

**Table 83. ADC accuracy - limited test conditions, 64-pin packages<sup>(1)(2)</sup> (continued)**

| Symbol             | Parameter                 | Conditions   |              |                     | Min <sup>(3)</sup> | Typ | Max <sup>(3)</sup> | Unit |
|--------------------|---------------------------|--|--------------|---------------------|--------------------|-----|--------------------|------|
| SNR <sup>(4)</sup> | Signal-to-noise ratio     | ADC clock freq. ≤ 72 MHz<br>Sampling freq ≤ 5 Msps<br>V <sub>DDA</sub> = 3.3 V<br>25°C<br>64-pin package | Single ended | Fast channel 5.1 Ms | 66                 | 67  | -                  | dB   |
|                    |                           |  |              | Slow channel 4.8 Ms | 66                 | 67  | -                  |      |
|                    |                           |  | Differential | Fast channel 5.1 Ms | 69                 | 70  | -                  |      |
|                    |                           |  |              | Slow channel 4.8 Ms | 69                 | 70  | -                  |      |
| THD <sup>(4)</sup> | Total harmonic distortion |  | Single ended | Fast channel 5.1 Ms | -                  | -80 | -80                |      |
|                    |                           |  |              | Slow channel 4.8 Ms | -                  | -78 | -77                |      |
|                    |                           |  | Differential | Fast channel 5.1 Ms | -                  | -83 | -82                |      |
|                    |                           |  |              | Slow channel 4.8 Ms | -                  | -81 | -80                |      |

1. ADC DC accuracy values are measured after internal calibration.
2. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current. Any positive injection current within the limits specified for I<sub>INJ(PIN)</sub> and ΣI<sub>INJ(PIN)</sub> in [Section 6.3.15](#) does not affect the ADC accuracy.
3. Data based on characterization results, not tested in production.
4. Value measured with a -0.5 dB full scale 50 kHz sine wave input signal.

**Table 84. ADC accuracy, 64-pin packages<sup>(1)(2)(3)</sup>**

| Symbol | Parameter                    | Conditions   |                     |                     | Min <sup>(4)</sup> | Max <sup>(4)</sup> | Unit |
|--------|------------------------------|--|---------------------|---------------------|--------------------|--------------------|------|
| ET     | Total unadjusted error       | ADC clock freq. ≤ 72 MHz,<br>Sampling freq. ≤ 5 Msps<br>2.0 V ≤ V <sub>DDA</sub> ≤ 3.6 V<br>64-pin package | Single ended        | Fast channel 5.1 Ms | -                  | ±6.5               | LSB  |
|        |                              |  |                     | Slow channel 4.8 Ms | -                  | ±6.5               |      |
|        |                              |  | Differential        | Fast channel 5.1 Ms | -                  | ±4                 |      |
|        |                              |  |                     | Slow channel 4.8 Ms | -                  | ±4.5               |      |
| EO     | Offset error                 |  | Single ended        | Fast channel 5.1 Ms | -                  | ±3                 |      |
|        |                              |  |                     | Slow channel 4.8 Ms | -                  | ±3                 |      |
|        |                              |  | Differential        | Fast channel 5.1 Ms | -                  | ±2.5               |      |
|        |                              |  |                     | Slow channel 4.8 Ms | -                  | ±2.5               |      |
| EG     | Gain error                   | Single ended   | Fast channel 5.1 Ms | -                   | ±6                 |                    |      |
|        |                              |  | Slow channel 4.8 Ms | -                   | ±6                 |                    |      |
|        |                              | Differential   | Fast channel 5.1 Ms | -                   | ±3.5               |                    |      |
|        |                              |  | Slow channel 4.8 Ms | -                   | ±4                 |                    |      |
| ED     | Differential linearity error | Single ended   | Fast channel 5.1 Ms | -                   | ±1.5               |                    |      |
|        |                              |  | Slow channel 4.8 Ms | -                   | ±1.5               |                    |      |
|        |                              | Differential   | Fast channel 5.1 Ms | -                   | ±1.5               |                    |      |
|        |                              |  | Slow channel 4.8 Ms | -                   | ±1.5               |                    |      |



Table 84. ADC accuracy, 64-pin packages<sup>(1)(2)(3)</sup> (continued)

| Symbol               | Parameter                            | Conditions   |              | Min <sup>(4)</sup>  | Max <sup>(4)</sup> | Unit |      |
|----------------------|--------------------------------------|--|--------------|---------------------|--------------------|------|------|
| EL                   | Integral linearity error             | ADC clock freq. ≤ 72 MHz,<br>Sampling freq ≤ 5 Msps,<br>2.0 V ≤ V <sub>DDA</sub> ≤ 3.6 V<br>64-pin package | Single ended | Fast channel 5.1 Ms | -                  | ±3   | LSB  |
|                      |                                      |  |              | Slow channel 4.8 Ms | -                  | ±3.5 |      |
|                      |                                      |  | Differential | Fast channel 5.1 Ms | -                  | ±2   |      |
|                      |                                      |  |              | Slow channel 4.8 Ms | -                  | ±2.5 |      |
| ENOB <sup>(5)</sup>  | Effective number of bits             | ADC clock freq. ≤ 72 MHz,<br>Sampling freq ≤ 5 Msps,<br>2.0 V ≤ V <sub>DDA</sub> ≤ 3.6 V<br>64-pin package | Single ended | Fast channel 5.1 Ms | 10.4               | -    | bits |
|                      |                                      |  |              | Slow channel 4.8 Ms | 10.4               | -    |      |
|                      |                                      |  | Differential | Fast channel 5.1 Ms | 10.8               | -    |      |
|                      |                                      |  |              | Slow channel 4.8 Ms | 10.8               | -    |      |
| SINAD <sup>(5)</sup> | Signal-to-noise and distortion ratio | ADC clock freq. ≤ 72 MHz,<br>Sampling freq ≤ 5 Msps,<br>2.0 V ≤ V <sub>DDA</sub> ≤ 3.6 V<br>64-pin package | Single ended | Fast channel 5.1 Ms | 64                 | -    | dB   |
|                      |                                      |  |              | Slow channel 4.8 Ms | 63                 | -    |      |
|                      |                                      |  | Differential | Fast channel 5.1 Ms | 67                 | -    |      |
|                      |                                      |  |              | Slow channel 4.8 Ms | 67                 | -    |      |
| SNR <sup>(5)</sup>   | Signal-to-noise ratio                | ADC clock freq. ≤ 72 MHz,<br>Sampling freq ≤ 5 Msps,<br>2.0 V ≤ V <sub>DDA</sub> ≤ 3.6 V<br>64-pin package | Single ended | Fast channel 5.1 Ms | 64                 | -    | dB   |
|                      |                                      |  |              | Slow channel 4.8 Ms | 64                 | -    |      |
|                      |                                      |  | Differential | Fast channel 5.1 Ms | 67                 | -    |      |
|                      |                                      |  |              | Slow channel 4.8 Ms | 67                 | -    |      |
| THD <sup>(5)</sup>   | Total harmonic distortion            | ADC clock freq. ≤ 72 MHz,<br>Sampling freq ≤ 5 Msps,<br>2.0 V ≤ V <sub>DDA</sub> ≤ 3.6 V<br>64-pin package | Single ended | Fast channel 5.1 Ms | -                  | -75  | dB   |
|                      |                                      |  |              | Slow channel 4.8 Ms | -                  | -75  |      |
|                      |                                      |  | Differential | Fast channel 5.1 Ms | -                  | -79  |      |
|                      |                                      |  |              | Slow channel 4.8 Ms | -                  | -78  |      |

1. ADC DC accuracy values are measured after internal calibration.
2. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current. Any positive injection current within the limits specified for I<sub>INJ(PIN)</sub> and ΣI<sub>INJ(PIN)</sub> in [Section 6.3.15](#) does not affect the ADC accuracy.
3. Better performance may be achieved in restricted V<sub>DDA</sub>, frequency and temperature ranges.
4. Data based on characterization results, not tested in production.
5. Value measured with a -0.5 dB full scale 50 kHz sine wave input signal.

Table 85. ADC accuracy at 1MSPS<sup>(1)(2)</sup>

| Symbol | Parameter                    | Test conditions   | Typ          | Max <sup>(3)</sup> | Unit |     |
|--------|------------------------------|---|--------------|--------------------|------|-----|
| ET     | Total unadjusted error       | ADC Freq ≤ 72 MHz<br>Sampling Freq ≤ 1MSPS<br>2.4 V ≤ V <sub>DDA</sub> = V <sub>REF+</sub> ≤ 3.6 V<br>Single-ended mode | Fast channel | ±2.5               | ±5   | LSB |
|        |                              |   | Slow channel | ±3.5               | ±5   |     |
| EO     | Offset error                 |   | Fast channel | ±1                 | ±2.5 |     |
|        |                              |   | Slow channel | ±1.5               | ±2.5 |     |
| EG     | Gain error                   |   | Fast channel | ±2                 | ±3   |     |
|        |                              |   | Slow channel | ±3                 | ±4   |     |
| ED     | Differential linearity error |   | Fast channel | ±0.7               | ±2   |     |
|        |                              |   | Slow channel | ±0.7               | ±2   |     |
| EL     | Integral linearity error     | Fast channel  | ±1           | ±3                 |      |     |
|        |                              | Slow channel  | ±1.2         | ±3                 |      |     |

1. ADC DC accuracy values are measured after internal calibration.
2. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current. Any positive injection current within the limits specified for IINJ(PIN) and ΣIINJ(PIN) in [Section 6.3.15: I/O port characteristics](#) does not affect the ADC accuracy.
3. Data based on characterization results, not tested in production.

Figure 50. ADC accuracy characteristics

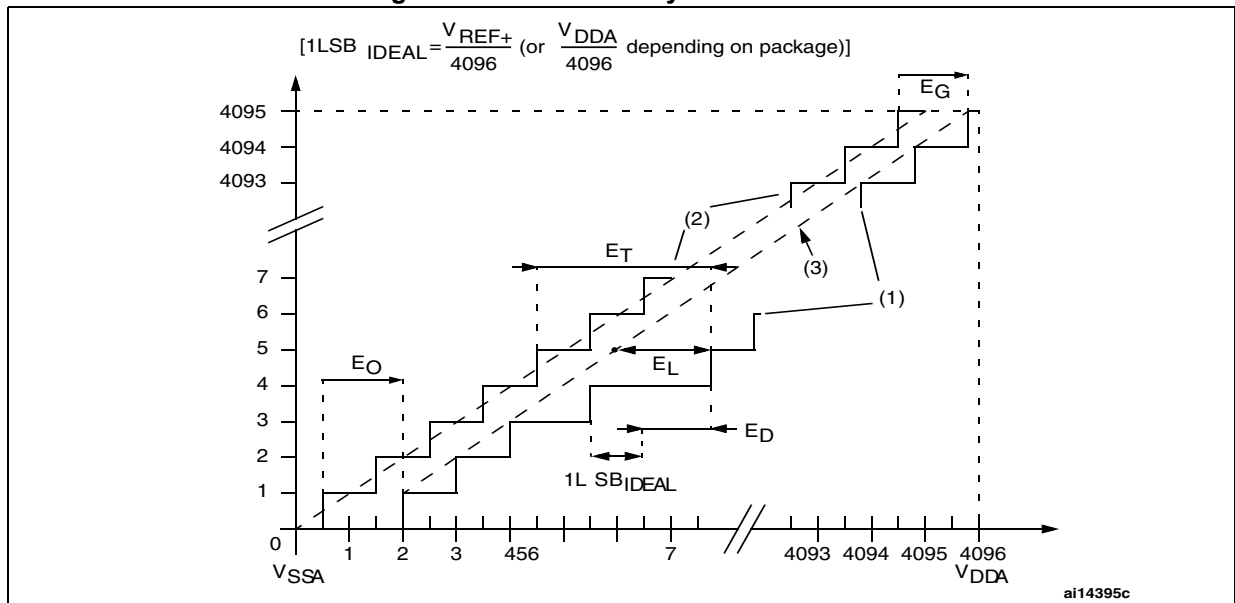
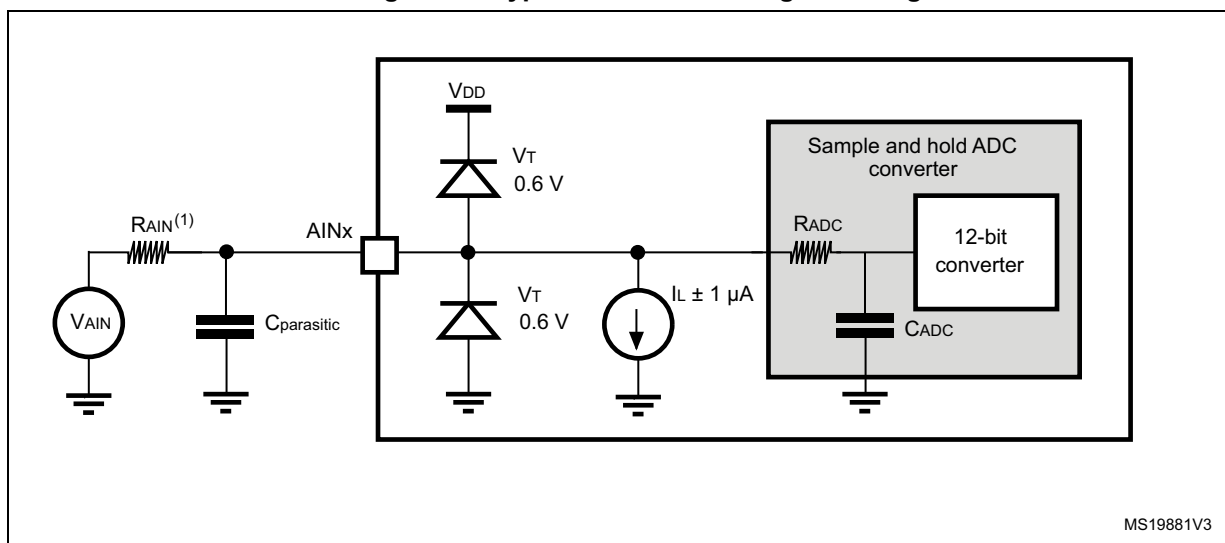


Figure 51. Typical connection diagram using the ADC



1. Refer to [Table 79](#) for the values of  $R_{AIN}$ .
2.  $C_{parasitic}$  represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high  $C_{parasitic}$  value downgrades conversion accuracy. To remedy this,  $f_{ADC}$  should be reduced.

### General PCB design guidelines

Power supply decoupling should be performed as shown in [Figure 12](#). The 10 nF capacitor should be ceramic (good quality) and it should be placed as close as possible to the chip.

## 6.3.20 DAC electrical specifications

Table 86. DAC characteristics

| Symbol               | Parameter                 | Conditions  | Min | Typ | Max              | Unit       |
|----------------------|---------------------------|---|-----|-----|------------------|------------|
| $V_{DDA}$            | Analog supply voltage     | -   | 2.4 | -   | 3.6              | V          |
| $R_{LOAD}^{(1)}$     | Resistive load            | DAC output buffer ON  | 5   | -   | -                | k $\Omega$ |
| $R_L$                | Resistive load            | Dac output buffer ON: connected to $V_{SSA}$  | 5   | -   | -                | k $\Omega$ |
|                      |                           | Dac output buffer ON: connected to $V_{DDA}$  | 25  | -   | -                | k $\Omega$ |
| $R_O^{(1)}$          | Output impedance          | DAC output buffer OFF   | -   | -   | 15               | k $\Omega$ |
| $C_{LOAD}^{(1)}$     | Capacitive load           | DAC output buffer ON  | -   | -   | 50               | pF         |
| $V_{DAC\_OUT}^{(1)}$ | Voltage on DAC_OUT output | Corresponds to 12-bit input code (0x0E0) to (0xF1C) at $V_{DDA} = 3.6$ V and (0x155) and (0xEAB) at $V_{DDA} = 2.4$ V DAC output buffer ON. | 0.2 | -   | $V_{DDA} - 0.2$  | V          |
|                      |                           | DAC output buffer OFF   | -   | 0.5 | $V_{DDA} - 1LSB$ | mV         |

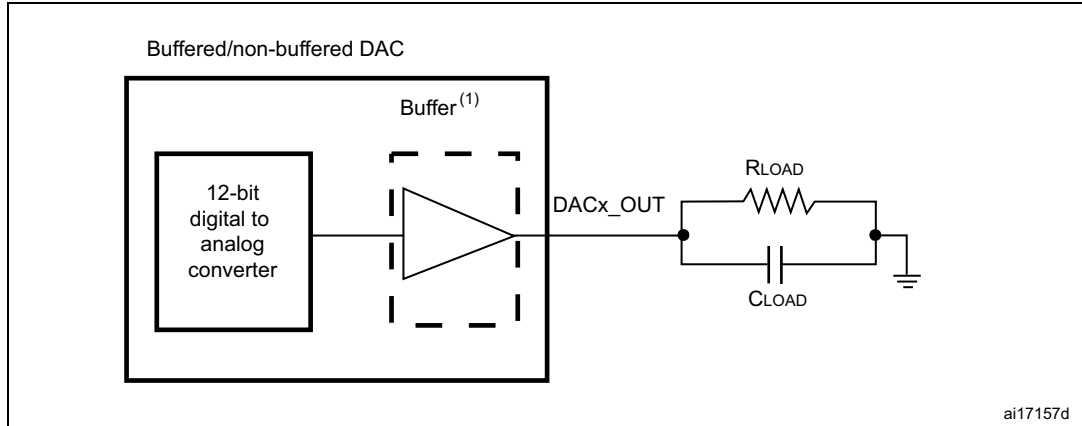
Table 86. DAC characteristics (continued)

| Symbol                     | Parameter   | Conditions   | Min | Typ | Max       | Unit             |
|----------------------------|---|--|-----|-----|-----------|------------------|
| $I_{REF}$                  | DAC DC current consumption in quiescent mode (Standby mode)   | With no load, worst code (0xF1C) on the input                        | -   | -   | 220       | $\mu\text{A}$    |
| $I_{DDA}^{(3)}$            | DAC DC current consumption in quiescent mode (Standby mode) <sup>(2)</sup>  | With no load, middle code (0x800) on the input.                      | -   | -   | 380       | $\mu\text{A}$    |
|                            |   | With no load, worst code (0xF1C) on the input.                       | -   | -   | 480       | $\mu\text{A}$    |
| $DNL^{(3)}$                | Differential non linearity<br>Difference between two consecutive code-1LSB)   | Given for a 10-bit input code  | -   | -   | $\pm 0.5$ | LSB              |
|                            |   | Given for a 12-bit input code  | -   | -   | $\pm 2$   | LSB              |
| $INL^{(3)}$                | Integral non linearity<br>(difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 4095)                 | Given for a 10-bit input code  | -   | -   | $\pm 1$   | LSB              |
|                            |   | Given for a 12-bit input code  | -   | -   | $\pm 4$   | LSB              |
| Offset <sup>(3)</sup>      | Offset error (difference between measured value at Code (0x800) and the ideal value = $V_{DDA}/2$ )   | -  | -   | -   | $\pm 10$  | mV               |
|                            |   | Given for a 10-bit input code at $V_{DDA} = 3.6\text{ V}$            | -   | -   | $\pm 3$   | LSB              |
|                            |   | Given for a 12-bit input code at $V_{DDA} = 3.6\text{ V}$            | -   | -   | $\pm 12$  | LSB              |
| Gain error <sup>(3)</sup>  | Gain error  | Given for a 12-bit input code  | -   | -   | $\pm 0.5$ | %                |
| $t_{SETTLING}^{(3)}$       | Settling time (full scale: for a 12-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value $\pm 1\text{LSB}$ ) | $C_{LOAD} \leq 50\text{ pF}$ ,<br>$R_{LOAD} \geq 5\text{ k}\Omega$   | -   | 3   | 4         | $\mu\text{s}$    |
| $t_{STAB}$                 | Power-up time   | -  | 1   |     |           | conversion cycle |
| Update rate <sup>(3)</sup> | Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB)   | $C_{LOAD} \leq 50\text{ pF}$ ,<br>$R_{LOAD} \geq 5\text{ k}\Omega$   | -   | -   | 1         | MS/s             |
| $t_{WAKEUP}^{(3)}$         | Wakeup time from off state (Setting the ENx bit in the DAC Control register)  | $C_{LOAD} \leq 50\text{ pF}$ ,<br>$R_{LOAD} \geq 5\text{ k}\Omega$   | -   | 6.5 | 10        | $\mu\text{s}$    |
| PSRR+ <sup>(1)</sup>       | Power supply rejection ratio (to $V_{DDA}$ ) (static DC measurement)  | $C_{LOAD} = 50\text{ pF}$ ,<br>No $R_{LOAD} \geq 5\text{ k}\Omega$ , | -   | -67 | -40       | dB               |
| $I_{skink}^{(1)}$          | Output sink current   | DAC buffer ON<br>Output level higher than 0.2 V                      | 100 | -   | -         | $\mu\text{A}$    |

1. Guaranteed by design, not tested in production.

2. Quiescent mode refers to the state of the DAC a keeping steady value on the output, so no dynamic consumption is involved.
3. Data based on characterization results, not tested in production.

**Figure 52. 12-bit buffered /non-buffered DAC**



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC\_CR register.

### 6.3.21 Comparator characteristics

**Table 87. Comparator characteristics<sup>(1)</sup>**

| Symbol       | Parameter   | Conditions                  | Min. | Typ.          | Max.      | Unit          |
|--------------|---|-----------------------------|------|---------------|-----------|---------------|
| $V_{DDA}$    | Analog supply voltage                                       | -                           | 2    | -             | 3.6       | V             |
| $V_{IN}$     | Comparator input voltage range                              | -                           | 0    | -             | $V_{DDA}$ |               |
| $V_{BG}$     | Scaler input voltage  | -                           | -    | $V_{REFINIT}$ | -         |               |
| $V_{SC}$     | Scaler offset voltage                                       | -                           | -    | $\pm 5$       | $\pm 10$  | mV            |
| $t_{S\_SC}$  | Scaler startup time from power down                         | -                           | -    | -             | 0.2       | ms            |
| $t_{START}$  | Comparator startup time                                     | $V_{DDA} \geq 2.7\text{ V}$ | -    | -             | 4         | $\mu\text{s}$ |
|              |   | $V_{DDA} < 2.7\text{ V}$    | -    | -             | 10        |               |
| $t_D$        | Propagation delay for 200 mV step with 100 mV overdrive     | $V_{DDA} \geq 2.7\text{ V}$ | -    | 25            | 28        | ns            |
|              |   | $V_{DDA} < 2.7\text{ V}$    | -    | 28            | 30        |               |
|              | Propagation delay for full range step with 100 mV overdrive | $V_{DDA} \geq 2.7\text{ V}$ | -    | 32            | 35        |               |
|              |   | $V_{DDA} < 2.7\text{ V}$    | -    | 35            | 40        |               |
| $V_{OFFSET}$ | Comparator offset error                                     | $V_{DDA} \geq 2.7\text{ V}$ | -    | $\pm 5$       | $\pm 10$  | mV            |
|              |   | $V_{DDA} < 2.7\text{ V}$    | -    | -             | $\pm 25$  |               |

Table 87. Comparator characteristics<sup>(1)</sup> (continued)

| Symbol               | Parameter                | Conditions             | Min. | Typ. | Max. | Unit          |
|----------------------|--------------------------|------------------------|------|------|------|---------------|
| $TV_{\text{OFFSET}}$ | Total offset variation   | Full temperature range | -    | -    | 3    | mV            |
| $I_{\text{DDA}}$     | COMP current consumption | -                      | -    | 400  | 600  | $\mu\text{A}$ |

1. Guaranteed by design, not tested in production.

## 6.3.22 Operational amplifier characteristics

Table 88. Operational amplifier characteristics<sup>(1)</sup>

| Symbol                      | Parameter   |                           | Condition  | Min                  | Typ | Max       | Unit                         |
|-----------------------------|---|---------------------------|--|----------------------|-----|-----------|------------------------------|
| $V_{DDA}$                   | Analog supply voltage   |                           | -  | 2.4                  | -   | 3.6       | V                            |
| CMIR                        | Common mode input range   |                           | -  | 0                    | -   | $V_{DDA}$ | V                            |
| $V_{I\text{OFFSET}}$        | Input offset voltage  | Maximum calibration range | 25°C, No Load on output.   | -                    | -   | 4         | mV                           |
|                             |   |                           | All voltage/Temp.  | -                    | -   | 6         |                              |
|                             |   | After offset calibration  | 25°C, No Load on output.   | -                    | -   | 1.6       |                              |
|                             |   |                           | All voltage/Temp.  | -                    | -   | 3         |                              |
| $\Delta V_{I\text{OFFSET}}$ | Input offset voltage drift  |                           | -  | -                    | 5   | -         | $\mu\text{V}/^\circ\text{C}$ |
| $I_{\text{LOAD}}$           | Drive current   |                           | -  | -                    | -   | 500       | $\mu\text{A}$                |
| $I_{\text{DDA}}$            | OPAMP consumption   |                           | No load, quiescent mode  | -                    | 690 | 1450      | $\mu\text{A}$                |
| TS_OPAMP_VOUT               | ADC sampling time when reading the OPAMP output.  |                           | -  | 400                  | -   | -         | ns                           |
| CMRR                        | Common mode rejection ratio   |                           | -  | -                    | 90  | -         | dB                           |
| PSRR                        | Power supply rejection ratio  |                           | DC   | 73                   | 117 | -         | dB                           |
| GBW                         | Bandwidth   |                           | -  | -                    | 8.2 | -         | MHz                          |
| SR                          | Slew rate   |                           | -  | -                    | 4.7 | -         | V/ $\mu\text{s}$             |
| $R_{\text{LOAD}}$           | Resistive load  |                           | -  | 4                    | -   | -         | k $\Omega$                   |
| $C_{\text{LOAD}}$           | Capacitive load   |                           | -  | -                    | -   | 50        | pF                           |
| $V_{\text{OH}\text{SAT}}$   | High saturation voltage <sup>(2)</sup>  |                           | $R_{\text{load}} = \text{min, Input at } V_{\text{DDA}}$ .   | $V_{\text{DDA}}-100$ | -   | -         | mV                           |
|                             |   |                           | $R_{\text{load}} = 20\text{K, Input at } V_{\text{DDA}}$ .   | $V_{\text{DDA}}-20$  | -   | -         |                              |
| $V_{\text{OL}\text{SAT}}$   | Low saturation voltage <sup>(2)</sup>   |                           | $R_{\text{load}} = \text{min, input at } 0\text{V}$  | -                    | -   | 100       | mV                           |
|                             |   |                           | $R_{\text{load}} = 20\text{K, input at } 0\text{V.}$   | -                    | -   | 20        |                              |
| $\phi\text{m}$              | Phase margin  |                           | -  | -                    | 62  | -         | °                            |
| $t_{\text{OFFTRIM}}$        | Offset trim time: during calibration, minimum time needed between two steps to have 1 mV accuracy |                           | -  | -                    | -   | 2         | ms                           |
| $t_{\text{WAKEUP}}$         | Wake up time from OFF state.  |                           | $C_{\text{LOAD}} \leq 50 \text{ pf, } R_{\text{LOAD}} \geq 4 \text{ k}\Omega$ , Follower configuration | -                    | 2.8 | 5         | $\mu\text{s}$                |

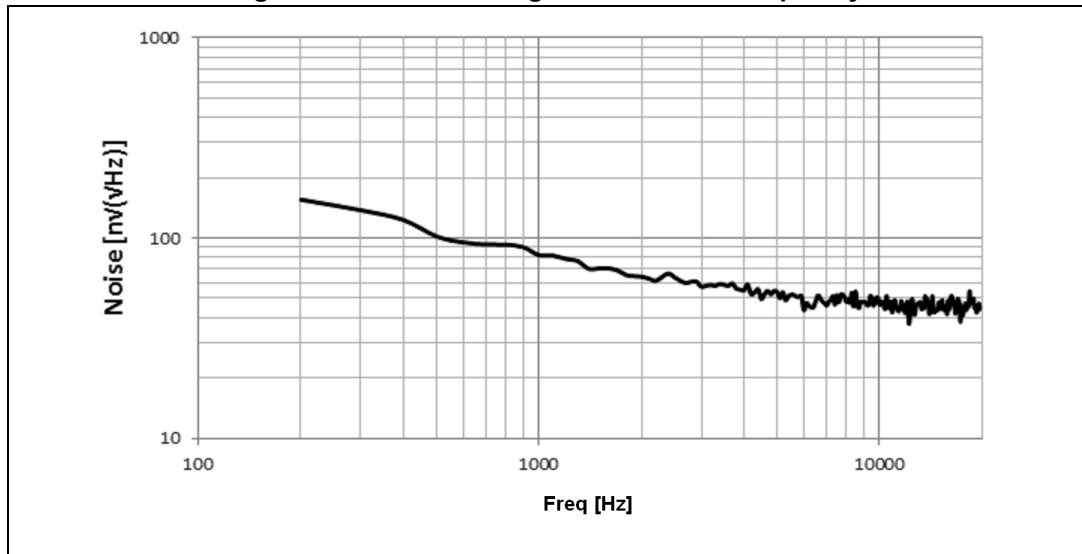
Table 88. Operational amplifier characteristics<sup>(1)</sup> (continued)

| Symbol               | Parameter   | Condition  | Min | Typ      | Max                 | Unit                   |
|----------------------|---|--|-----|----------|---------------------|------------------------|
| PGA gain             | Non inverting gain value                                    | -  | -   | 2        | -                   | -                      |
|                      |   |  | -   | 4        | -                   | -                      |
|                      |   |  | -   | 8        | -                   | -                      |
|                      |   |  | -   | 16       | -                   | -                      |
| R <sub>network</sub> | R2/R1 internal resistance values in PGA mode <sup>(3)</sup> | Gain=2   | -   | 5.4/5.4  | -                   | kΩ                     |
|                      |   | Gain=4   | -   | 16.2/5.4 | -                   |                        |
|                      |   | Gain=8   | -   | 37.8/5.4 | -                   |                        |
|                      |   | Gain=16  | -   | 40.5/2.7 | -                   |                        |
| PGA gain error       | PGA gain error  | -  | -1% | -        | 1%                  | -                      |
| I <sub>bias</sub>    | OPAMP input bias current                                    | -  | -   | -        | ±0.2 <sup>(4)</sup> | μA                     |
| PGA BW               | PGA bandwidth for different non inverting gain              | PGA Gain = 2,<br>Clload = 50pF,<br>Rload = 4 KΩ  | -   | 4        | -                   | MHz                    |
|                      |   | PGA Gain = 4,<br>Clload = 50pF,<br>Rload = 4 KΩ  | -   | 2        | -                   |                        |
|                      |   | PGA Gain = 8,<br>Clload = 50pF,<br>Rload = 4 KΩ  | -   | 1        | -                   |                        |
|                      |   | PGA Gain = 16,<br>Clload = 50pF,<br>Rload = 4 KΩ | -   | 0.5      | -                   |                        |
| en                   | Voltage noise density                                       | @ 1KHz, Output loaded with 4 KΩ                  | -   | 109      | -                   | $\frac{nV}{\sqrt{Hz}}$ |
|                      |   | @ 10KHz, Output loaded with 4 KΩ                 | -   | 43       | -                   |                        |

1. Guaranteed by design, not tested in production.
2. The saturation voltage can be also limited by the Iload (drive current).
3. R2 is the internal resistance between OPAMP output and OPAMP inverting input.  
R1 is the internal resistance between OPAMP inverting input and ground.  
The PGA gain = 1+R2/R1
4. Mostly TTa I/O leakage, when used in analog mode.



Figure 53. OPAMP voltage noise versus frequency



### 6.3.23 Temperature sensor characteristics

Table 89. TS characteristics

| Symbol                   | Parameter                                      | Min  | Typ     | Max     | Unit            |
|--------------------------|--|------|---------|---------|-----------------|
| $T_L^{(1)}$              | $V_{SENSE}$ linearity with temperature         | -    | $\pm 1$ | $\pm 2$ | $^{\circ}C$     |
| Avg_Slope <sup>(1)</sup> | Average slope                                  | 4.0  | 4.3     | 4.6     | mV/ $^{\circ}C$ |
| $V_{25}$                 | Voltage at 25 $^{\circ}C$                      | 1.34 | 1.43    | 1.52    | V               |
| $t_{START}^{(1)}$        | Startup time                                   | 4    | -       | 10      | $\mu s$         |
| $T_{S\_temp}^{(1)(2)}$   | ADC sampling time when reading the temperature | 2.2  | -       | -       | $\mu s$         |

1. Guaranteed by design, not tested in production.
2. Shortest sampling time can be determined in the application by multiple iterations.

Table 90. Temperature sensor calibration values

| Calibration value name | Description  | Memory address            |
|------------------------|--|---------------------------|
| TS_CAL1                | TS ADC raw data acquired at temperature of 30 $^{\circ}C$ , $V_{DDA} = 3.3 V$  | 0x1FFF F7B8 - 0x1FFF F7B9 |
| TS_CAL2                | TS ADC raw data acquired at temperature of 110 $^{\circ}C$ , $V_{DDA} = 3.3 V$ | 0x1FFF F7C2 - 0x1FFF F7C3 |

### 6.3.24 $V_{BAT}$ monitoring characteristics

**Table 91.  $V_{BAT}$  monitoring characteristics**

| Symbol                 | Parameter  | Min | Typ | Max | Unit       |
|------------------------|--|-----|-----|-----|------------|
| R                      | Resistor bridge for $V_{BAT}$                                | -   | 50  | -   | K $\Omega$ |
| Q                      | Ratio on $V_{BAT}$ measurement                               | -   | 2   | -   | -          |
| $E_r^{(1)}$            | Error on Q   | -1  | -   | +1  | %          |
| $T_{S\_vbat}^{(1)(2)}$ | ADC sampling time when reading the $V_{BAT}$<br>1mV accuracy | 2.2 | -   | -   | $\mu$ s    |

1. Guaranteed by design, not tested in production.
2. Shortest sampling time can be determined in the application by multiple iterations.

## 7 Package information

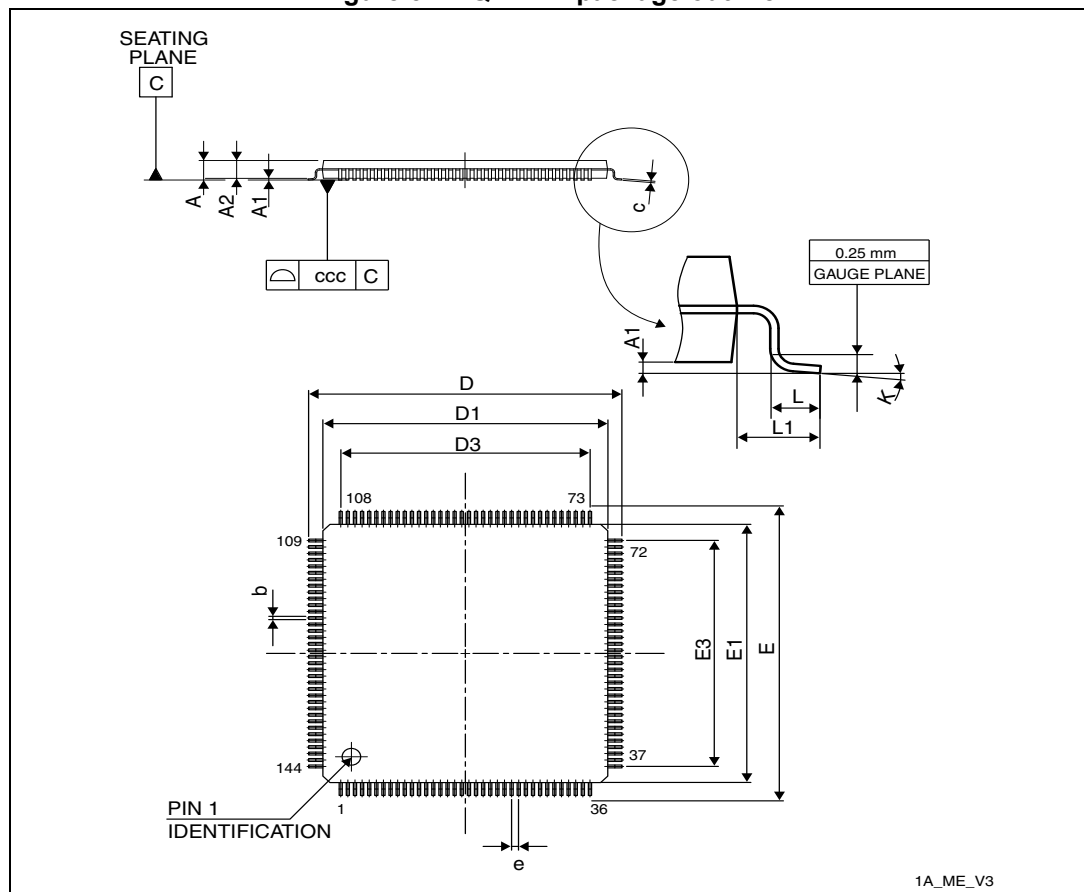
### 7.1 Package mechanical data

To meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 7.2 LQFP144 package information

LQFP144 is a 144-pin, 20 x 20 mm low-profile quad flat package.

Figure 54. LQFP144 package outline



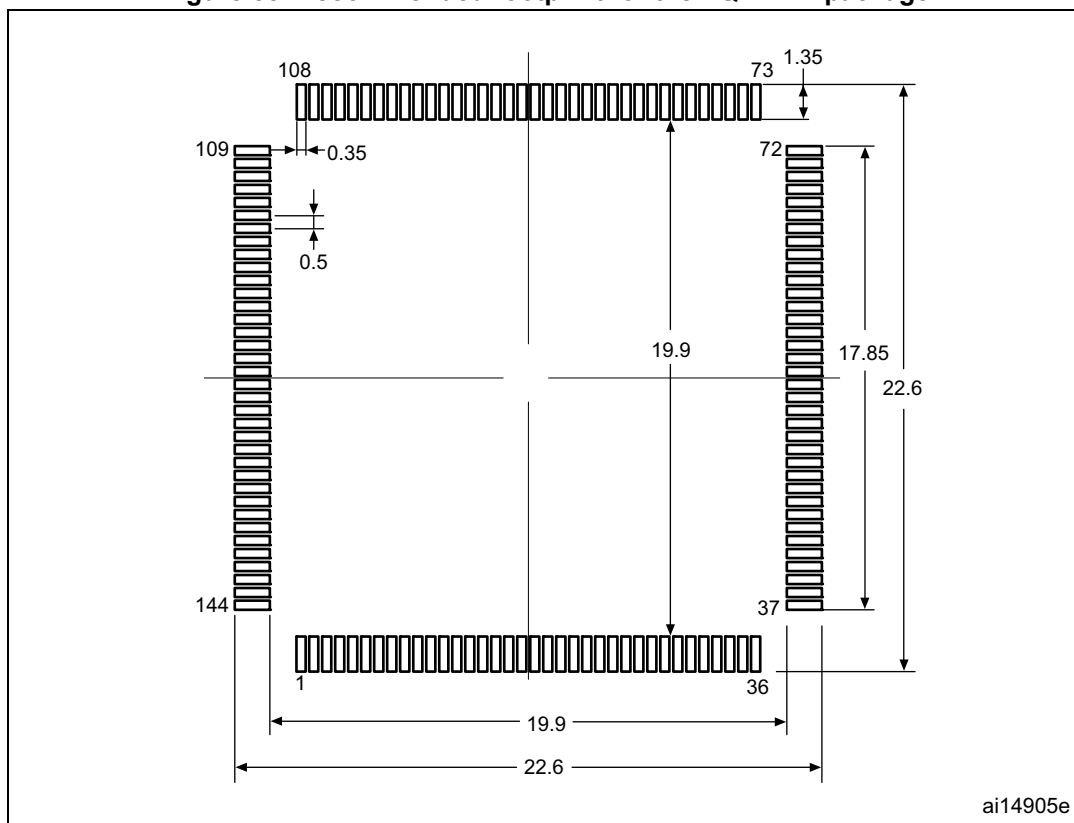
1. Drawing is not to scale.

Table 92. LQFP144 mechanical data

| Symbol | millimeters |        |        | inches <sup>(1)</sup> |        |        |
|--------|-------------|--------|--------|-----------------------|--------|--------|
|        | Min         | Typ    | Max    | Min                   | Typ    | Max    |
| A      | -           | -      | 1.600  | -                     | -      | 0.0630 |
| A1     | 0.050       | -      | 0.150  | 0.0020                | -      | 0.0059 |
| A2     | 1.350       | 1.400  | 1.450  | 0.0531                | 0.0551 | 0.0571 |
| b      | 0.170       | 0.220  | 0.270  | 0.0067                | 0.0087 | 0.0106 |
| c      | 0.090       | -      | 0.200  | 0.0035                | -      | 0.0079 |
| D      | 21.800      | 22.000 | 22.200 | 0.8583                | 0.8661 | 0.8740 |
| D1     | 19.800      | 20.000 | 20.200 | 0.7795                | 0.7874 | 0.7953 |
| D3     | -           | 17.500 | -      | -                     | 0.6890 | -      |
| E      | 21.800      | 22.000 | 22.200 | 0.8583                | 0.8661 | 0.8740 |
| E1     | 19.800      | 20.000 | 20.200 | 0.7795                | 0.7874 | 0.7953 |
| E3     | -           | 17.500 | -      | -                     | 0.6890 | -      |
| e      | -           | 0.500  | -      | -                     | 0.0197 | -      |
| L      | 0.450       | 0.600  | 0.750  | 0.0177                | 0.0236 | 0.0295 |
| L1     | -           | 1.000  | -      | -                     | 0.0394 | -      |
| k      | 0°          | 3.5°   | 7°     | 0°                    | 3.5°   | 7°     |
| ccc    | -           | -      | 0.080  | -                     | -      | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 55. Recommended footprint for the LQFP144 package



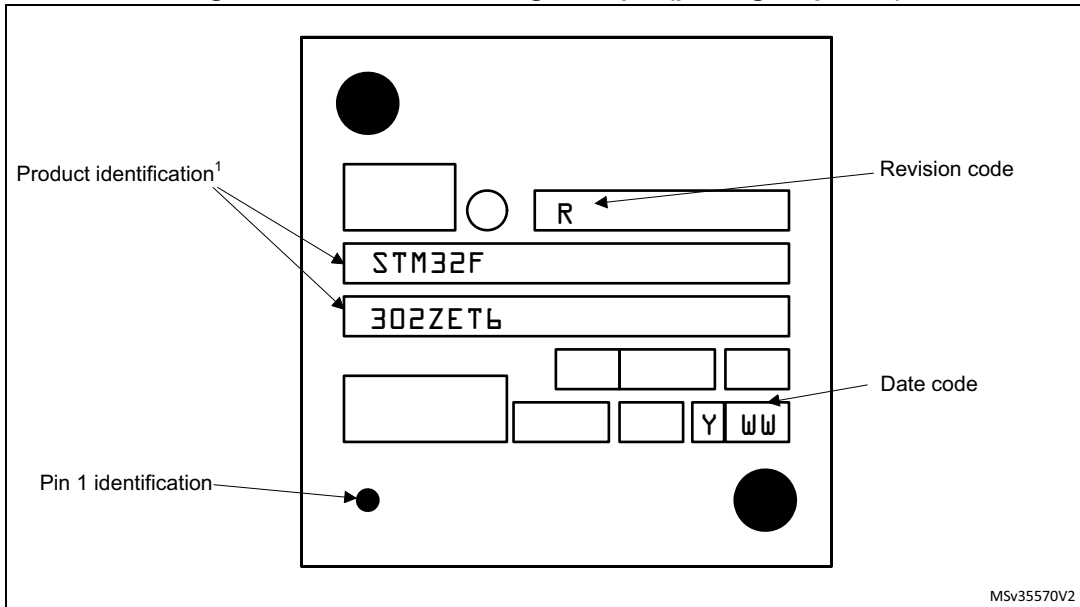
1. Drawing is not to scale.
2. Dimensions are expressed in millimeters.

**Device marking for LQFP144**

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

**Figure 56. LQFP144 marking example (package top view)**

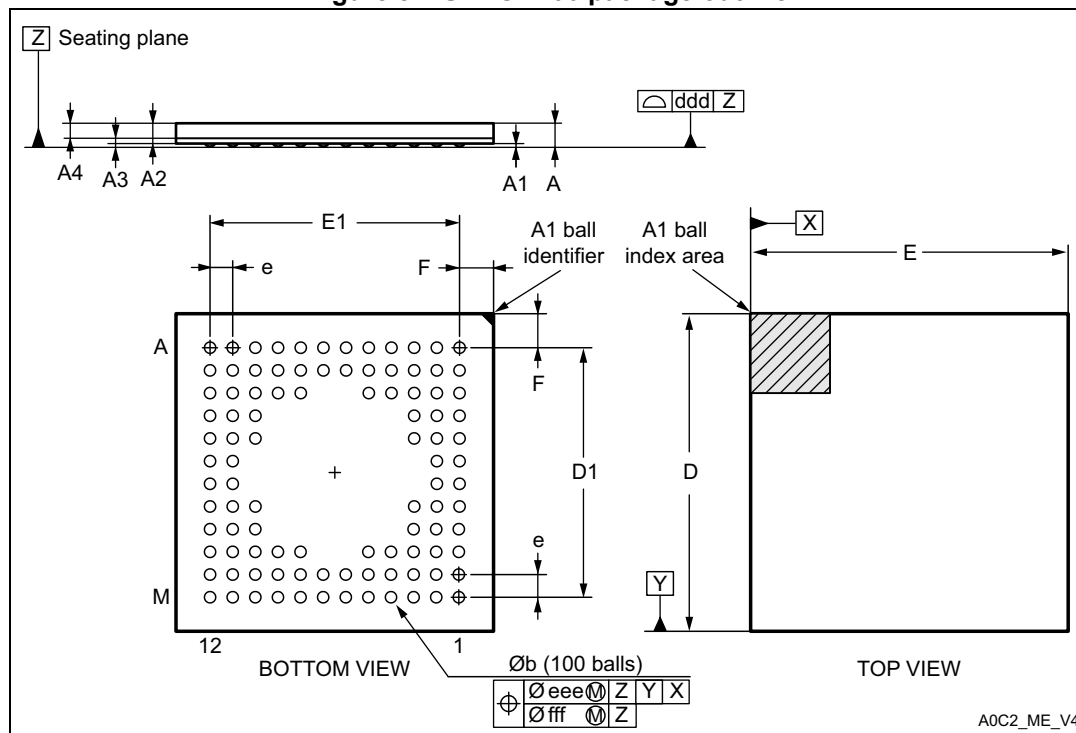


1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

### 7.3 UFBGA100 package information

UFBGA100 is a 100-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package.

Figure 57. UFBGA100 package outline



1. Drawing is not to scale.

Table 93. UFBGA100 package mechanical data

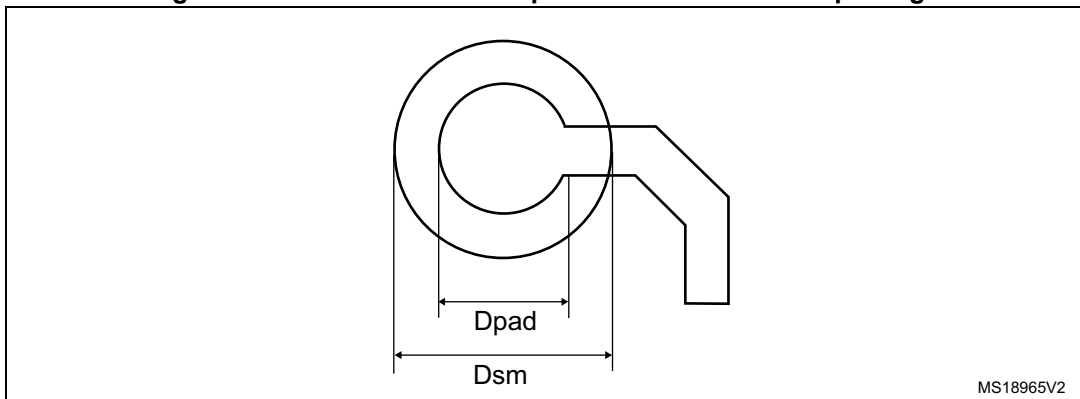
| Symbol | millimeters |       |       | inches <sup>(1)</sup> |        |        |
|--------|-------------|-------|-------|-----------------------|--------|--------|
|        | Min.        | Typ.  | Max.  | Min.                  | Typ.   | Max.   |
| A      | 0.460       | 0.530 | 0.600 | 0.0181                | 0.0209 | 0.0236 |
| A1     | 0.050       | 0.080 | 0.110 | 0.0020                | 0.0031 | 0.0043 |
| A2     | 0.400       | 0.450 | 0.500 | 0.0157                | 0.0177 | 0.0197 |
| A3     | -           | 0.130 | -     | -                     | 0.0051 | -      |
| A4     | 0.270       | 0.320 | 0.370 | 0.0106                | 0.0126 | 0.0146 |
| b      | 0.200       | 0.250 | 0.300 | 0.0079                | 0.0098 | 0.0118 |
| D      | 6.950       | 7.000 | 7.050 | 0.2736                | 0.2756 | 0.2776 |
| D1     | 5.450       | 5.500 | 5.550 | 0.2146                | 0.2165 | 0.2185 |
| E      | 6.950       | 7.000 | 7.050 | 0.2736                | 0.2756 | 0.2776 |
| E1     | 5.450       | 5.500 | 5.550 | 0.2146                | 0.2165 | 0.2185 |
| e      | -           | 0.500 | -     | -                     | 0.0197 | -      |
| F      | 0.700       | 0.750 | 0.800 | 0.0276                | 0.0295 | 0.0315 |

**Table 93. UFBGA100 package mechanical data (continued)**

| Symbol | millimeters |      |       | inches <sup>(1)</sup> |      |        |
|--------|-------------|------|-------|-----------------------|------|--------|
|        | Min.        | Typ. | Max.  | Min.                  | Typ. | Max.   |
| ddd    | -           | -    | 0.100 | -                     | -    | 0.0039 |
| eee    | -           | -    | 0.150 | -                     | -    | 0.0059 |
| fff    | -           | -    | 0.050 | -                     | -    | 0.0020 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 58. Recommended footprint for the UFBGA100 package**



**Table 94. UFBGA100 recommended PCB design rules (0.5 mm pitch BGA)**

| Dimension    | Recommended values  |
|--------------|---|
| Pitch        | 0.5   |
| Dpad         | 0.27 mm   |
| Dsm          | 0.35 mm typ. (depends on the soldermask registration tolerance) |
| Solder paste | 0.27 mm aperture diameter.                                      |

*Note:* Non-solder mask defined (NSMD) pads are recommended.

*Note:* 4 to 6 mils solder paste screen printing process.

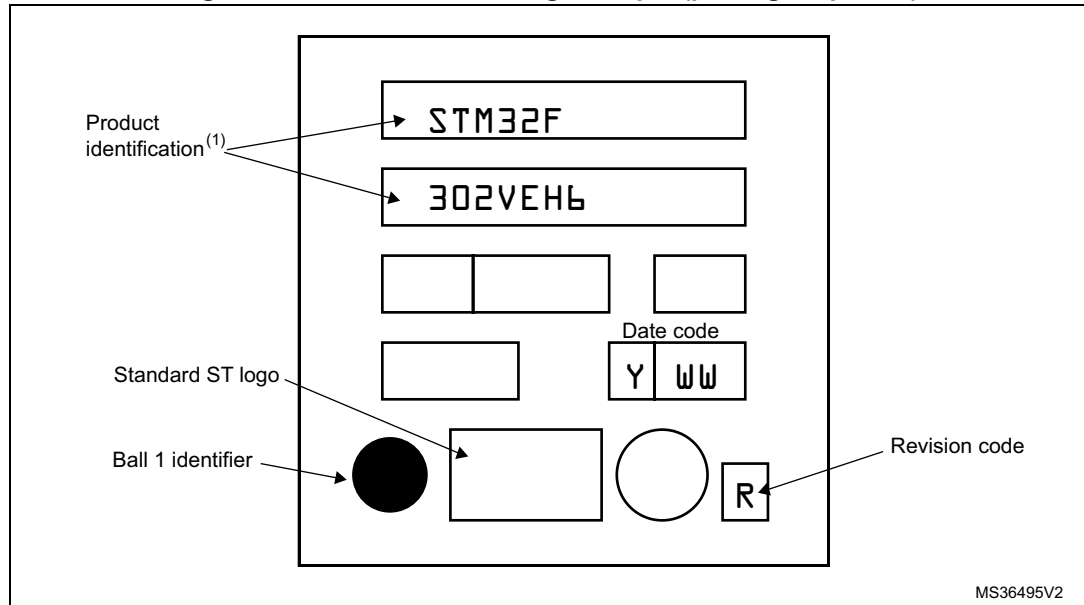


**Device marking for UFBGA100**

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

**Figure 59. UFBGA100 marking example (package top view)**

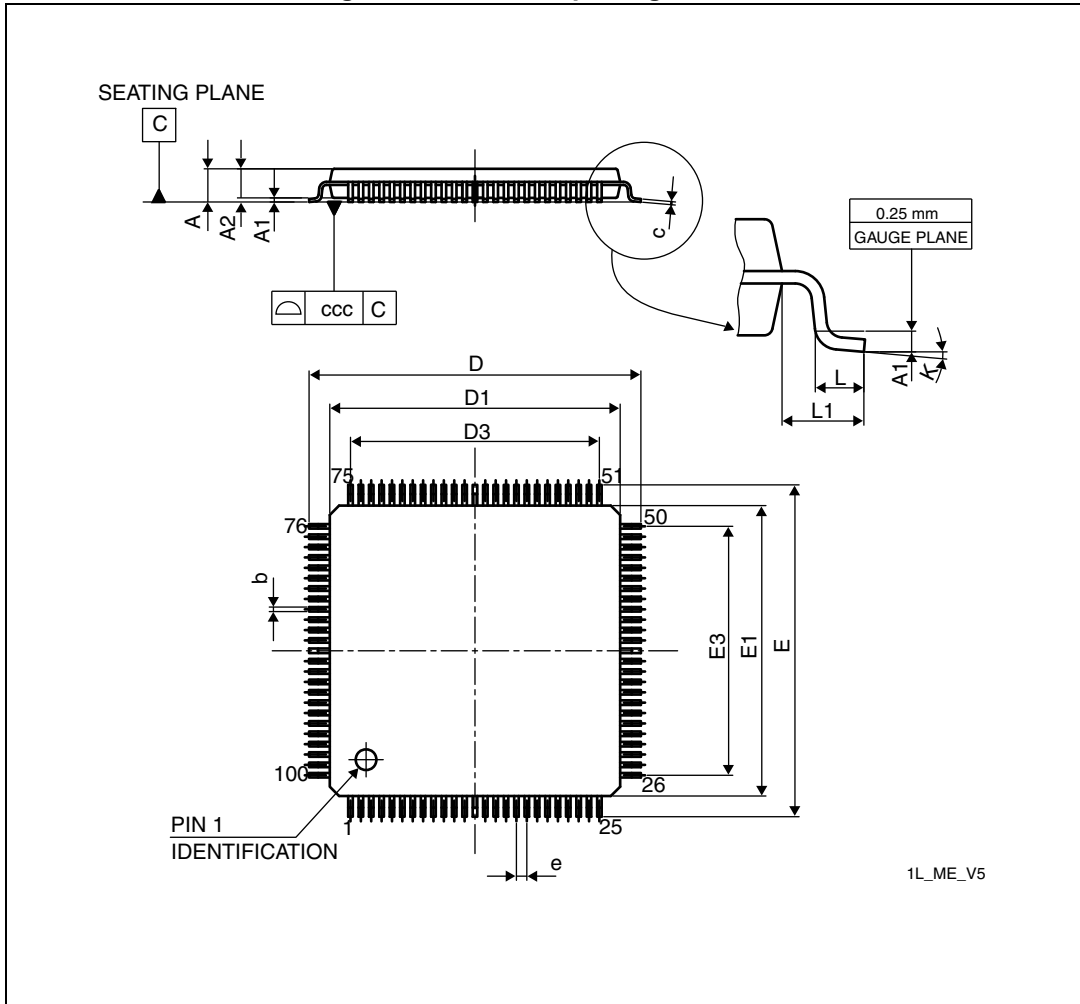


1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

### 7.4 LQFP100 package information

LQFP100 is a 100-pin, 14 x 14 mm low-profile quad flat package.

Figure 60. LQFP100 package outline



1. Drawing is not to scale.

Table 95. LQFP100 package mechanical data

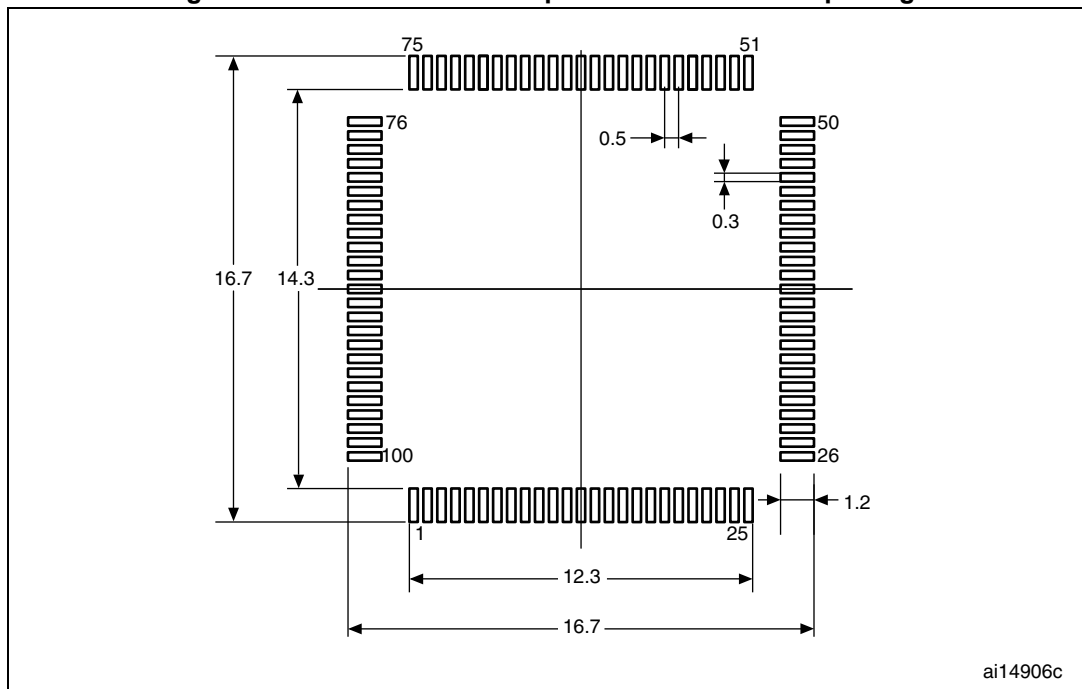
| Symbol | millimeters |        |        | inches <sup>(1)</sup> |        |        |
|--------|-------------|--------|--------|-----------------------|--------|--------|
|        | Min         | Typ    | Max    | Min                   | Typ    | Max    |
| A      | -           | -      | 1.600  | -                     | -      | 0.0630 |
| A1     | 0.050       | -      | 0.150  | 0.0020                | -      | 0.0059 |
| A2     | 1.350       | 1.400  | 1.450  | 0.0531                | 0.0551 | 0.0571 |
| b      | 0.170       | 0.220  | 0.270  | 0.0067                | 0.0087 | 0.0106 |
| c      | 0.090       | -      | 0.200  | 0.0035                | -      | 0.0079 |
| D      | 15.800      | 16.000 | 16.200 | 0.6220                | 0.6299 | 0.6378 |

Table 95. LQPF100 package mechanical data (continued)

| Symbol | millimeters |        |        | inches <sup>(1)</sup> |        |        |
|--------|-------------|--------|--------|-----------------------|--------|--------|
|        | Min         | Typ    | Max    | Min                   | Typ    | Max    |
| D1     | 13.800      | 14.000 | 14.200 | 0.5433                | 0.5512 | 0.5591 |
| D3     | -           | 12.000 | -      | -                     | 0.4724 | -      |
| E      | 15.800      | 16.000 | 16.200 | 0.6220                | 0.6299 | 0.6378 |
| E1     | 13.800      | 14.000 | 14.200 | 0.5433                | 0.5512 | 0.5591 |
| E3     | -           | 12.000 | -      | -                     | 0.4724 | -      |
| e      | -           | 0.500  | -      | -                     | 0.0197 | -      |
| L      | 0.450       | 0.600  | 0.750  | 0.0177                | 0.0236 | 0.0295 |
| L1     | -           | 1.000  | -      | -                     | 0.0394 | -      |
| k      | 0.0°        | 3.5°   | 7.0°   | 0.0°                  | 3.5°   | 7.0°   |
| ccc    | -           | -      | 0.080  | -                     | -      | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 61. Recommended footprint for the LQPF100 package



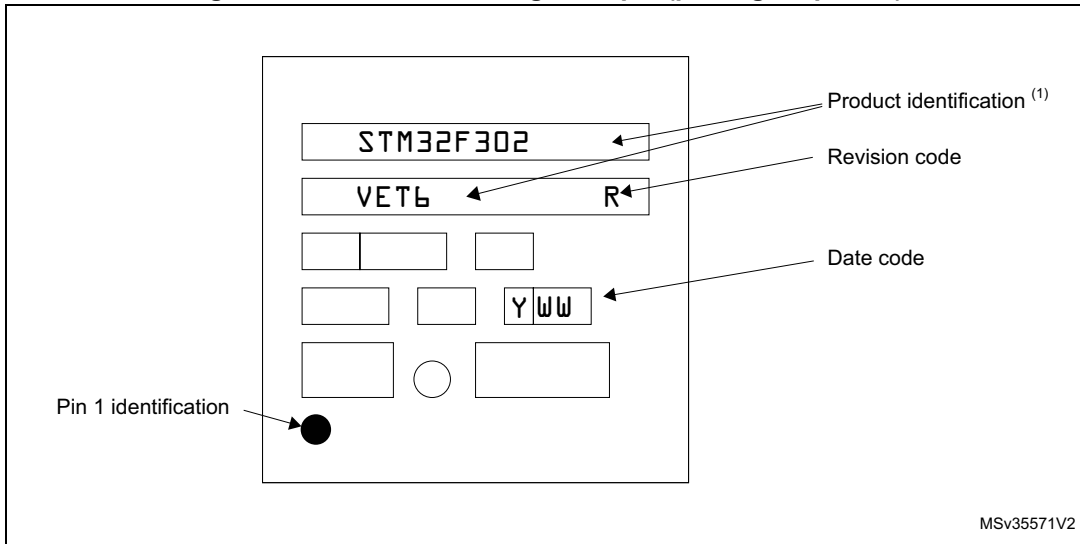
1. Drawing is not to scale.
2. Dimensions are expressed in millimeters.

**Device marking for LQFP100**

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

**Figure 62. LQFP100 marking example (package top view)**

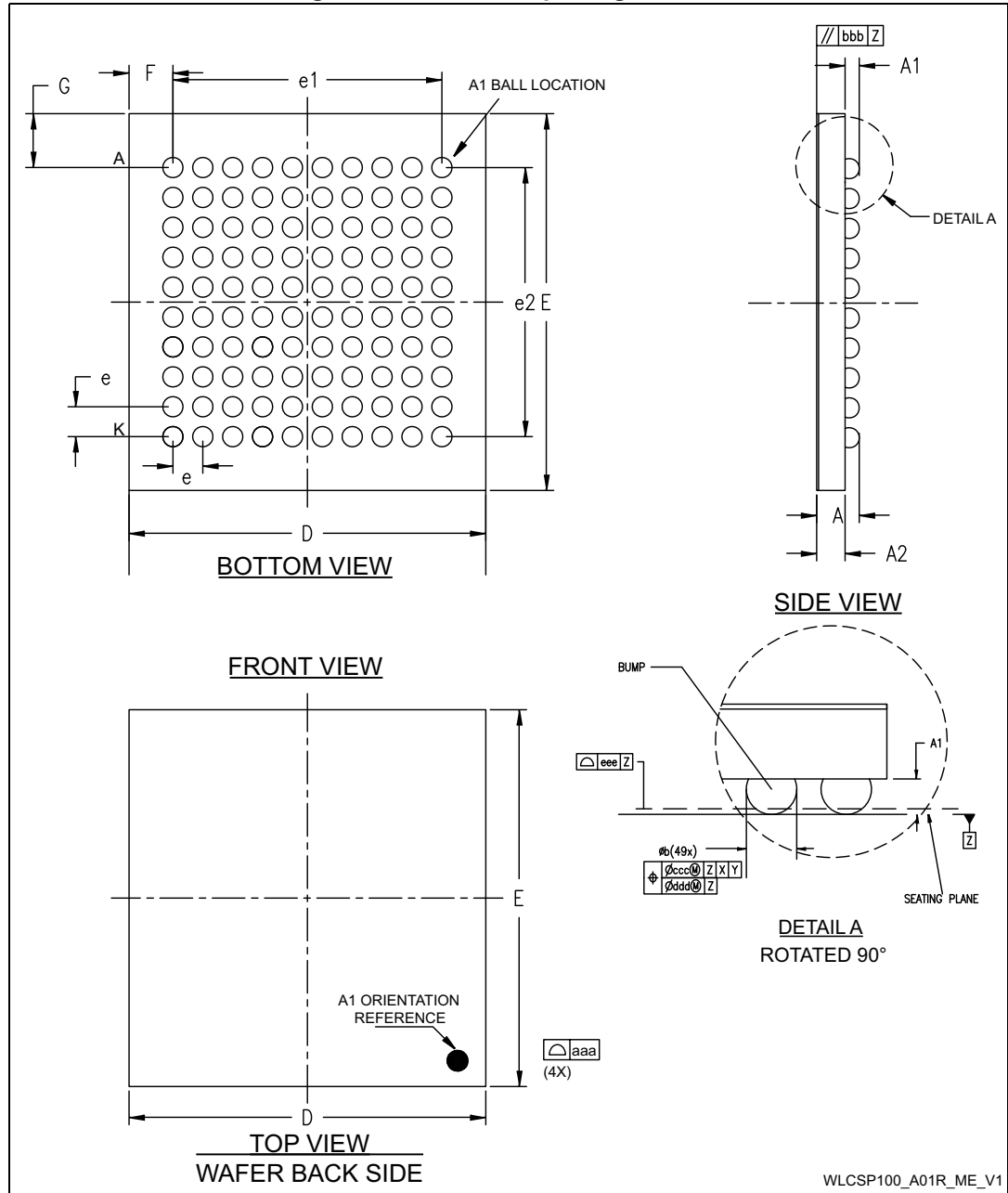


1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

### 7.5 WLCSP100 package information

WLCSP100 is a 100-ball, 4.775 x 5.041 mm, 0.4 mm pitch wafer level chip scale package.

Figure 63. WLCSP100 package outline



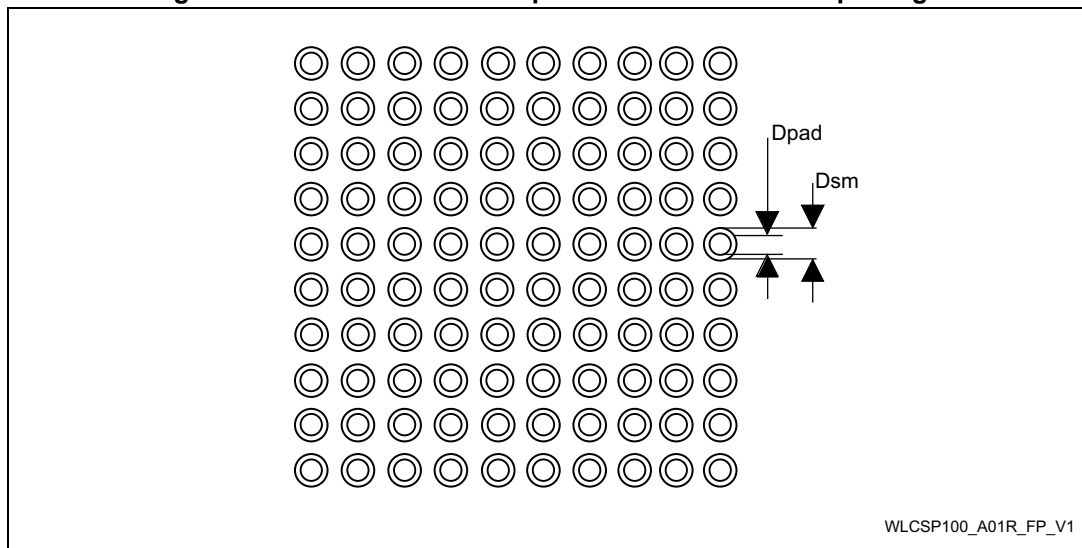
1. Drawing is not to scale.

Table 96. WLCSP100 package mechanical data

| Symbol             | millimeters |        |       | inches <sup>(1)</sup> |        |        |
|--------------------|-------------|--------|-------|-----------------------|--------|--------|
|                    | Min         | Typ    | Max   | Typ                   | Min    | Max    |
| A                  | 0.525       | 0.555  | 0.585 | 0.0207                | 0.0219 | 0.0230 |
| A1                 | -           | 0.175  | -     | -                     | 0.0069 | -      |
| A2                 | -           | 0.38   | -     | -                     | 0.0150 | -      |
| A3 <sup>(2)</sup>  | -           | 0.025  | -     | -                     | 0.0010 | -      |
| Ø b <sup>(3)</sup> | 0.22        | 0.25   | 0.28  | -                     | 0.0098 | 0.0110 |
| D                  | 4.74        | 4.775  | 4.81  | -                     | 0.1880 | 0.1894 |
| E                  | 5.006       | 5.041  | 5.076 | -                     | 0.1985 | 0.1998 |
| e                  | -           | 0.4    | -     | -                     | 0.0157 | -      |
| e1                 | -           | 3.6    | -     | -                     | 0.1417 | -      |
| e2                 | -           | 3.6    | -     | -                     | 0.1417 | -      |
| F                  | -           | 0.5875 | -     | -                     | 0.0231 | -      |
| G                  | -           | 0.7205 | -     | -                     | 0.0284 | -      |
| N                  | -           | 100    | -     | -                     | 3.9370 | -      |
| aaa                | -           | 0.1    | -     | -                     | 0.0039 | -      |
| bbb                | -           | 0.1    | -     | -                     | 0.0039 | -      |
| ccc                | -           | 0.1    | -     | -                     | 0.0039 | -      |
| ddd                | -           | 0.05   | -     | -                     | 0.0020 | -      |
| eee                | -           | 0.05   | -     | -                     | 0.0020 | -      |

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Back side coating.
3. Dimension is measured at the maximum bump diameter parallel to primary datum Z.

Figure 64. Recommended footprint for the WLCSP100 package



**Table 97. WLCSP100 recommended PCB design rules (0.4 mm pitch)**

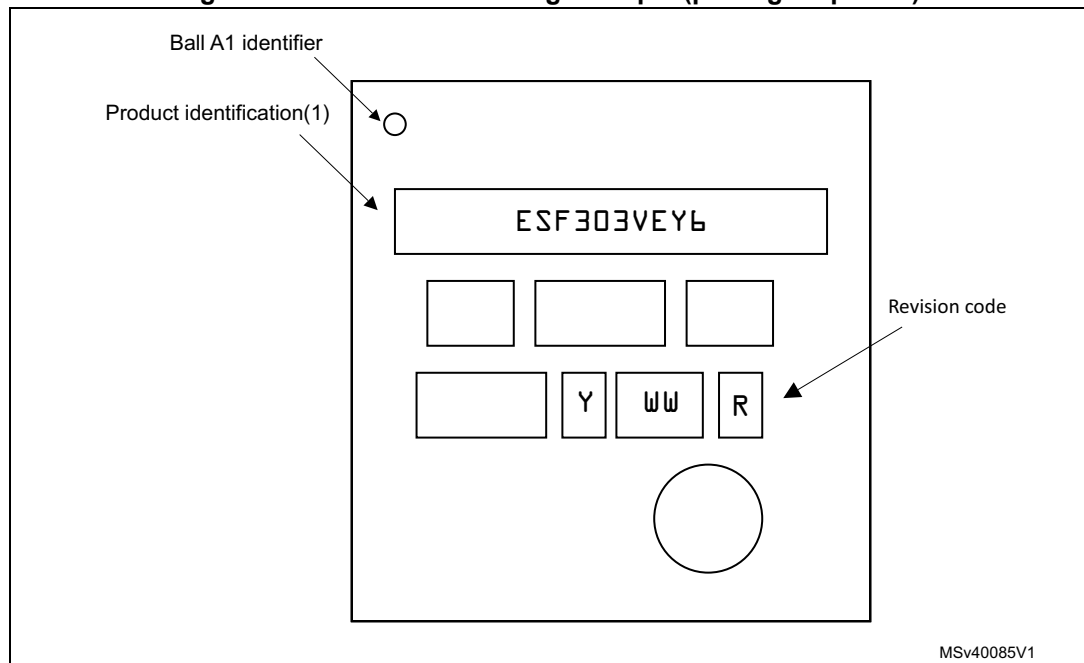
| Dimension         | Recommended values |
|-------------------|--------------------|
| Pitch             | 0.4 mm             |
| Dpad              | 0.225 mm           |
| Dsm               | 0.290 mm           |
| Stencil thickness | 0.1 mm             |

**Device marking for WLCSP100**

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

**Figure 65. WLCSP100 marking example (package top view)**

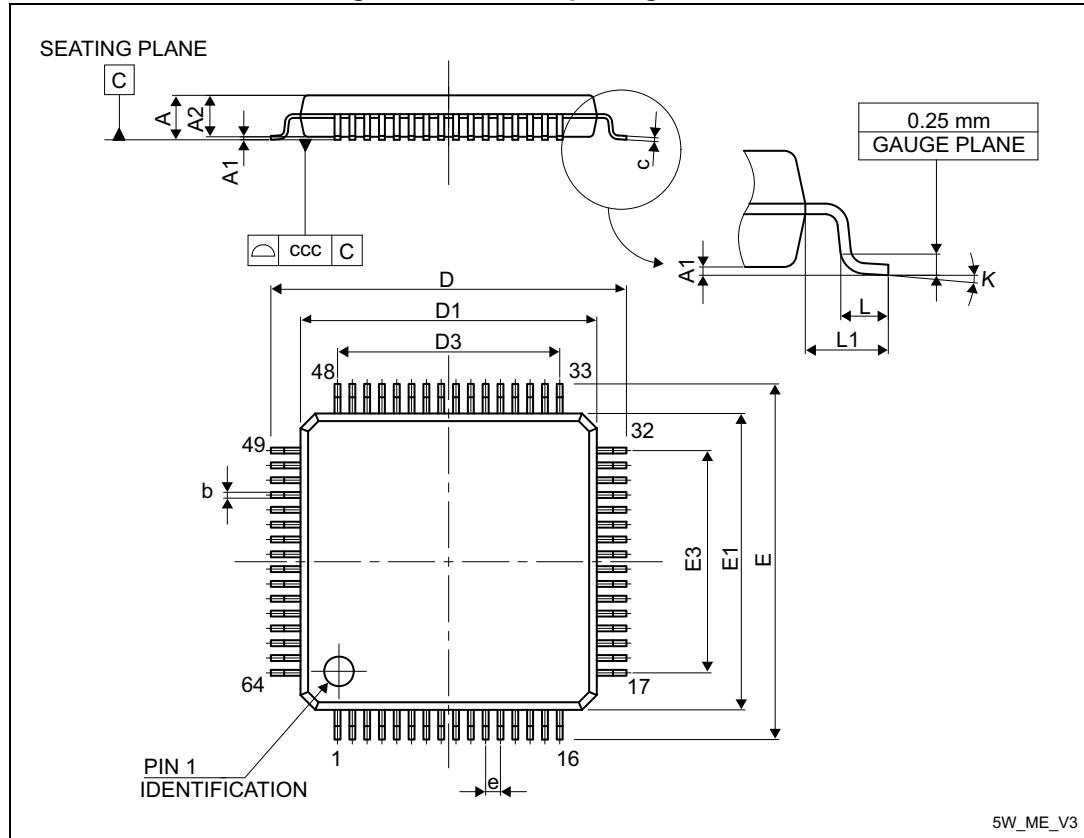


1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

### 7.6 LQFP64 package information

LQFP64 is a 64-pin, 10 x 10 mm low-profile quad flat package.

Figure 66. LQFP64 package outline



1. Drawing is not to scale.

Table 98. LQFP64 package mechanical data

| Symbol | millimeters |        |       | inches <sup>(1)</sup> |        |        |
|--------|-------------|--------|-------|-----------------------|--------|--------|
|        | Min         | Typ    | Max   | Min                   | Typ    | Max    |
| A      | -           | -      | 1.600 | -                     | -      | 0.0630 |
| A1     | 0.050       | -      | 0.150 | 0.0020                | -      | 0.0059 |
| A2     | 1.350       | 1.400  | 1.450 | 0.0531                | 0.0551 | 0.0571 |
| b      | 0.170       | 0.220  | 0.270 | 0.0067                | 0.0087 | 0.0106 |
| c      | 0.090       | -      | 0.200 | 0.0035                | -      | 0.0079 |
| D      | -           | 12.000 | -     | -                     | 0.4724 | -      |
| D1     | -           | 10.000 | -     | -                     | 0.3937 | -      |
| D3     | -           | 7.500  | -     | -                     | 0.2953 | -      |
| E      | -           | 12.000 | -     | -                     | 0.4724 | -      |
| E1     | -           | 10.000 | -     | -                     | 0.3937 | -      |

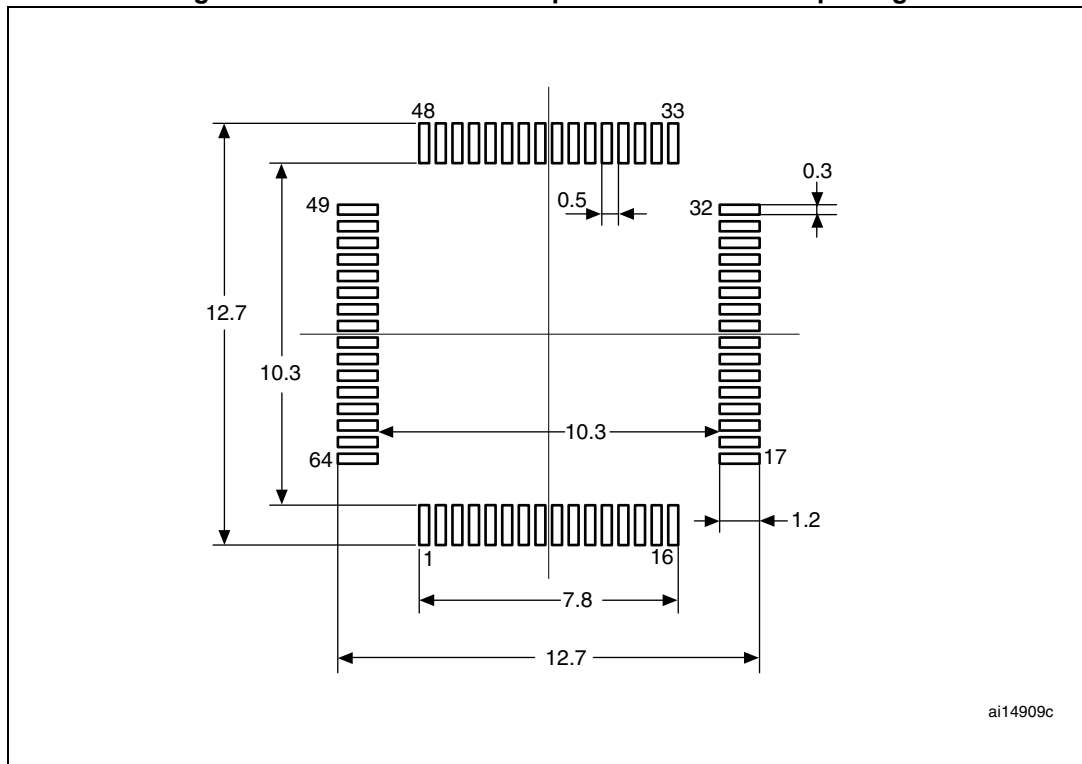


Table 98. LQFP64 package mechanical data (continued)

| Symbol | millimeters |       |       | inches <sup>(1)</sup> |        |        |
|--------|-------------|-------|-------|-----------------------|--------|--------|
|        | Min         | Typ   | Max   | Min                   | Typ    | Max    |
| E3     | -           | 7.500 | -     | -                     | 0.2953 | -      |
| e      | -           | 0.500 | -     | -                     | 0.0197 | -      |
| θ      | 0°          | 3.5°  | 7°    | 0°                    | 3.5°   | 7°     |
| L      | 0.450       | 0.600 | 0.750 | 0.0177                | 0.0236 | 0.0295 |
| L1     | -           | 1.000 | -     | -                     | 0.0394 | -      |
| ccc    | -           | -     | 0.080 | -                     | -      | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 67. Recommended footprint for the LQFP64 package



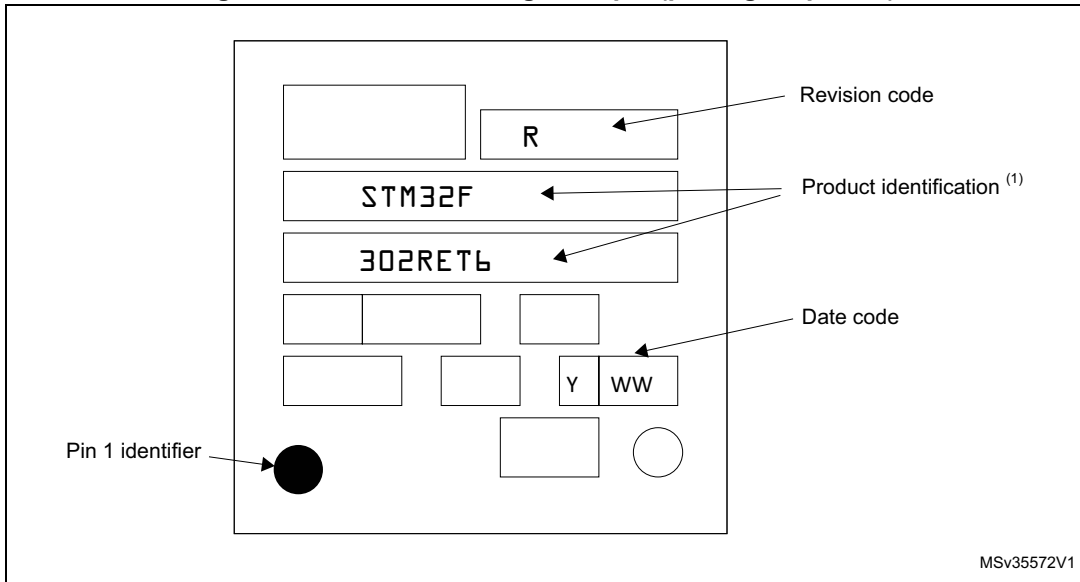
1. Dimensions are expressed in millimeters.

**Device marking for LQFP64**

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

**Figure 68. LQFP64 marking example (package top view)**



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

## 7.7 Thermal characteristics

The maximum chip junction temperature ( $T_{Jmax}$ ) must never exceed the values given in [Table 19: General operating conditions](#).

The maximum chip-junction temperature,  $T_J$  max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- $T_A$  max is the maximum temperature in °C,
- $\Theta_{JA}$  is the package junction-to- thermal resistance, in °C/W,
- $P_D$  max is the sum of  $P_{INT}$  max and  $P_{I/O}$  max ( $P_D$  max =  $P_{INT}$  max +  $P_{I/O}$ max),
- $P_{INT}$  max is the product of  $I_{DD}$  and  $V_{DD}$ , expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$  max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma ((V_{DD} - V_{OH}) \times I_{OH}),$$

taking into account the actual  $V_{OL} / I_{OL}$  and  $V_{OH} / I_{OH}$  of the I/Os at low and high level in the application.

**Table 99. Package thermal characteristics**

| Symbol        | Parameter  | Value | Unit |
|---------------|--|-------|------|
| $\Theta_{JA}$ | Thermal resistance junction-<br>LQFP144 - 20 × 20 mm               | 33    | °C/W |
|               | Thermal resistance junction-<br>UFBGA100 - 7 × 7 mm                | 59    |      |
|               | Thermal resistance junction-<br>LQFP100 - 14 × 14 mm               | 42    |      |
|               | Thermal resistance junction-<br>WLCSP100 - 0.4 mm pitch            | 44    |      |
|               | Thermal resistance junction-<br>LQFP64 - 10 × 10 mm / 0.5 mm pitch | 46    |      |

### 7.7.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from [www.jedec.org](http://www.jedec.org)

### 7.7.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in [Section 8: Part numbering](#).

Each temperature range suffix corresponds to a specific guaranteed temperature at maximum dissipation and to a specific maximum junction temperature.

As applications do not commonly use the STM32F302xD/E at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range is best suited to the application.

The following examples show how to calculate the temperature range needed for a given application.

### Example 1: High-performance application

Assuming the following application conditions:

Maximum temperature  $T_{Amax} = 82\text{ °C}$  (measured according to JESD51-2),  
 $I_{DDmax} = 50\text{ mA}$ ,  $V_{DD} = 3.5\text{ V}$ , maximum 20 I/Os used at the same time in output at low level with  $I_{OL} = 8\text{ mA}$ ,  $V_{OL} = 0.4\text{ V}$  and maximum 8 I/Os used at the same time in output at low level with  $I_{OL} = 20\text{ mA}$ ,  $V_{OL} = 1.3\text{ V}$

$$P_{INTmax} = 50\text{ mA} \times 3.5\text{ V} = 175\text{ mW}$$

$$P_{IOmax} = 20 \times 8\text{ mA} \times 0.4\text{ V} + 8 \times 20\text{ mA} \times 1.3\text{ V} = 272\text{ mW}$$

This gives:  $P_{INTmax} = 175\text{ mW}$  and  $P_{IOmax} = 272\text{ mW}$ :

$$P_{Dmax} = 175 + 272 = 447\text{ mW}$$

Using the values obtained in [Table 99](#)  $T_{Jmax}$  is calculated as follows:

– For LQFP100,  $42\text{ °C/W}$

$$T_{Jmax} = 82\text{ °C} + (42\text{ °C/W} \times 447\text{ mW}) = 82\text{ °C} + 18.774\text{ °C} = 100.774\text{ °C}$$

This is within the range of the suffix 6 version parts ( $-40 < T_J < 105\text{ °C}$ ).

In this case, parts must be ordered at least with the temperature range suffix 6 (see [Section 8: Part numbering](#)).

*Note:* With this given  $P_{Dmax}$  we can find the  $T_{Amax}$  allowed for a given device temperature range (order code suffix 6 or 7).

$$\text{Suffix 6: } T_{Amax} = T_{Jmax} - (42\text{ °C/W} \times 447\text{ mW}) = 105 - 18.774 = 86.226\text{ °C}$$

$$\text{Suffix 7: } T_{Amax} = T_{Jmax} - (42\text{ °C/W} \times 447\text{ mW}) = 125 - 18.774 = 106.226\text{ °C}$$

### Example 2: High-temperature application

Using the same rules, it is possible to address applications that run at high temperature with a low dissipation, as long as junction temperature  $T_J$  remains within the specified range.

Assuming the following application conditions:

Maximum temperature  $T_{Amax} = 100\text{ °C}$  (measured according to JESD51-2),  
 $I_{DDmax} = 20\text{ mA}$ ,  $V_{DD} = 3.5\text{ V}$ , maximum 20 I/Os used at the same time in output at low level with  $I_{OL} = 8\text{ mA}$ ,  $V_{OL} = 0.4\text{ V}$

$$P_{INTmax} = 20\text{ mA} \times 3.5\text{ V} = 70\text{ mW}$$

$$P_{IOmax} = 20 \times 8\text{ mA} \times 0.4\text{ V} = 64\text{ mW}$$

This gives:  $P_{INTmax} = 70\text{ mW}$  and  $P_{IOmax} = 64\text{ mW}$ :

$$P_{Dmax} = 70 + 64 = 134\text{ mW}$$

Thus:  $P_{Dmax} = 134\text{ mW}$

Using the values obtained in [Table 99](#)  $T_{Jmax}$  is calculated as follows:

– For LQFP100,  $42\text{ °C/W}$

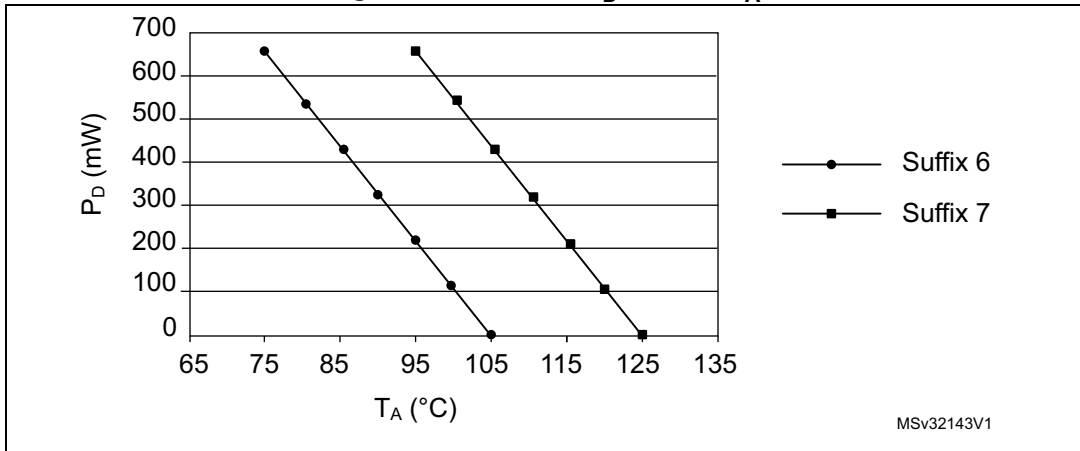
$$T_{Jmax} = 100\text{ °C} + (42\text{ °C/W} \times 134\text{ mW}) = 100\text{ °C} + 5.628\text{ °C} = 105.628\text{ °C}$$

This is above the range of the suffix 6 version parts ( $-40 < T_J < 105\text{ °C}$ ).

In this case, parts must be ordered at least with the temperature range suffix 7 (see [Section 8: Part numbering](#)) unless we reduce the power dissipation to be able to use suffix 6 parts.

Refer to [Figure 69](#) to select the required temperature range (suffix 6 or 7) according to your temperature or power requirements.

Figure 69. LQFP100 P<sub>D</sub> max vs. T<sub>A</sub>



# 8 Part numbering

For a list of available options (memory, package, and so on) or for further information on any aspect of this device, contact the nearest ST sales office.

**Table 100. Ordering information scheme**

| Example:   | STM32 | F | 302 | V | E | T | 6 | x |
|--|-------|---|-----|---|---|---|---|---|
| <b>Device family</b><br>STM32 = ARM-based 32-bit microcontroller                     |       |   |     |   |   |   |   |   |
| <b>Product type</b><br>F = General-purpose   |       |   |     |   |   |   |   |   |
| <b>Sub-family</b><br>302 = STM32F302xx   |       |   |     |   |   |   |   |   |
| <b>Pin count</b><br>R = 64 pins<br>V = 100 pins<br>Z = 144 pins                      |       |   |     |   |   |   |   |   |
| <b>Code size</b><br>D = 384 Kbytes of Flash memory<br>E = 512 Kbytes of Flash memory |       |   |     |   |   |   |   |   |
| <b>Package</b><br>H = UFBGA<br>T = LQFP<br>Y = WLCSP                                 |       |   |     |   |   |   |   |   |
| <b>Temperature range</b><br>6 = -40 to 85 °C<br>7 = -40 to 105 °C                    |       |   |     |   |   |   |   |   |
| <b>Options</b><br>xxx = programmed parts<br>TR = tape and reel                       |       |   |     |   |   |   |   |   |

## 9 Revision history

**Table 101. Document revision history**

| Date        | Revision | Changes  |
|-------------|----------|--|
| 20-Jan-2015 | 1        | Initial release.   |
| 09-Apr-2015 | 2        | Added USB_DM and USB_DP as additional function to PA11 and PA12 description, respectively in <a href="#">Table 13: STM32F302xD/E pin definitions</a> .<br>Updated:<br>– <a href="#">Figure 56: LQFP144 marking example (package top view)</a> ,<br>– <a href="#">Figure 59: UFBGA100 marking example (package top view)</a> ,<br>– <a href="#">Figure 62: LQFP100 marking example (package top view)</a> .   |
| 08-Mar-2016 | 3        | Renamed:<br>– FMC as FSMC,<br>– CCM RAM as CCM SRAM.<br>Removed:<br>– <a href="#">table: I2C timings specification</a> and <a href="#">Figure: I2C bus AC waveforms and measurement circuit</a> in <a href="#">Section : I2C interface characteristics</a> .<br>Added:<br>– Package information for WLCSP100 in <a href="#">Section 7: Package information</a> .   |
| 18-Oct-2016 | 4        | Updated:<br><a href="#">Table 2: STM32F302xD/E family device features and peripheral counts</a> , <a href="#">Section 3.17: Ultra-fast comparators (COMP)</a> , <a href="#">Table 66: DAC characteristics</a> , <a href="#">Table 61: ADC characteristics</a> , <a href="#">Table 13: STM32F302xD/E pin definitions</a> , <a href="#">Table 14: STM32F302xD/E alternate function mapping</a> , <a href="#">Figure 41: Recommended NRST pin protection</a><br>Added:<br><a href="#">Table 37: Wakeup time using USART</a> . |

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