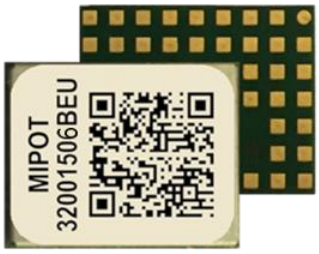
Wireless Protocol Modules MiP Series 32001506xEU Family

Stand Alone LoRa™ Modem with MCU

Datasheet



Overview

The 32001506xEU is a family of transceivers operating in the 868 MHz SRD Band optimized for very long range, low power applications, suitable for LPWA networks. Based on LoRa® RF Technology, it provides ultra-long range spread spectrum communication and high interference immunity.

Thanks to its small LGA form factor (11.3 x 8.9 mm only) and its low current consumption, this module allows the implementation of highly integrated low power (battery operated) solutions for Internet of Things (IoT) applications, security systems, sensor networks, metering, smart buildings, agriculture, supply chain.

The 32001506xEU family features a dual core microcontroller in which one is dedicated to the radio stack and the ARM Cortex M4 is free for the customer application firmware.

The available radio stacks support a wide range of applications using the LoRa modulation, accelerating the development of a LoRaWAN application (32001506BEU), or a local star network using the LoRa Mipot stack (32001506CEU). Using the LoRa Modem stack (32001506DEU), it is easy to create point-to-point applications or build a more complex custom stack. The 32001506FEU contains all the aforementioned stack allowing to switch between them at runtime.

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1. Product Features

Mechanical highlights:

- ✓ Extremely compact dimensions
- ✓ LGA pattern

Low power characteristics:

- ✓ Sleep current consumption 2.2 µA
- ✓ 11 mA in RX mode

Memories:

- ✓ 196 Kbyte Flash memory
- ✓ 32 Kbyte RAM
- ✓ 512 byte OTP (One Time Programmable) memory

RF performances:

- ✓ -135 dBm Sensitivity @LoRa®
- ✓ +14 dBm Output power

Additional features:

- ✓ ARM Cortex-M4 CPU
- ✓ Preloaded radio library
- ✓ Internal communication channel with the radio peripheral
- ✓ Based on STM32WL55J

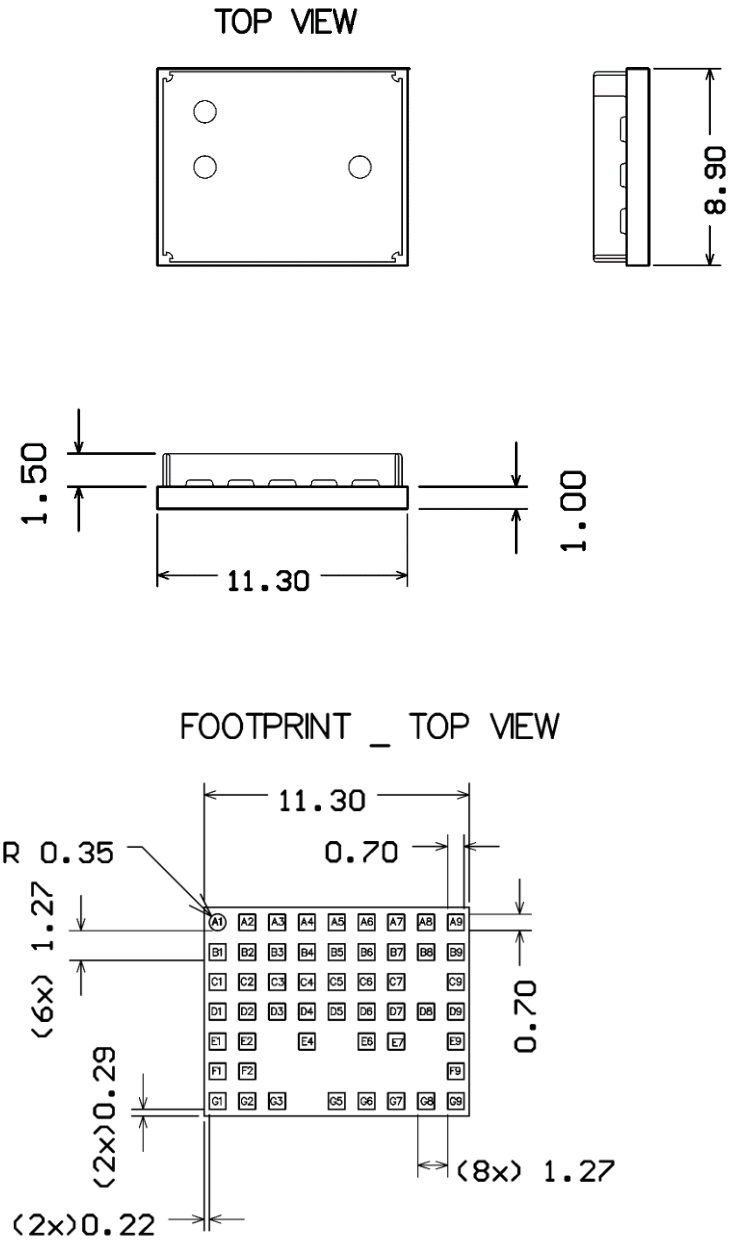
Multiple Stacks available:

- ✓ LoRaWAN (32001506BEU)
- ✓ LoRa Mipot (32001506CEU)
- ✓ LoRa Modem (32001506DEU)
- ✓ LoRa Multistack (32001506FEU)

Regulatory compliance:

- ✓ 2014/53/EU (RED)
- ✓ EN 300 220-1 v3.1.1 (2017-02)
- ✓ EN 300 220-2 v3.1.1 (2017-02)
- ✓ EN 301 489-1 v2.2.3 (2019-11)
- ✓ EN 301 489-3 v2.2.0 (2021-11)
- ✓ EN IEC 62311:2020
- ✓ IEC 62321:2008 / IEC 62321-1:2013 / IEC 62321-2:2013 / IEC 62321-3-1:2014
- ✓ EN 62321:2009/ EN 62321-1:2013 / EN 62321-2:2014 / EN 62321-3-1:2014
- ✓ UNE EN 62321:2009 / UNE EN 62321-1:2009 / UNE EN 62321-2:2014 / UNE EN 62321-3-1:2014
- ✓ EN 62368-1:2014 + AC:2015 + AC:2017 + A11:2017
- ✓ IEC 62368-1:2014 + COR1:2015 + COR2:2015
- ✓ UNE-EN 62368-1:2014 + AC1:2015 + AC2:2015 + AC:2017 + A11:2017

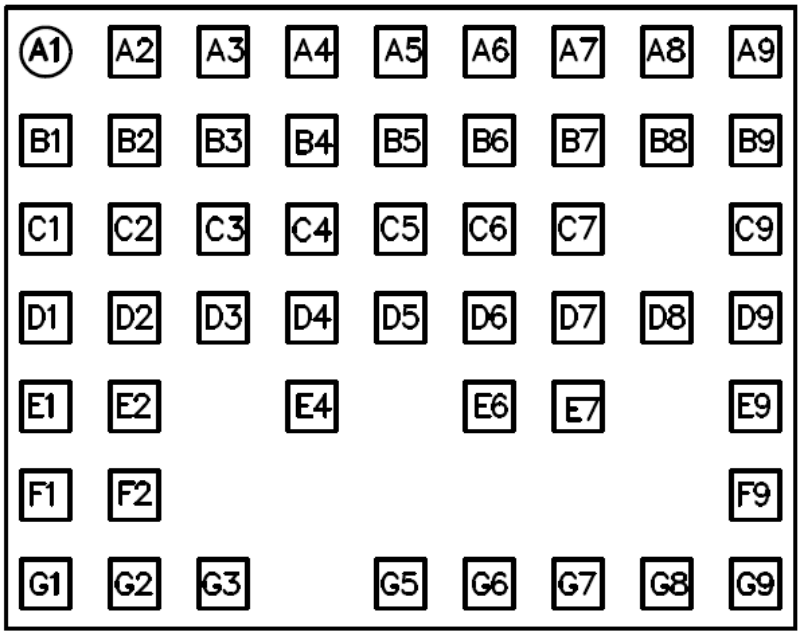
2. Mechanical Dimensions



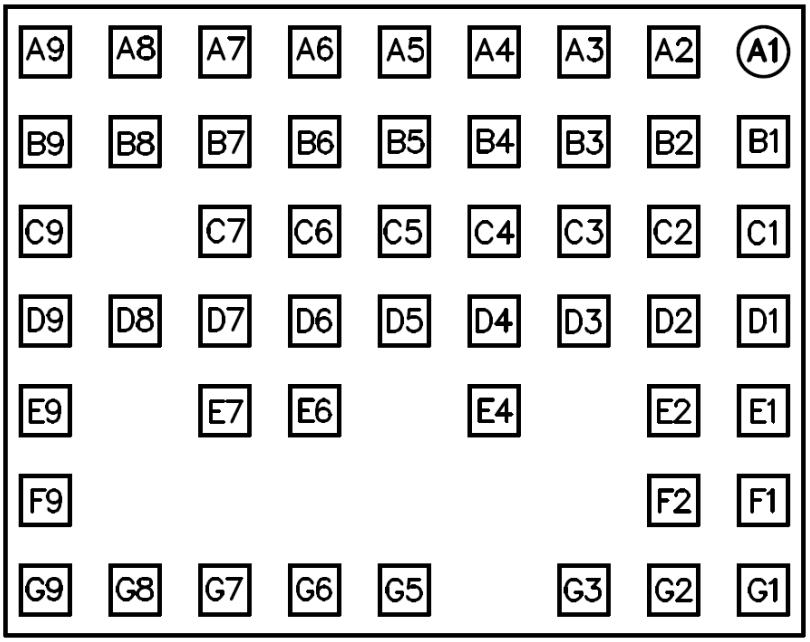
Note: Dimension in mm. General tolerance ±0.1mm. The tolerance is not cumulative

3. Pin Definition

Top View



Bottom View



32001506DEU LGA PAD	STM32WL BGA BALL
A1	PA6
A2	PA5
A3	PA4
A4	PC0
A5	PC1
A6	PB5
A7	PB8
A8	PB9
A9	VDD
B1	PA7
B2	PC6
B3	PA2
B4	PA3
B5	PB6
B6	PB7
B7	PA15
B8	VDDA
B9	VDD
C1	PH3-BOOT0
C2	PA8
C3	PA1
C4	GND
C5	PA0
C6	PB4
C7	VREF+
C9	GND

32001506DEU LGA PAD	STM32WL BGA BALL
D1	GND
D2	PB10
D3	PB11
D4	GND
D5	PB14
D6	PA10
D7	VBAT
D8	PB13
D9	PC2
E1	GND
E2	GND
E4	PB1
E6	PB2
E7	PA12
E9	PC3
F1	ANT
F2	GND
F9	PB12
G1	GND
G2	GND
G3	GND
G5	NRST
G6	SWDIO
G7	SWCLK
G8	SWO
G9	PA9

4. Firmware development

4.1. Overview

The 32001506xEU family module is based on the STM32WL55J and embeds the necessary circuitry for the RF subsystem in the 868 MHz band. The MCU employs an asymmetrical dual core CPU comprised of an ARM Cortex-M4 and an ARM Cortex-M0+.

The Cortex-M0+ core is reserved for the RF stack while the user code runs on the Cortex-M4. The communication between the cores is done using the Inter-Processor Communication Controller (IPCC).

The RF stack is preloaded in the module and uses the same set of commands of the host based version.

For details about the MCU, please refer to STM32WL55J data sheet (DS13293) and reference manual (RM0453).

4.2. Memory organization

The memory available for the user code depend on the model because of different memory requirements of the different stacks, and is shown in the following tables.

Available memory for 32001506BEU

Start address	End Address	Length	Description
0x0800 0000	TBD	TBD	User Flash Memory
0x2000 0000	0x2000 7FFF	32768	User RAM
0x2000 8000	0x2000 83FF	1024	IPCC RAM
0x1FFF 7200	0x1FFF 73FF	512	User OTP Memory

Available memory for 32001506CEU

Start address	End Address	Length	Description
0x0800 0000	TBD	TBD	User Flash Memory
0x2000 0000	0x2000 7FFF	32768	User RAM
0x2000 8000	0x2000 83FF	1024	IPCC RAM
0x1FFF 7200	0x1FFF 73FF	512	User OTP Memory

Available memory for 32001506DEU

Start address	End Address	Length	Description
0x0800 0000	0x0802 FFFF	196608	User Flash Memory
0x2000 0000	0x2000 7FFF	32768	User RAM
0x2000 8000	0x2000 83FF	1024	IPCC RAM
0x1FFF 7200	0x1FFF 73FF	512	User OTP Memory

Available memory for 32001506FEU

Start address	End Address	Length	Description
0x0800 0000	TBD	TBD	User Flash Memory
0x2000 0000	0x2000 7FFF	32768	User RAM
0x2000 8000	0x2000 83FF	1024	IPCC RAM
0x1FFF 7200	0x1FFF 73FF	512	User OTP Memory

4.3. Reserved Pins

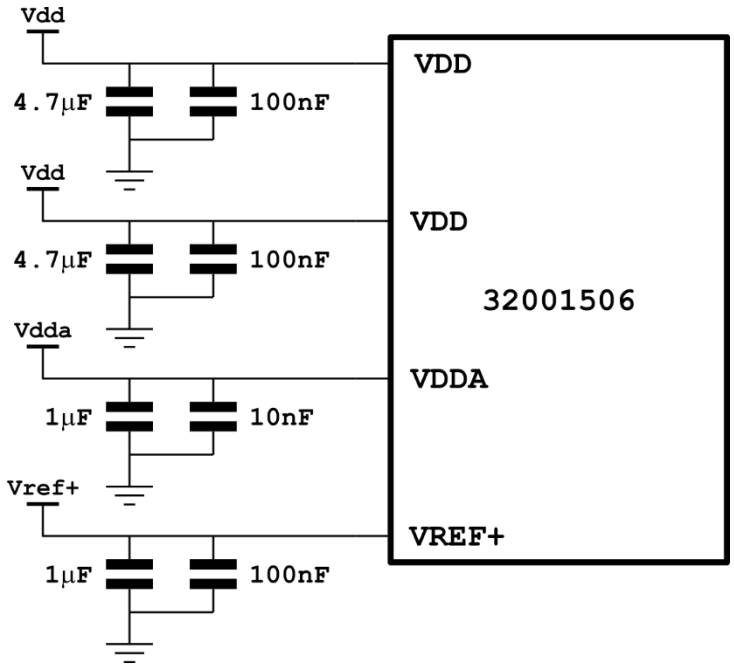
Some Pins of the STM32WL55J are reserved for internal use, so those are not available for the user application and must be not modified in any way.

- PA11
- PB0
- PC4
- PC5
- PC13
- PC15

5. Hardware integration

5.1. Decoupling capacitors

Each power supply pin must be decoupled with capacitors with the values suggested in the figure.



5.2. Layout guidelines

For better noise rejection, put the decoupling capacitors as close as possible to the power pins of the module, giving precedence to the low value ones.

The trace connecting to the RF pin must have an impedance of 50 Ω. For better performance, connect the GND pads around the RF pin without thermals.

6. Electrical Characteristics

6.1. Absolute Maximum Ratings

Parameter	Max.	Unit
Supply Voltage (VDD)	+3.9	V
Radio Frequency Input Level, pin F1	0	dBm
Voltage Standing Wave Radio (VSWR) at RF Input, ANT, pad F1	10:1	
I/O Pin voltage	VDD + 0.3	V
Storage Temperature	-40 ÷ 100	°C
Operating Temperature	-40 ÷ 85	°C

6.2. Operating Condition

Note: All RF parameters measured with input (pad F1, ANT) connected to a 50 Ω impedance signal source or load.

GENERAL ELECTRICAL CHARACTERISTICS @ 25 °C

Parameter	Min.	Typ.	Max.	Unit	Notes
Supply Voltage (VDD)	1.9	3.0	3.6	V	
VDDA	0	-	3.6	V	
VBAT	1.55	-	3.6	V	
VIN	-0.3	-	VDD+0.3	V	
Sleep DC Current	-	2.2	3.0	µA	

RECEIVER ELECTRICAL CHARACTERISTICS @ 25 °C

Parameter	Min.	Typ.	Max.	Unit	Notes
DC Current Drain	-	-	11	mA	6
Operating Frequency	868.0	-	868.6	MHz	
Channel Frequency Precision	-	±15	-	kHz	
Sensitivity, 2-FSK	-	-115	-	dBm	2,3,5
Sensitivity, LoRa®	-	-135	-	dBm	2,4,5
Image Frequency Rejection	-	54	-	dB	7
Spurious radiated level	-	-	-57	dBm	
Output Logic Low	GND	-	0.05	V	
Output Logic High	VDD-0.2	-	VDD	V	

TRANSMITTER ELECTRICAL CHARACTERISTICS @ 25 °C

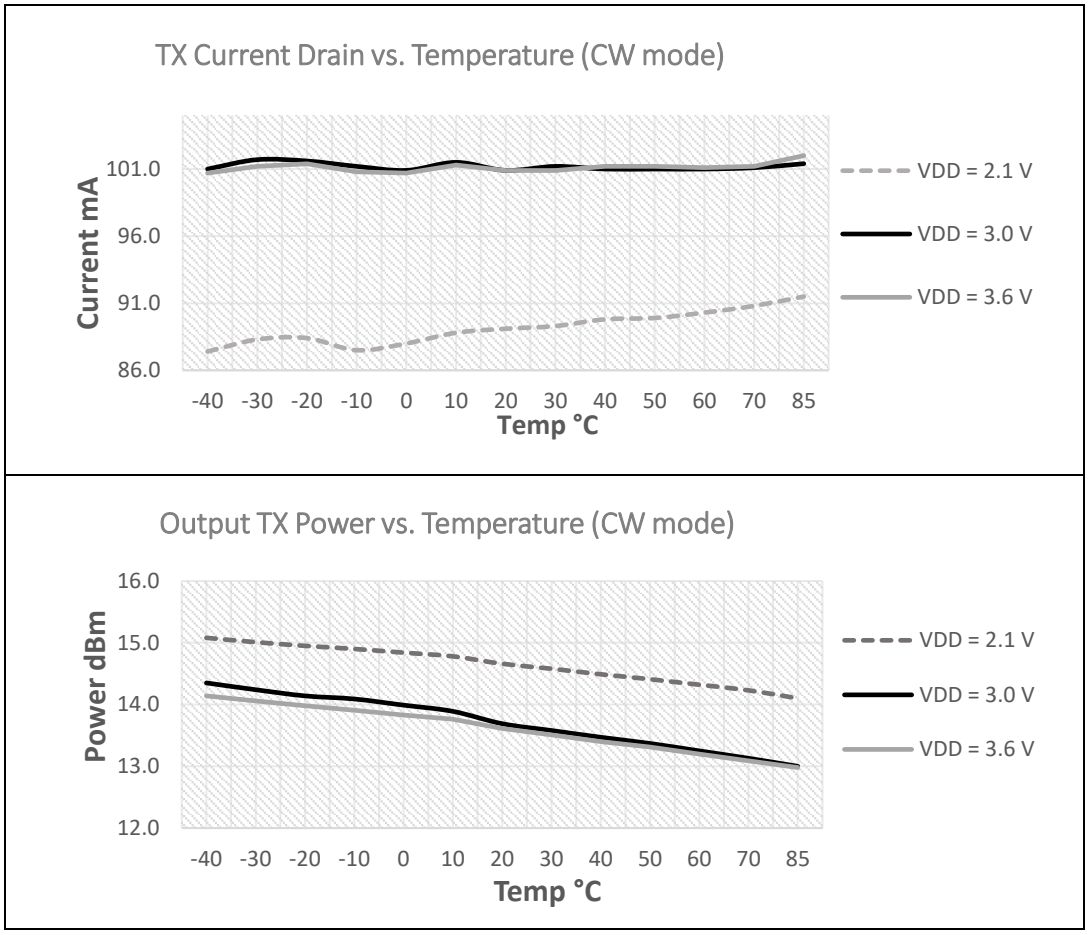
Parameter	Min.	Typ.	Max.	Unit	Notes
Current Drain (CW @14dBm)	-	103	-	mA	1,2
Operating frequency	868.0	-	868.6	MHz	
Occupied Bandwidth	-	125	-	kHz	
Operating Channel Width	-	200	-	kHz	
Maximum Output power (50 Ω load)	-	14	-	dBm	1,2,10
RF Output Impedance	-	50	-	Ω	
Input Logic Low	GND	-	0.05	V	
Input Logic High	VDD-0.2	-	VDD	V	

Notes:

1) VDD = 3.6 V.
2) All RF parameters measured with input (pin F1, ANT) connected to 50 Ω impedance signal source or load.
3) Pseudo random code NRZ, 2-FSK BER (bit error rate) = 0.1 % or better, 2-level FSK modulation without pre-filtering, Bit Rate = 4.8 Kbit/s, frequency deviation = 5 kHz, filter bandwidth = 20 kHz
4) LoRa® PER (packet error rate) = 1 %, packet of 64 bytes, preamble of 8 bytes, error correction code CR = 4/5, CRC on payload enabled, no reduced encoding, no implicit header.
5) Sensitivities given using highest LNA gain step.
6) Power consumption measured with -140 dBm signal and AGC ON.
7) Blocking immunity, ACR and co-channel rejection, given for a single tone interferer and referenced to sensitivity +6 dB, blocking tests performed with unmodulated signal measured as per ETSI 300 220-1.
8) Time by power-on to valid data reception.
9) Time by test signal at RF input to valid data reception.
10) In order to not exceed the maximum power permitted by the ETSI EN 300 220 regulation, choose an appropriate antenna system and power supply.

7. Temperature Range Curves

Note: All RF parameters measured with input (pad F1) connected to a 50 Ω impedance signal source or load.



8. Safety note

To meet safety requirements, the module must be powered by an external power source that meets limits of ES1 and PS1 according to IEC 62368-1.

9. Supporting documentation

Title	Description	Doc
Command Reference Manual	Description of commands for the LoRaWAN stack	32001506BEU_Com_Ref
Command Reference Manual	Description of commands for the LoRa Mipot stack	32001506CEU_Com_Ref
Command Reference Manual	Description of commands for the LoRa Modem stack	32001506DEU_Com_Ref
Command Reference Manual	Description of commands for the multi-stack module	32001506FEU_Com_Ref
Manufacturing Process Information for LGA MiP Series Modules	Packaging information, Tape& Reel Specification, Reflow soldering information	AN_MNF002
STM32WL55J data sheet	Overview of the MCU and its peripherals	DS13293 (from ST)
STM32WL55J reference manual	Detailed description of the MCU and its peripherals	RM0453 (from ST)

10. Ordering Information

Title	Description	DoC
32001506BEU	MiP-Lw-2C256N-EU	Europe
32001506CEU	MiP-LoMi-2C256N-EU	Europe
32001506DEU	MiP-LoMo-2C256N-EU	Europe
32001506FEU	MiP-LwMo-2C256N-EU	Europe

11. Regulatory Approvals

Doc	Title	Description
DoC	32001505BEU_DoC	Declaration of Conformity
DoI	32001506BEU_DoI	Declaration of Identity

12. Revision History

Revision	Date	Description
1.0	20.09.2022	Initial version