M24128-BW M24128-BR
M24256-BW M24256-BR

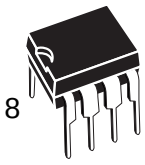
256 Kbit and 128 Kbit Serial I²C Bus EEPROM with three Chip Enable lines

Feature summary

- Compatible with I²C extended addressing
- Two-wire I²C serial interface supports 400kHz protocol
- Single supply voltage:
  - 2.5 to 5.5V for M24128-BW, M24256-BW
  - 1.8 to 5.5V for M24128-BR, M24256-BR
- Hardware write control
- Byte and Page Write (up to 64 Bytes)
- Random and Sequential Read modes
- Self-Timed programming cycle
- Automatic address incrementing
- Enhanced ESD/Latch-Up protection
- More than 1 million Write cycles
- More than 40-year data retention
- Packages
  - ECOPACK® (RoHS compliant)

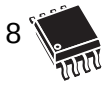
Table 1. Product List

Density	Part Number
128 Kbit	M24128-BW
	M24128-BR
256 Kbit	M24256-BW
	M24256-BR



PDIP8 (BN)

SO8 (MN)



SO8 (MW)
200 mil width

TSSOP8 (DW)
169 mil width

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1 Summary description

These I^2C-compatible electrically erasable programmable memory (EEPROM) devices are organized as 32K x 8 bits (M24256-BW and M24256-BR) and 16K x 8 bits (M24128-BW and M24128-BR).

I^2C uses a two-wire serial interface, comprising a bi-directional data line and a clock line. The devices carry a built-in 4-bit Device Type Identifier code (1010) in accordance with the I^2C bus definition.

The device behaves as a slave in the I^2C protocol, with all memory operations synchronized by the serial clock. Read and Write operations are initiated by a Start condition, generated by the bus master. The Start condition is followed by a Device Select Code and Read/$\overline{\text{Write}}$ bit ($\overline{\text{RW}}$) (as described in *Table 3*), terminated by an acknowledge bit.

When writing data to the memory, the device inserts an acknowledge bit during the 9th bit time, following the bus master's 8-bit transmission. When data is read by the bus master, the bus master acknowledges the receipt of the data byte in the same way. Data transfers are terminated by a Stop condition after an Ack for Write, and after a NoAck for Read.

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages.
ECOPACK® packages are Lead-free and RoHS compliant.

ECOPACK is an ST trademark. ECOPACK specifications are available at: *www.st.com*.

Figure 1. Logic Diagram

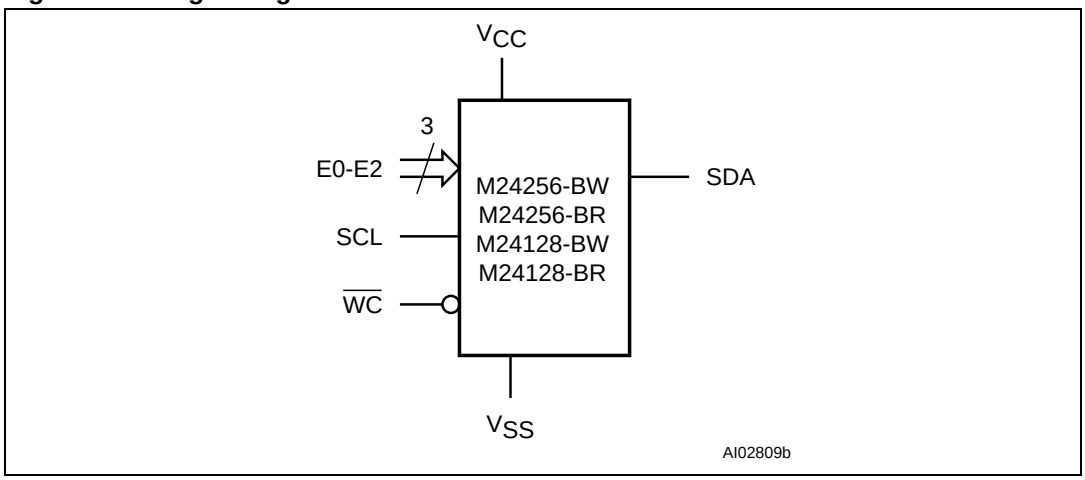
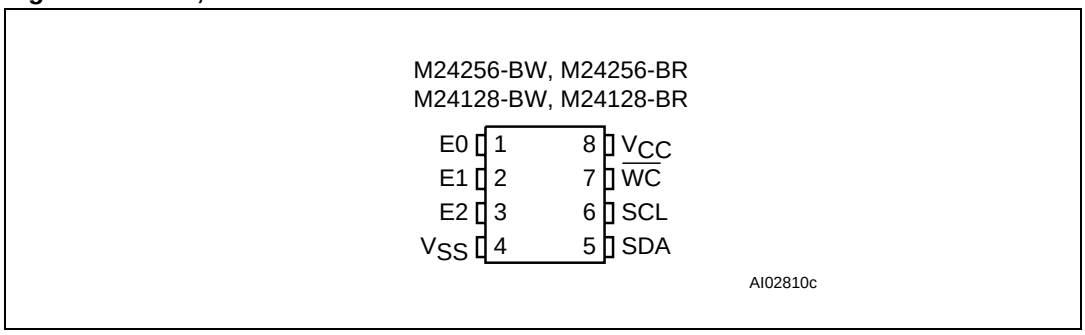


Table 2. Signal Names

E0, E1, E2	Chip Enable
SDA	Serial Data
SCL	Serial Clock
$\overline{\text{WC}}$	Write Control
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2. DIP, SO and TSSOP Connections



1. See *Section 7: Package mechanical* for package dimensions, and how to identify pin-1.

2 Signal description

2.1 Serial Clock (SCL)

This input signal is used to strobe all data in and out of the device. In applications where this signal is used by slave devices to synchronize the bus to a slower clock, the bus master must have an open drain output, and a pull-up resistor must be connected from Serial Clock (SCL) to V_{CC}. (*Figure 4* indicates how the value of the pull-up resistor can be calculated). In most applications, though, this method of synchronization is not employed, and so the pull-up resistor is not necessary, provided that the bus master has a push-pull (rather than open drain) output.

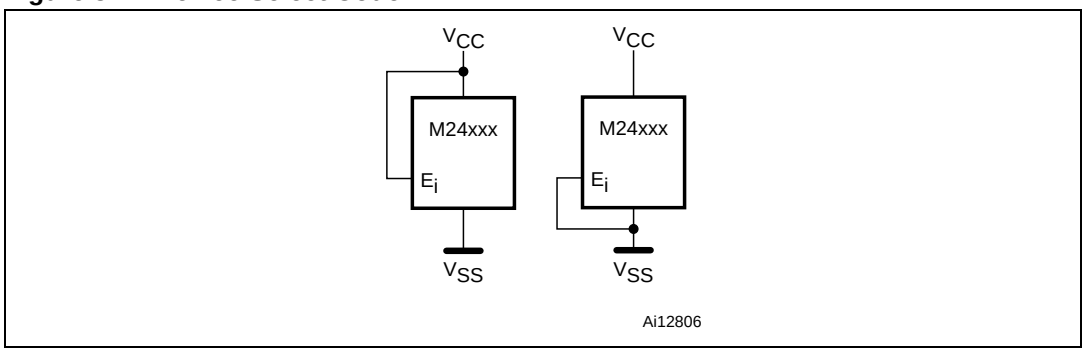
2.2 Serial Data (SDA)

This bi-directional signal is used to transfer data in or out of the device. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A pull up resistor must be connected from Serial Data (SDA) to V_{CC}. (*Figure 4* indicates how the value of the pull-up resistor can be calculated).

2.3 Chip Enable (E0, E1, E2)

These input signals are used to set the value that is to be looked for on the three least significant bits (b3, b2, b1) of the 7-bit Device Select Code. These inputs must be tied to V_{CC} or V_{SS}, to establish the Device Select Code as shown in *Figure 3*. When not connected (left floating), these inputs are read as Low (0,0,0).

Figure 3. Device Select Code



2.4 Write Control ($\overline{WC}$)

This input signal is useful for protecting the entire contents of the memory from inadvertent write operations. Write operations are disabled to the entire memory array when Write Control ($\overline{WC}$) is driven High. When unconnected, the signal is internally read as V_{IL}, and Write operations are allowed.

When Write Control ($\overline{WC}$) is driven High, Device Select and Address bytes are acknowledged, Data bytes are not acknowledged.

2.5 Supply voltage (V_{CC})

2.5.1 Operating supply voltage V_{CC}

Prior to selecting the memory and issuing instructions to it, a valid and stable V_{CC} voltage within the specified [V_{CC}(min), V_{CC}(max)] range must be applied (see *Table 8* and *Table 9*). In order to secure a stable DC supply voltage, it is recommended to decouple the V_{CC} line with a suitable capacitor (usually of the order of 10nF to 100nF) close to the V_{CC}/V_{SS} package pins.

This voltage must remain stable and valid until the end of the transmission of the instruction and, for a Write instruction, until the completion of the internal write cycle (t_W).

2.5.2 Internal device reset

In order to prevent inadvertent Write operations during Power-up, a Power On Reset (POR) circuit is included. At Power-up (continuous rise of V_{CC}), the device does not respond to any instruction until V_{CC} has reached the Power On Reset threshold voltage (this threshold is lower than the minimum V_{CC} operating voltage defined in *Table 8* and *Table 9*).

When V_{CC} has passed the POR threshold, the device is reset and is in Standby Power mode.

2.5.3 Power-down

At Power-down (continuous decrease of V_{CC}), as soon as V_{CC} drops from the normal operating voltage to below the Power On Reset threshold voltage, the device stops responding to any instruction sent to it.

During Power-down, the device must be deselected and in the Standby Power mode (that is there should be no internal Write cycle in progress).

Figure 4. Maximum R_P Value versus Bus Parasitic Capacitance (C) for an I^2C Bus

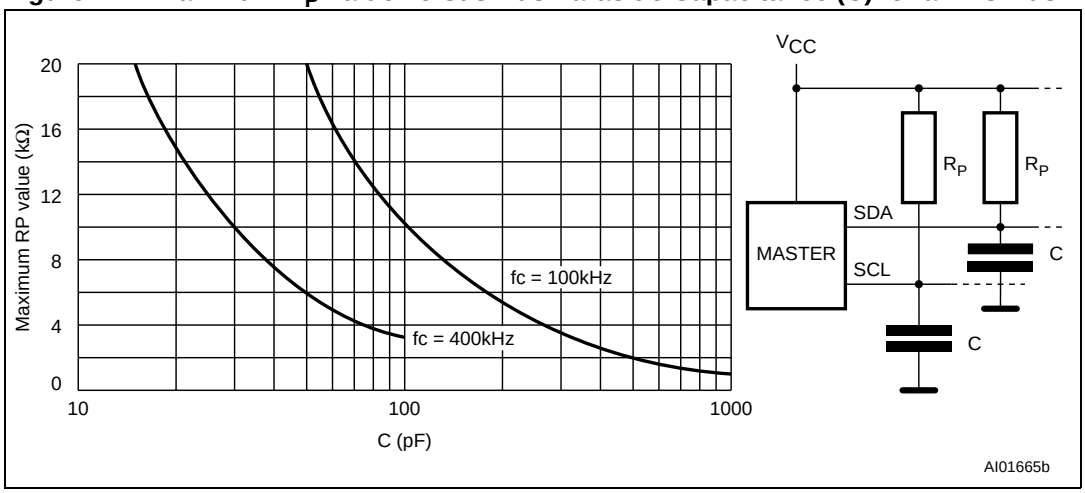


Figure 5. I^2C Bus Protocol

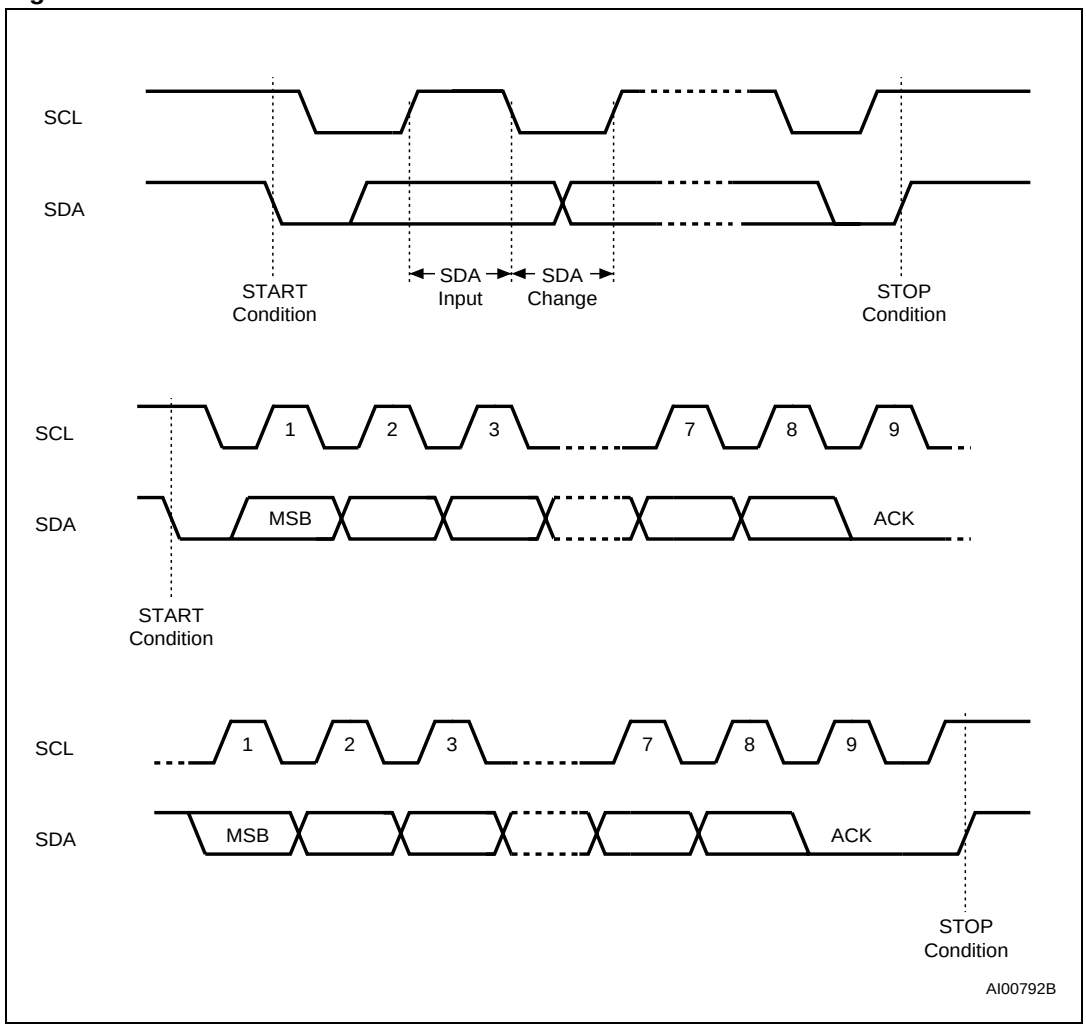


Table 3. Device Select Code

	Device Type Identifier(1)				Chip Enable Address(2)			RW
	b7	b6	b5	b4	b3	b2	b1	b0
Device Select Code	1	0	1	0	E2	E1	E0	RW

1. The most significant bit, b7, is sent first.
2. E0, E1 and E2 are compared against the respective external pins on the memory device.

Table 4. Most Significant address Byte

b15	b14	b13	b12	b11	b10	b9	b8

Table 5. Least Significant address Byte

b7	b6	b5	b4	b3	b2	b1	b0

3 Device operation

The device supports the I^2C protocol. This is summarized in *Figure 5*. Any device that sends data on to the bus is defined to be a transmitter, and any device that reads the data to be a receiver. The device that controls the data transfer is known as the bus master, and the other as the slave device. A data transfer can only be initiated by the bus master, which will also provide the serial clock for synchronization. The M24xxx-B device is always a slave in all communication.

3.1 Start condition

Start is identified by a falling edge of Serial Data (SDA) while Serial Clock (SCL) is stable in the High state. A Start condition must precede any data transfer command. The device continuously monitors (except during a Write cycle) Serial Data (SDA) and Serial Clock (SCL) for a Start condition, and will not respond unless one is given.

3.2 Stop condition

Stop is identified by a rising edge of Serial Data (SDA) while Serial Clock (SCL) is stable and driven High. A Stop condition terminates communication between the device and the bus master. A Read command that is followed by NoAck can be followed by a Stop condition to force the device into the Stand-by mode. A Stop condition at the end of a Write command triggers the internal EEPROM Write cycle.

3.3 Acknowledge bit (ACK)

The acknowledge bit is used to indicate a successful byte transfer. The bus transmitter, whether it be bus master or slave device, releases Serial Data (SDA) after sending eight bits of data. During the 9^{th} clock pulse period, the receiver pulls Serial Data (SDA) Low to acknowledge the receipt of the eight data bits.

3.4 Data input

During data input, the device samples Serial Data (SDA) on the rising edge of Serial Clock (SCL). For correct device operation, Serial Data (SDA) must be stable during the rising edge of Serial Clock (SCL), and the Serial Data (SDA) signal must change *only* when Serial Clock (SCL) is driven Low.

3.5 Memory addressing

To start communication between the bus master and the slave device, the bus master must initiate a Start condition. Following this, the bus master sends the Device Select Code, shown in *Table 3* (on Serial Data (SDA), most significant bit first).

The Device Select Code consists of a 4-bit Device Type Identifier, and a 3-bit Chip Enable “Address” (E2, E1, E0). To address the memory array, the 4-bit Device Type Identifier is 1010b.

Up to eight memory devices can be connected on a single I^2C bus. Each one is given a unique 3-bit code on the Chip Enable (E0, E1, E2) inputs. When the Device Select Code is received, the device only responds if the Chip Enable Address is the same as the value on the Chip Enable (E0, E1, E2) inputs.

The 8th bit is the Read/$\overline{\text{Write}}$ bit ($\overline{\text{RW}}$). This bit is set to 1 for Read and 0 for Write operations.

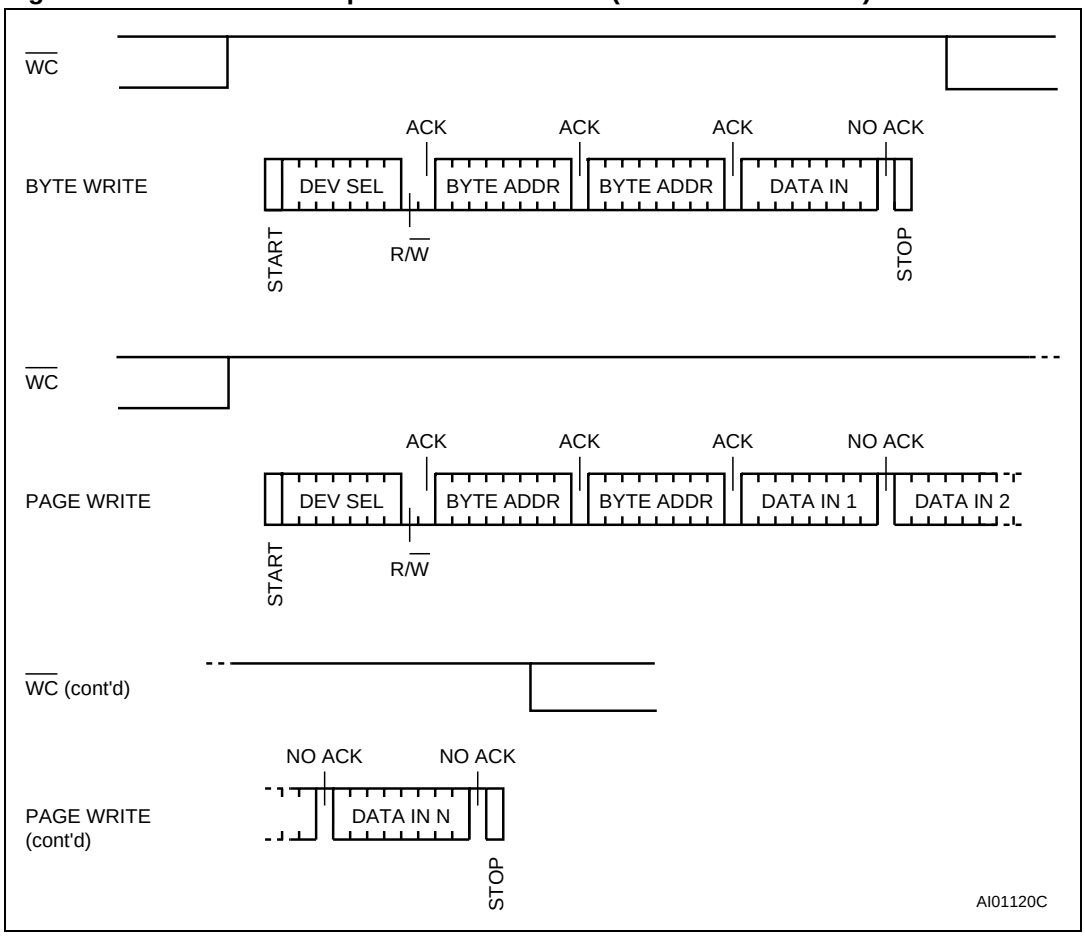
If a match occurs on the Device Select code, the corresponding device gives an acknowledgment on Serial Data (SDA) during the 9th bit time. If the device does not match the Device Select code, it deselects itself from the bus, and goes into Stand-by mode.

Table 6. Operating modes

Mode	$\overline{\text{RW}}$ bit	$\overline{\text{WC}}$(1)	Bytes	Initial Sequence
Current Address Read	1	X	1	START, Device Select, $\overline{\text{RW}}$ = 1
Random Address Read	0	X	1	START, Device Select, $\overline{\text{RW}}$ = 0, Address
	1	X		reSTART, Device Select, $\overline{\text{RW}}$ = 1
Sequential Read	1	X	≥ 1	Similar to Current or Random Address Read
Byte Write	0	V_{IL}	1	START, Device Select, $\overline{\text{RW}}$ = 0
Page Write	0	V_{IL}	≤64	START, Device Select, $\overline{\text{RW}}$ = 0

1. X = V_{IH} or V_{IL}.

Figure 6. Write mode sequences with $\overline{WC}$ = 1 (data write inhibited)



3.6 Write operations

Following a Start condition the bus master sends a Device Select Code with the R/$\overline{W}$ bit (R$\overline{W}$) reset to 0. The device acknowledges this, as shown in *Figure 7*, and waits for two address bytes. The device responds to each address byte with an acknowledge bit, and then waits for the data byte.

Writing to the memory may be inhibited if Write Control ($\overline{WC}$) is driven High. Any Write instruction with Write Control ($\overline{WC}$) driven High (during a period of time from the Start condition until the end of the two address bytes) will not modify the memory contents, and the accompanying data bytes are *not* acknowledged, as shown in *Figure 6*.

Each data byte in the memory has a 16-bit (two byte wide) address. The Most Significant Byte (*Table 4*) is sent first, followed by the Least Significant Byte (*Table 5*). Bits b15 to b0 form the address of the byte in memory.

When the bus master generates a Stop condition immediately after the Ack bit (in the "10^{th} bit" time slot), either at the end of a Byte Write or a Page Write, the internal memory Write cycle is triggered. A Stop condition at any other time slot does not trigger the internal Write cycle.

After the Stop condition, the delay t_W, and the successful completion of a Write operation, the device's internal address counter is incremented automatically, to point to the next byte address after the last one that was modified.

During the internal Write cycle, Serial Data (SDA) is disabled internally, and the device does not respond to any requests.

3.7 Byte Write

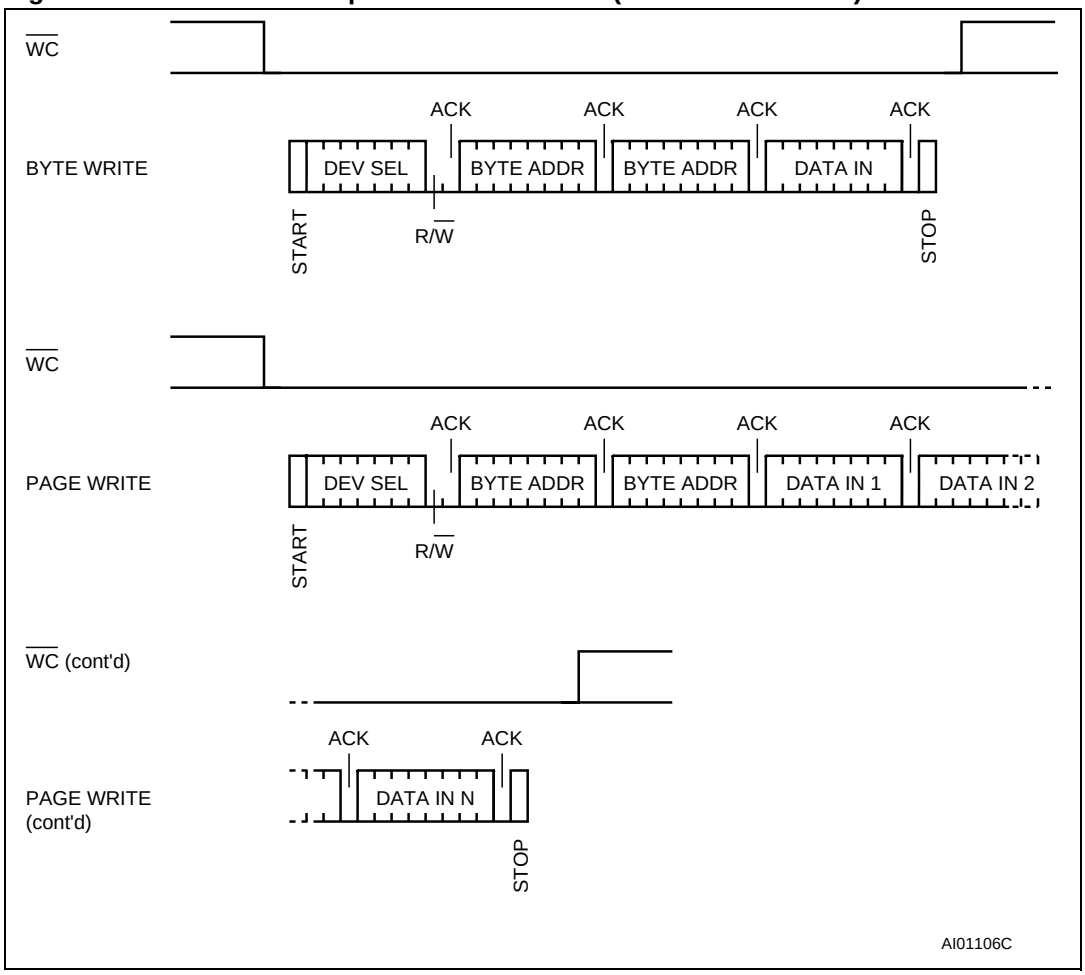
After the Device Select code and the address bytes, the bus master sends one data byte. If the addressed location is Write-protected, by Write Control ($\overline{WC}$) being driven High, the device replies with NoAck, and the location is not modified. If, instead, the addressed location is not Write-protected, the device replies with Ack. The bus master terminates the transfer by generating a Stop condition, as shown in *Figure 7*.

3.8 Page Write

The Page Write mode allows up to 64 bytes to be written in a single Write cycle, provided that they are all located in the same 'row' in the memory: that is, the most significant memory address bits, b15-b6, are the same. If more bytes are sent than will fit up to the end of the row, a condition known as 'roll-over' occurs. This should be avoided, as data starts to become overwritten in an implementation dependent way.

The bus master sends from 1 to 64 bytes of data, each of which is acknowledged by the device if Write Control ($\overline{WC}$) is Low. If Write Control ($\overline{WC}$) is High, the contents of the addressed memory location are not modified, and each data byte is followed by a NoAck. After each byte is transferred, the internal byte address counter (the 6 least significant address bits only) is incremented. The transfer is terminated by the bus master generating a Stop condition.

Figure 7. Write Mode Sequences with $\overline{WC}$ = 0 (data write enabled)



3.9 ECC (Error Correction Code) and Write cycling

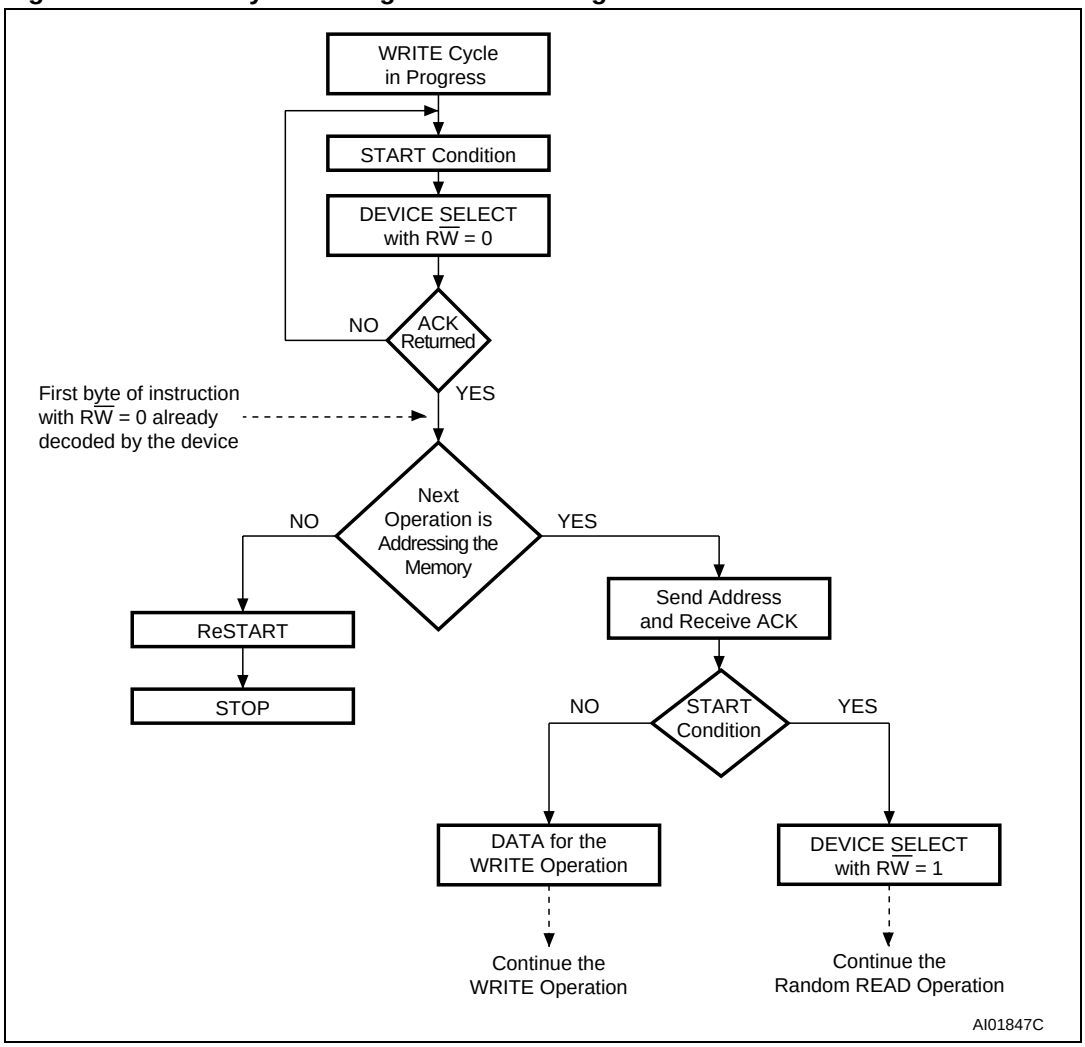
The M24256-BW and M24256-BR devices offer an ECC (Error Correction Code) logic which compares each 4-Byte packet with its associated ECC Word (6 EEPROM bits). As a result, if a single bit out of 4 Bytes of data happens to be erroneous during a Read operation, the ECC detects it and replaces it by the correct value. The read reliability is therefore much improved by the use of this feature.

Note however that even if a single Byte has to be written, 4 Bytes are internally modified (plus the ECC Word), that is, the addressed Byte is cycled together with the three other Bytes making up the packet. It is therefore recommended to write by packets of 4 Bytes in order to benefit from the larger amount of Write cycles.

The M24256-BW and M24256-BR devices are qualified as 1 million (1,000,000) Write cycles, using a cycling routine that writes to the device by multiples of 4-Byte packets.

The M24128-BW and M24128-BR devices do not offer the ECC logic and are qualified as 1 million (1,000,000) Write cycles.

Figure 8. Write Cycle Polling Flowchart using ACK



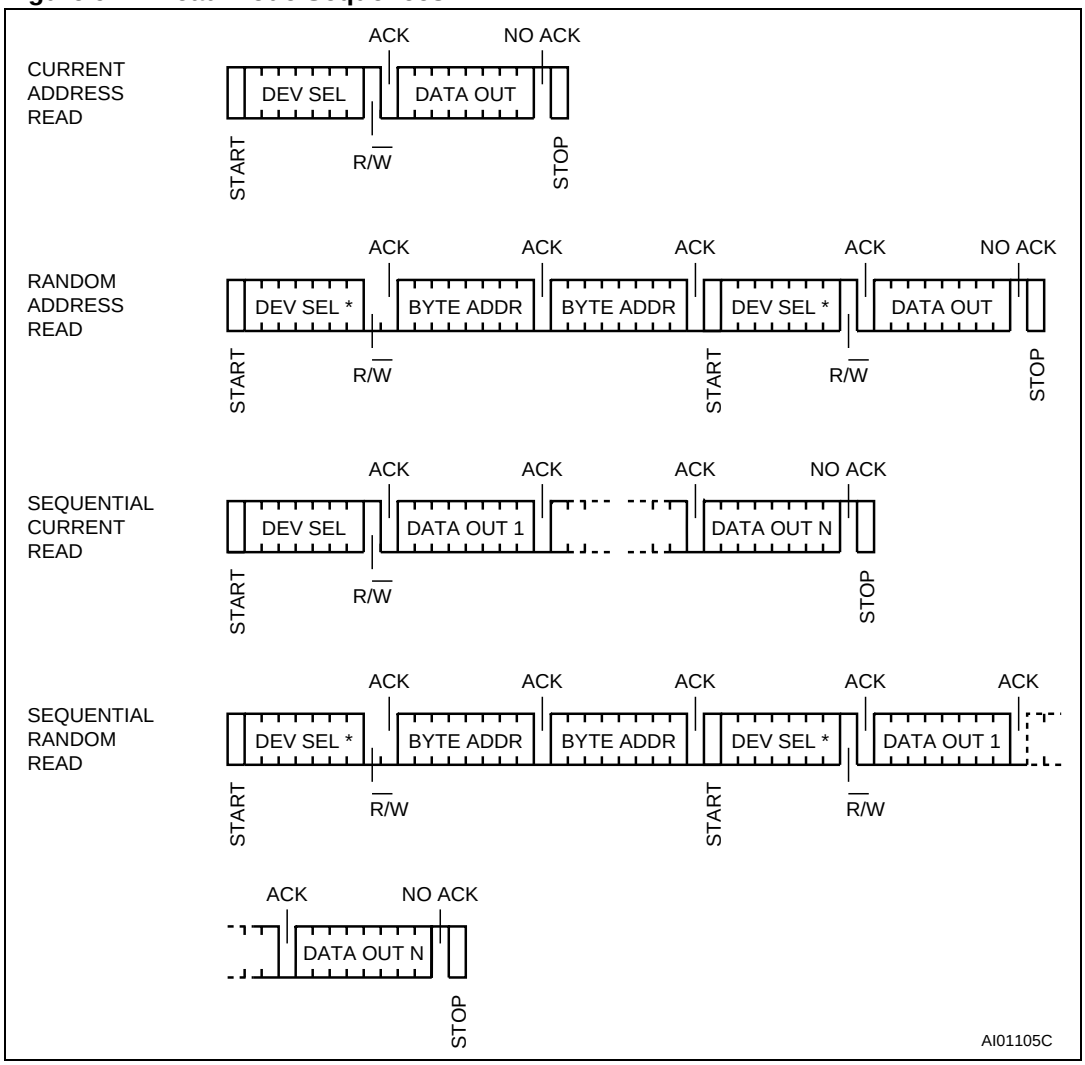
3.10 Minimizing system delays by polling on ACK

During the internal Write cycle, the device disconnects itself from the bus, and writes a copy of the data from its internal latches to the memory cells. The maximum Write time (t_w) is shown in *Table 14* and *Table 15*, but the typical time is shorter. To make use of this, a polling sequence can be used by the bus master.

The sequence, as shown in *Figure 8*, is:

- Initial condition: a Write cycle is in progress.
- Step 1: the bus master issues a Start condition followed by a Device Select Code (the first byte of the new instruction).
- Step 2: if the device is busy with the internal Write cycle, no Ack will be returned and the bus master goes back to Step 1. If the device has terminated the internal Write cycle, it responds with an Ack, indicating that the device is ready to receive the second part of the instruction (the first byte of this instruction having been sent during Step 1).

Figure 9. Read Mode Sequences



1. The seven most significant bits of the Device Select Code of a Random Read (in the 1st and 4th bytes) must be identical.

3.11 Read Operations

Read operations are performed independently of the state of the Write Control ($\overline{WC}$) signal.

After the successful completion of a Read operation, the device's internal address counter is incremented by one, to point to the next byte address.

3.12 Random Address Read

A dummy Write is first performed to load the address into this address counter (as shown in *Figure 9*) but *without* sending a Stop condition. Then, the bus master sends another Start condition, and repeats the Device Select Code, with the R$\overline{W}$ bit set to 1. The device acknowledges this, and outputs the contents of the addressed byte. The bus master must *not* acknowledge the byte, and terminates the transfer with a Stop condition.

3.13 Current Address Read

For the Current Address Read operation, following a Start condition, the bus master only sends a Device Select Code with the R/$\overline{W}$ bit set to 1. The device acknowledges this, and outputs the byte addressed by the internal address counter. The counter is then incremented. The bus master terminates the transfer with a Stop condition, as shown in *Figure 9*, *without* acknowledging the byte.

3.14 Sequential Read

This operation can be used after a Current Address Read or a Random Address Read. The bus master *does* acknowledge the data byte output, and sends additional clock pulses so that the device continues to output the next byte in sequence. To terminate the stream of bytes, the bus master must *not* acknowledge the last byte, and *must* generate a Stop condition, as shown in *Figure 9*.

The output data comes from consecutive addresses, with the internal address counter automatically incremented after each byte output. After the last memory address, the address counter 'rolls-over', and the device continues to output data from memory address 00h.

3.15 Acknowledge in Read Mode

For all Read commands, the device waits, after each byte read, for an acknowledgment during the 9th bit time. If the bus master does not drive Serial Data (SDA) Low during this time, the device terminates the data transfer and switches to its Stand-by mode.

4 Initial delivery state

The device is delivered with all the memory array bits set to 1 (each byte contains FFh).

5 Maximum rating

Stressing the device outside the ratings listed in *Table 7* may cause permanent damage to the device. These are stress ratings only, and operation of the device at these, or any other conditions outside those indicated in the Operating sections of this specification, is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 7. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
T_A	Ambient Operating Temperature	–40	130	°C
T_{STG}	Storage Temperature	–65	150	°C
T_{LEAD}	Lead Temperature during Soldering	see note (1)		°C
	PDIP-Specific Lead Temperature during Soldering		260(2)	°C
V_{IO}	Input or Output range	–0.50	6.5	V
V_{CC}	Supply Voltage	–0.50	6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model)(3)	–3000	3000	V

1. Compliant with JEDEC Std J-STD-020C (for small body, Sn-Pb or Pb assembly), the ST ECOPACK® 7191395 specification, and the European directive on Restrictions on Hazardous Substances (RoHS) 2002/95/EU.
2. T_{LEAD} max must not be applied for more than 10s.
3. AEC-Q100-002 (compliant with JEDEC Std JESD22-A114A, C1=100pF, R1=1500Ω, R2=500Ω)

6 DC and AC parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC Characteristic tables that follow are derived from tests performed under the Measurement Conditions summarized in the relevant tables. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 8. Operating conditions (M24128-BW, M24256-BW)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	2.5	5.5	V
T_A	Ambient Operating Temperature	–40	85	°C

Table 9. Operating conditions (M24128-BR, M24256-BR)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	1.8	5.5	V
T_A	Ambient Operating Temperature	–40	85	°C

Table 10. AC measurement conditions

Symbol	Parameter	Min.	Max.	Unit
C_L	Load Capacitance	100		pF
	Input Rise and Fall Times		50	ns
	Input Levels	$0.2V_{CC}$ to $0.8V_{CC}$		V
	Input and Output Timing Reference Levels	$0.3V_{CC}$ to $0.7V_{CC}$		V

Figure 10. AC measurement I/O waveform

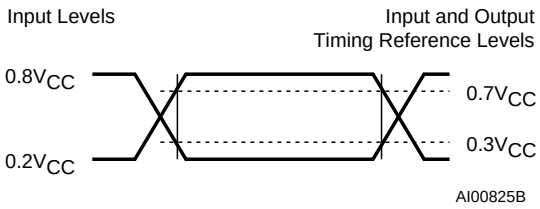


Table 11. Input parameters

Symbol	Parameter(1),(2)	Test Condition	Min.	Max.	Unit
C_{IN}	Input Capacitance (SDA)			8	pF
C_{IN}	Input Capacitance (other pins)			6	pF
Z_L	Input Impedance ($\overline{WC}$)	$V_{IN} < 0.3\ V_{CC}$	30		kΩ
Z_H		$V_{IN} > 0.7V_{CC}$	500		kΩ
t_{NS}	Pulse width ignored (Input Filter on SCL and SDA)	Single glitch		100	ns

1. T_A = 25°C, f = 400kHz
2. Sampled only, not 100% tested.

Table 12. DC characteristics (M24128-BW, M24256-BW)

Symbol	Parameter	Test Condition (in addition to those in *Table 8*)	Min.	Max.	Unit
I_{LI}	Input Leakage Current (SCL, SDA)	$V_{IN} = V_{SS}$ or V_{CC} device in Stand-by mode		± 2	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ or V_{CC}, SDA in Hi-Z		± 2	µA
I_{CC}	Supply Current (Read)	V_{CC} =2.5V, f_c=400kHz (rise/fall time < 30ns)		1	mA
		V_{CC} = 5V, f_c=400kHz (rise/fall time < 30ns)		2	mA
I_{CC0}	Supply Current (Write)	During t_W, 2.5V < V_{CC} < 5.5V		5(1)	mA
I_{CC1}	Standby Supply Current	$V_{IN} = V_{SS}$ or V_{CC}, 2.5V < V_{CC} < 5.5V		10	µA
V_{IL}	Input Low Voltage (SCL, SDA)		–0.45	$0.3V_{CC}$	V
V_{IH}	Input High Voltage (SCL, SDA, $\overline{WC}$)		$0.7V_{CC}$	V_{CC}+1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA, V_{CC} = 2.5 V		0.4	V

1. Characterized value, not tested in production.

Table 13. DC Characteristics (M24128-BR, M24256-BR)

Symbol	Parameter	Test Condition (in addition to those in *Table 9*)	Min.	Max.	Unit
I_{LI}	Input Leakage Current (SCL, SDA)	$V_{IN} = V_{SS}$ or V_{CC} device in Stand-by mode		± 2	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ or V_{CC}, SDA in Hi-Z		± 2	µA
I_{CC}	Supply Current (Read)	V_{CC} =1.8V, f_c=100kHz (rise/fall time < 30ns)		0.8	mA
I_{CC0}	Supply Current (Write)	During t_W, 1.8V < V_{CC} < 5.5V		5(1)	mA
I_{CC1}	Standby Supply Current	$V_{IN} = V_{SS}$ or V_{CC}, 1.8V < V_{CC} < 5.5V		5	µA
V_{IL}	Input Low Voltage (SCL, SDA)		–0.45	0.3 V_{CC}	V
	Input Low Voltage (E2, E1, E0, $\overline{WC}$)		–0.45	0.5	V
V_{IH}	Input High Voltage (E2, E1, E0, SCL, SDA, $\overline{WC}$)		0.7V_{CC}	V_{CC}+1	V
V_{OL}	Output Low Voltage	I_{OL} = 0.7 mA, V_{CC} = 1.8 V		0.2	V

1. Characterized value, not tested in production.

Table 14. AC characteristics (M24128-BW, M24256-BW)

Test conditions specified in *Table 8*					
Symbol	**Alt.**	**Parameter**	**Min.**	**Max.**	**Unit**
f_C	f_{SCL}	Clock Frequency		400	kHz
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	600		ns
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	1300		ns
t_{CH1CH2}	t_R	Clock Rise Time		300	ns
t_{CL1CL2}	t_F	Clock Fall Time		300	ns
t_{DH1DH2}(1)	t_R	SDA Rise Time	20	300	ns
t_{DL1DL2}(1)	t_F	SDA Fall Time	20	300	ns
t_{DXCX}	$t_{SU:DAT}$	Data In Set Up Time	100		ns
t_{CLDX}	$t_{HD:DAT}$	Data In Hold Time	0		ns
t_{CLQX}	t_{DH}	Data Out Hold Time	200		ns
t_{CLQV}(2)	t_{AA}	Clock Low to Next Data Valid (Access Time)	200	900	ns
t_{CHDX}(3)	$t_{SU:STA}$	Start Condition Set Up Time	600		ns
t_{DLCL}	$t_{HD:STA}$	Start Condition Hold Time	600		ns
t_{CHDH}	$t_{SU:STO}$	Stop Condition Set Up Time	600		ns
t_{DHDL}	t_{BUF}	Time between Stop Condition and Next Start Condition	1300		ns
t_W	t_{WR}	Write Time		5	ms

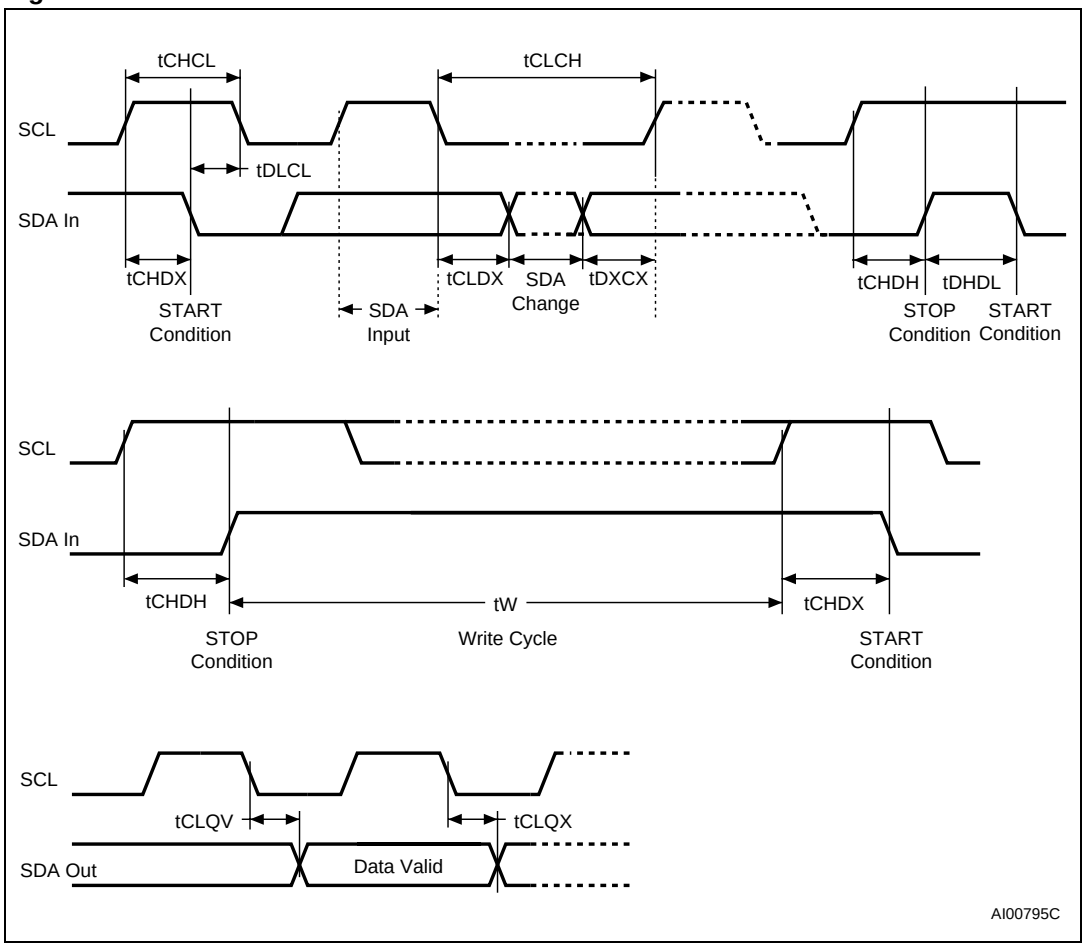
1. Sampled only, not 100% tested.
2. To avoid spurious START and STOP conditions, a minimum delay is placed between SCL=1 and the falling or rising edge of SDA.
3. For a reSTART condition, or following a Write cycle.

Table 15. AC characteristics (M24128-BR, M24256-BR)

Test conditions specified in *Table 9*					
Symbol	**Alt.**	**Parameter**	**Min.**	**Max.**	**Unit**
f_C	f_{SCL}	Clock Frequency		400	kHz
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	600		ns
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	1300		ns
t_{CH1CH2}	t_R	Clock Rise Time		300	ns
t_{CL1CL2}	t_F	Clock Fall Time		300	ns
t_{DH1DH2}(1)	t_R	SDA Rise Time	20	300	ns
t_{DL1DL2}(1)	t_F	SDA Fall Time	20	300	ns
t_{DXCX}	$t_{SU:DAT}$	Data In Set Up Time	100		ns
t_{CLDX}	$t_{HD:DAT}$	Data In Hold Time	0		ns
t_{CLQX}	t_{DH}	Data Out Hold Time	200		ns
t_{CLQV}(2)	t_{AA}	Clock Low to Next Data Valid (Access Time)	200	900	ns
t_{CHDX}(3)	$t_{SU:STA}$	Start Condition Set Up Time	600		ns
t_{DLCL}	$t_{HD:STA}$	Start Condition Hold Time	600		ns
t_{CHDH}	$t_{SU:STO}$	Stop Condition Set Up Time	600		ns
t_{DHDL}	t_{BUF}	Time between Stop Condition and Next Start Condition	1300		ns
t_W	t_{WR}	Write Time		10	ms

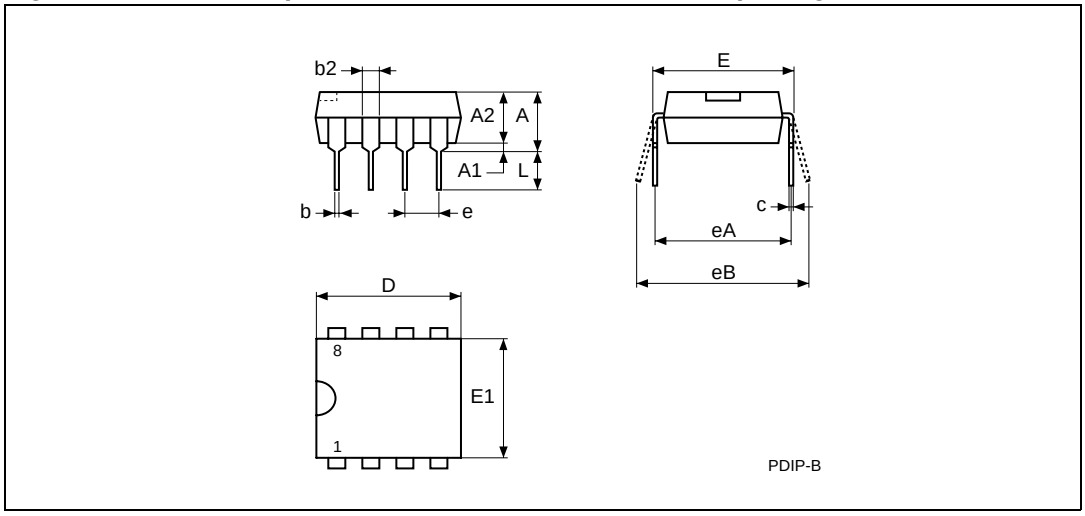
1. Sampled only, not 100% tested.
2. To avoid spurious START and STOP conditions, a minimum delay is placed between SCL=1 and the falling or rising edge of SDA.
3. For a reSTART condition, or following a Write cycle.

Figure 11. AC waveforms



7 Package mechanical

Figure 12. PDIP8 – 8 pin Plastic DIP, 0.25mm lead frame, package outline

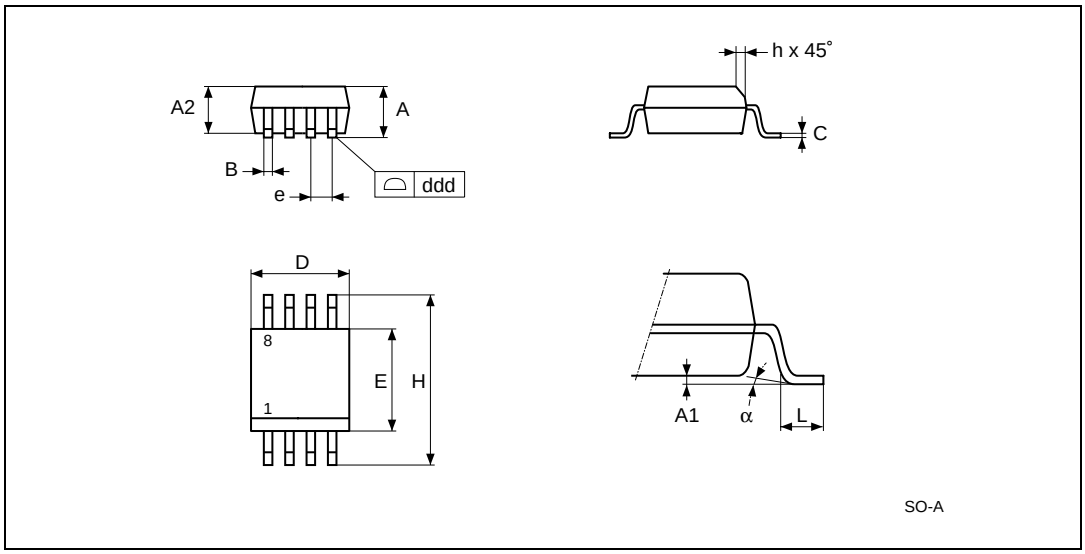


1. Drawing is not to scale.

Table 16. PDIP8 – 8 pin Plastic DIP, 0.25mm lead frame, package mechanical data

Symbol	millimeters			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A			5.33			0.210
A1		0.38			0.015	
A2	3.30	2.92	4.95	0.130	0.115	0.195
b	0.46	0.36	0.56	0.018	0.014	0.022
b2	1.52	1.14	1.78	0.060	0.045	0.070
c	0.25	0.20	0.36	0.010	0.008	0.014
D	9.27	9.02	10.16	0.365	0.355	0.400
E	7.87	7.62	8.26	0.310	0.300	0.325
E1	6.35	6.10	7.11	0.250	0.240	0.280
e	2.54	–	–	0.100	–	–
eA	7.62	–	–	0.300	–	–
eB			10.92			0.430
L	3.30	2.92	3.81	0.130	0.115	0.150

Figure 13. SO8 narrow – 8 lead Plastic Small Outline, 150 mils body width, package outline

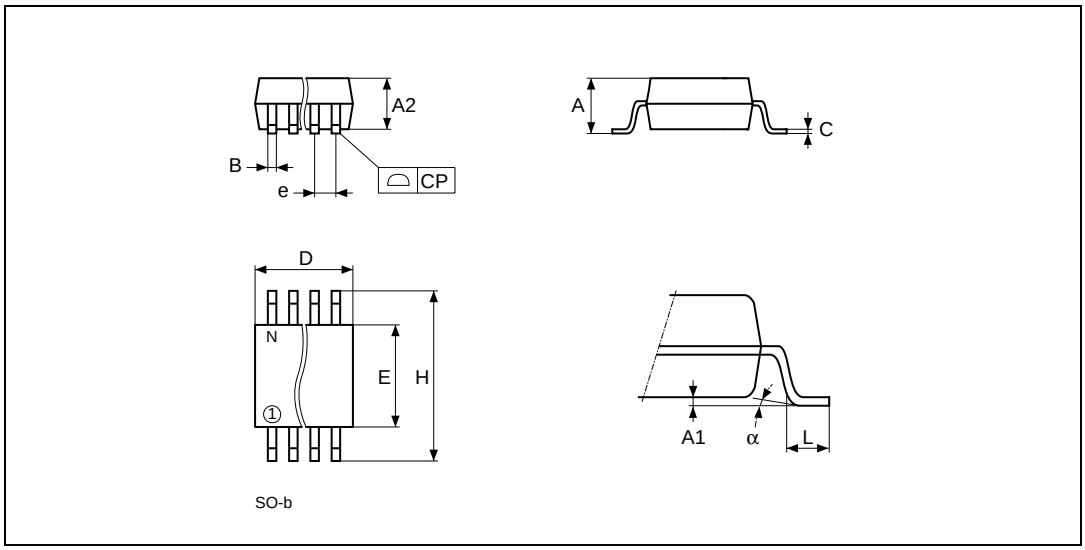


1. Drawing is not to scale.

Table 17. SO8 narrow – 8 lead Plastic Small Outline, 150 mils body width, package mechanical data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
A2		1.10	1.65		0.043	0.065
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
ddd			0.10			0.004
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N	8			8		

Figure 14. SO8 wide – 8 lead Plastic Small Outline, 200 mils body width, Package Outline

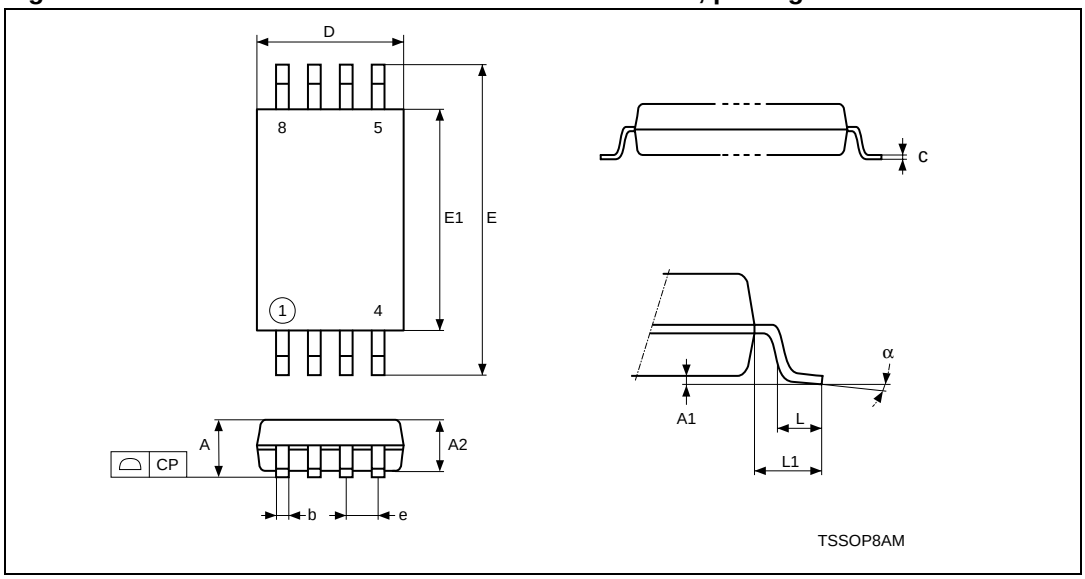


1. Drawing is not to scale.
2. The '1' that appears in the top view of the package shows the position of pin 1 and the 'N' indicates the total number of pins.

Table 18. SO8 wide – 8 lead Plastic Small Outline, 200 mils body width, package mechanical data

Symbol	millimeters			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A			2.03			0.080
A1		0.10	0.25		0.004	0.010
A2			1.78			0.070
B		0.35	0.45		0.014	0.018
C	0.20	–	–	0.008	–	–
D		5.15	5.35		0.203	0.211
E		5.20	5.40		0.205	0.213
e	1.27	–	–	0.050	–	–
H		7.70	8.10		0.303	0.319
L		0.50	0.80		0.020	0.031
α		0°	10°		0°	10°
N	8			8		
CP			0.10			0.004

Figure 15. TSSOP8 – 8 lead Thin Shrink Small Outline, package outline



1. Drawing is not to scale.

Table 19. TSSOP8 – 8 lead Thin Shrink Small Outline, package mechanical data

Symbol	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A			1.200			0.0472
A1		0.050	0.150		0.0020	0.0059
A2	1.000	0.800	1.050	0.0394	0.0315	0.0413
b		0.190	0.300		0.0075	0.0118
c		0.090	0.200		0.0035	0.0079
CP			0.100			0.0039
D	3.000	2.900	3.100	0.1181	0.1142	0.1220
e	0.650	–	–	0.0256	–	–
E	6.400	6.200	6.600	0.2520	0.2441	0.2598
E1	4.400	4.300	4.500	0.1732	0.1693	0.1772
L	0.600	0.450	0.750	0.0236	0.0177	0.0295
L1	1.000			0.0394		
α		0°	8°		0°	8°

8 Part numbering

Table 20. Ordering Information Scheme

Example: M24256 – B W MN 6 T P

Device Type

M24 = I^2C serial access EEPROM

Device Function

256 = 256 Kbit (32K x 8)

128 = 128 Kbit (16K x 8)

Operating Voltage

W = V_{CC} = 2.5 to 5.5V

R = V_{CC} = 1.8 to 5.5V

Package

BN = PDIP8

MN = SO8 (150 mil width)

MW = SO8 (200 mil width)

DW = TSSOP8 (169 mil width)

Device Grade

6 = Industrial temperature range, –40 to 85 °C.
Device tested with standard test flow

Option

blank = Standard Packing

T = Tape and Reel Packing

Plating Technology

blank = Standard SnPb plating

P or G = ECOPACK® (RoHS compliant)

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST Sales Office.

The category of Second-Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

9 Revision history

Table 21. Document revision history

Date	Revision	Description of Revision
28-Dec-1999	2.1	TSSOP8 package added
24-Feb-2000	2.2	E2, E1, E0 must be tied to Vcc or Vss Low Pass Filter Time Constant changed to Glitch Filter
22-Nov-2000	2.3	-V voltage range added
30-Jan-2001	2.4	-V voltage range changed to 2.5V to 3.6V Lead Soldering Temperature in the Absolute Maximum Ratings table amended Write Cycle Polling Flow Chart using ACK illustration updated. SO8(wide) package added References to PSDIP8 changed to PDIP8, and Package Mechanical data updated
01-Jun-2001	2.5	-R voltage range added. Package mechanical data updated for TSSOP8 and TSSOP14 packages according to JEDEC\MO-153 Document promoted from “Preliminary Data” to “Full Data Sheet”
16-Oct-2001	2.6	TSSOP14 package removed Absolute Max Ratings and DC characteristics updated for M24256-BV
09-Nov-2001	2.7	Specification of Test Condition for Leakage Currents in the DC Characteristics table improved
21-Mar-2002	2.8	1 million Erase/Write cycle endurance for M24256-B and M24256-BW products with process letter "V"
18-Oct-2002	3.0	Document reformatted. Parameters changed are: 1 million Erase/Write cycle endurance and 5 ms write time for M24128-B and M24128-BW products with process letter "B".
20-Nov-2002	3.1	Superfluous (and incorrectly present) 100kHz AC Characteristics table for M24256-BR removed.
02-Jun-2003	3.2	Initial delivery state specified. -R and -S ranges are no longer Preliminary Data. Package mechanical data for unavailable package removed.
22-Oct-2003	4.0	Table of contents, and Pb-free options added. Minor wording changes in Summary Description, Power-On Reset, Memory Addressing, Write Operations, Read Operations. V_{IL}(min) improved to -0.45V.
16-Apr-2004	5.0	SO8W package added. Absolute Maximum Ratings for V_{IO}(min) and V_{CC}(min) changed. Soldering temperature information clarified for RoHS compliant devices.

Table 21. Document revision history (continued)

Date	Revision	Description of Revision
13-Jun-2005	6.0	M24xxx-B, M24xxx-BV and M24xxx-BS removed from the datasheet. Product List summary table added. *Power On Reset* paragraph updated. *Figure 4: Maximum RP Value versus Bus Parasitic Capacitance (C) for an I2C Bus* updated. Z_L and Z_H definition changed. I_{CC} and I_{CC1} updated in *Table 12: DC characteristics (M24128-BW, M24256-BW)*. Device Grade information further clarified to *Table 20: Ordering Information Scheme*.
04-Apr-2006	7	*Power On Reset* paragraph replaced by *Section 2.5: Supply voltage (VCC)*. *Figure 3: Device Select Code* added. *Section 3.9: ECC (Error Correction Code) and Write cycling* added. I_{CC0} added and I_{CC1} specified over the whole voltage range in *Table 12* and *Table 13*. SO8 narrow package specifications updated (see *Figure 13* and *Table 17*). Packages are ECOPACK® compliant. Small text changes.

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