

SN54HCT574, SN74HCT574 OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCLS177E – MARCH 1984 – REVISED AUGUST 2003

- Operating Voltage Range of 4.5 V to 5.5 V
- High-Current 3-State Noninverting Outputs Drive Bus Lines Directly or Up To 15 LSTTL Loads
- Low Power Consumption, 80- μ A Max I_{CC}
- Typical $t_{pd} = 22$ ns
- ± 6 -mA Output Drive at 5 V
- Low Input Current of 1 μ A Max
- Inputs Are TTL-Voltage Compatible
- Bus-Structured Pinout

description/ordering information

These octal edge-triggered D-type flip-flops feature 3-state outputs designed specifically for bus driving. The 'HCT574 devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

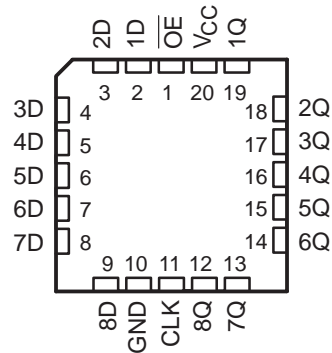
The eight flip-flops enter data on the low-to-high transition of the clock (CLK) input.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

SN54HCT574 . . . J OR W PACKAGE
SN74HCT574 . . . DB, DW, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54HCT574 . . . FK PACKAGE
(TOP VIEW)



ORDERING INFORMATION

| T_A | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|------------|---------------|-----------------------|------------------|
| -40°C to 85°C | PDIP – N | Tube of 20 | SN74HCT574N | SN74HCT574N |
| | SOIC – DW | Tube of 25 | SN74HCT574DW | HCT574 |
| | | Reel of 2000 | SN74HCT574DWR | |
| | SOP – NS | Reel of 2000 | SN74HCT574NSR | HCT574 |
| | SSOP – DB | Reel of 2000 | SN74HCT574DBR | HT574 |
| | TSSOP – PW | Tube of 70 | SN74HCT574PW | HT574 |
| Reel of 2000 | | SN74HCT574PWR | | |
| Reel of 250 | | SN74HCT574PWT | | |
| -55°C to 125°C | CDIP – J | Tube of 20 | SNJ54HCT574J | SNJ54HCT574J |
| | CFP – W | Tube of 85 | SNJ54HCT574W | SNJ54HCT574W |
| | LCCC – FK | Tube of 55 | SNJ54HCT574FK | SNJ54HCT574FK |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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 **TEXAS
INSTRUMENTS**

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description/ordering information (continued)

\overline{OE} does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

FUNCTION TABLE
(each flip-flop)

| INPUTS | | | OUTPUT |
|-----------------|--------|---|--------|
| \overline{OE} | CLK | D | Q |
| L | ↑ | H | H |
| L | ↑ | L | L |
| L | H or L | X | Q_0 |
| H | X | X | Z |

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|----------------|
| Supply voltage range, V_{CC} | -0.5 V to 7 V |
| Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) | ± 20 mA |
| Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) | ± 20 mA |
| Continuous output current, I_O ($V_O = 0$ to V_{CC}) | ± 35 mA |
| Continuous current through V_{CC} or GND | ± 70 mA |
| Package thermal impedance, θ_{JA} (see Note 2): | |
| DB package | 70°C/W |
| DW package | 58°C/W |
| N package | 69°C/W |
| NS package | 60°C/W |
| PW package | 83°C/W |
| Storage temperature range, T_{stg} | -65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

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recommended operating conditions (see Note 3)

| | | SN54HCT574 | | | SN74HCT574 | | | UNIT |
|-----------------|---------------------------------|----------------------------------|-----|-----|-----------------|-----|-----|------|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| V _{CC} | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| V _{IH} | High-level input voltage | V _{CC} = 4.5 V to 5.5 V | | | 2 | | | V |
| V _{IL} | Low-level input voltage | V _{CC} = 4.5 V to 5.5 V | | | 0.8 | | | V |
| V _I | Input voltage | 0 | | | V _{CC} | | | V |
| V _O | Output voltage | 0 | | | V _{CC} | | | V |
| Δt/Δv | Input transition rise/fall time | 500 | | | 500 | | | ns |
| T _A | Operating free-air temperature | -55 | | | 125 | | | °C |

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | T _A = 25°C | | | SN54HCT574 | | SN74HCT574 | | UNIT |
|--------------------|--|-------------------|--------------------------|------|-------|------------|-----|------------|-----|------|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| V _{OH} | V _I = V _{IH} or V _{IL} | 4.5 V | I _{OH} = -20 μA | | 4.4 | 4.499 | 4.4 | 4.4 | V | |
| | | | I _{OH} = -6 mA | | 3.98 | 4.3 | 3.7 | 3.84 | | |
| V _{OL} | V _I = V _{IH} or V _{IL} | 4.5 V | I _{OL} = 20 μA | | 0.001 | 0.1 | 0.1 | 0.1 | V | |
| | | | I _{OL} = 6 mA | | 0.17 | 0.26 | 0.4 | 0.33 | | |
| I _I | V _I = V _{CC} or 0 | 5.5 V | ±0.1 | ±100 | ±1000 | ±1000 | nA | | | |
| I _{OZ} | V _O = V _{CC} or 0 | 5.5 V | ±0.01 | ±0.5 | ±10 | ±5 | μA | | | |
| I _{CC} | V _I = V _{CC} or 0, I _O = 0 | 5.5 V | 8 | | 160 | 80 | μA | | | |
| ΔI _{CC} † | One input at 0.5 V or 2.4 V, Other inputs at 0 or V _{CC} | 5.5 V | 1.4 | 2.4 | 3 | 2.9 | mA | | | |
| C _i | | 4.5 V to 5.5 V | 3 | 10 | 10 | 10 | pF | | | |

† This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

| | | V _{CC} | T _A = 25°C | | SN54HCT574 | | SN74HCT574 | | UNIT |
|--------------------|---------------------------------|-----------------|-----------------------|-----|------------|-----|------------|-----|------|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| f _{clock} | Clock frequency | 4.5 V | 30 | | 20 | | 24 | | MHz |
| | | 5.5 V | 33 | | 22 | | 27 | | |
| t _w | Pulse duration, CLK high or low | 4.5 V | 16 | | 24 | | 20 | | ns |
| | | 5.5 V | 14 | | 22 | | 18 | | |
| t _{su} | Setup time, data before CLK↑ | 4.5 V | 20 | | 30 | | 25 | | ns |
| | | 5.5 V | 17 | | 27 | | 23 | | |
| t _h | Hold time, data after CLK↑ | 4.5 V | 5 | | 5 | | 5 | | ns |
| | | 5.5 V | 5 | | 5 | | 5 | | |

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



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switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V_{CC} | $T_A = 25^\circ\text{C}$ | | | SN54HCT574 | | SN74HCT574 | | UNIT |
|-----------|-----------------|-------------|----------|--------------------------|-----|-----|------------|-----|------------|-----|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| f_{max} | | | 4.5 V | 30 | 36 | | 20 | | 24 | MHz | |
| | | | 5.5 V | 33 | 40 | | 22 | | 27 | | |
| t_{pd} | CLK | Any Q | 4.5 V | | 30 | 36 | | 54 | | 45 | ns |
| | | | 5.5 V | | 25 | 32 | | 48 | | 41 | |
| t_{en} | \overline{OE} | Any Q | 4.5 V | | 26 | 30 | | 45 | | 38 | ns |
| | | | 5.5 V | | 23 | 27 | | 41 | | 34 | |
| t_{dis} | \overline{OE} | Any Q | 4.5 V | | 23 | 30 | | 45 | | 38 | ns |
| | | | 5.5 V | | 22 | 27 | | 41 | | 34 | |
| t_t | | Any Q | 4.5 V | | 10 | 12 | | 18 | | 15 | ns |
| | | | 5.5 V | | 9 | 11 | | 16 | | 14 | |

switching characteristics over recommended operating free-air temperature range, $C_L = 150 \text{ pF}$ (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V_{CC} | $T_A = 25^\circ\text{C}$ | | | SN54HCT574 | | SN74HCT574 | | UNIT |
|-----------|-----------------|-------------|----------|--------------------------|-----|-----|------------|-----|------------|-----|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| f_{max} | | | 4.5 V | 30 | 36 | | 20 | | 24 | MHz | |
| | | | 5.5 V | 33 | 40 | | 22 | | 27 | | |
| t_{pd} | CLK | Any Q | 4.5 V | | 40 | 53 | | 80 | | 66 | ns |
| | | | 5.5 V | | 35 | 47 | | 71 | | 60 | |
| t_{en} | \overline{OE} | Any Q | 4.5 V | | 34 | 47 | | 71 | | 59 | ns |
| | | | 5.5 V | | 29 | 39 | | 94 | | 78 | |
| t_t | | Any Q | 4.5 V | | 18 | 42 | | 63 | | 53 | ns |
| | | | 5.5 V | | 16 | 38 | | 57 | | 48 | |

operating characteristics, $T_A = 25^\circ\text{C}$

| PARAMETER | TEST CONDITIONS | TYP | UNIT |
|--|-----------------|-----|------|
| C_{pd} Power dissipation capacitance per flip-flop | No load | 93 | pF |

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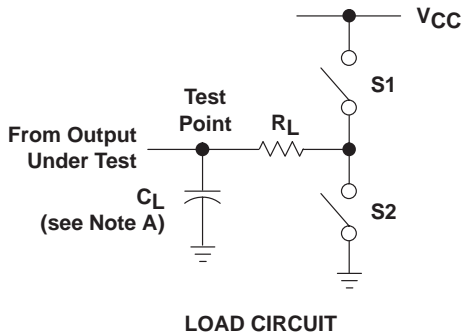


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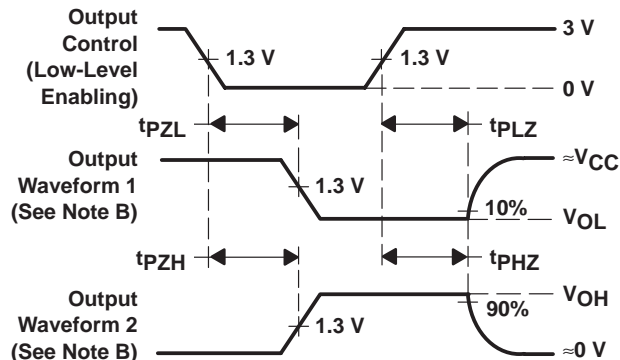
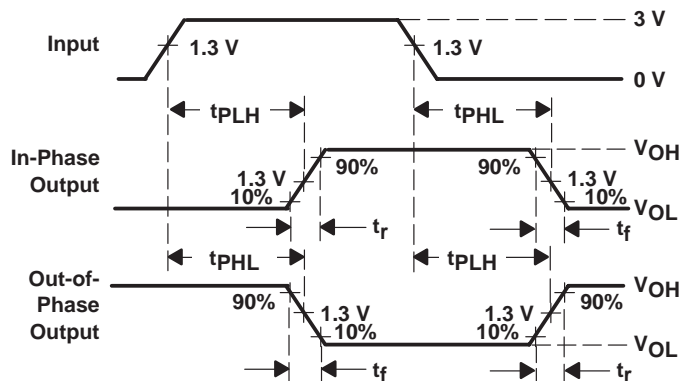
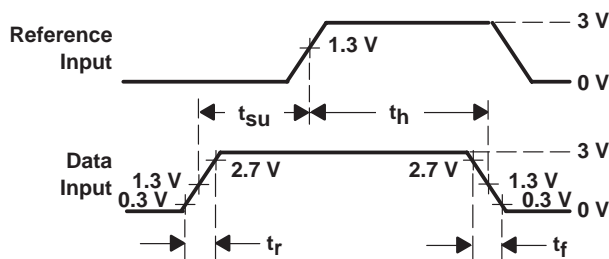
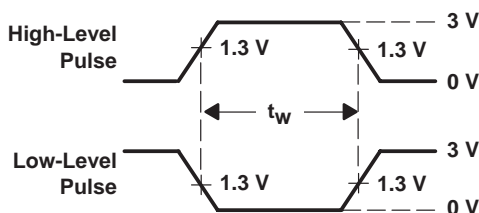
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PARAMETER MEASUREMENT INFORMATION



| PARAMETER | R_L | C_L | S1 | S2 |
|-------------------|-----------|-----------------|--------|--------|
| t_{en} | t_{PZH} | 50 pF or 150 pF | Open | Closed |
| | t_{PZL} | | Closed | Open |
| t_{dis} | t_{PHZ} | 50 pF | Open | Closed |
| | t_{PLZ} | | Closed | Open |
| t_{pd} or t_t | -- | 50 pF or 150 pF | Open | Open |



- NOTES:
- A. C_L includes probe and test-fixture capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r = 6$ ns, $t_f = 6$ ns.
 - D. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
 - E. The outputs are measured one at a time with one input transition per measurement.
 - F. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - G. t_{PZL} and t_{PZH} are the same as t_{en} .
 - H. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN74HCT574DBR | ACTIVE | SSOP | DB | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HT574 | Samples |
| SN74HCT574DBRE4 | ACTIVE | SSOP | DB | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HT574 | Samples |
| SN74HCT574DW | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HCT574 | Samples |
| SN74HCT574DWG4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HCT574 | Samples |
| SN74HCT574DWR | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HCT574 | Samples |
| SN74HCT574DWRE4 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HCT574 | Samples |
| SN74HCT574DWRG4 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HCT574 | Samples |
| SN74HCT574N | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 85 | SN74HCT574N | Samples |
| SN74HCT574N3 | OBSOLETE | PDIP | N | 20 | | TBD | Call TI | Call TI | -40 to 85 | | |
| SN74HCT574NE4 | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 85 | SN74HCT574N | Samples |
| SN74HCT574NSR | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HCT574 | Samples |
| SN74HCT574PW | ACTIVE | TSSOP | PW | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HT574 | Samples |
| SN74HCT574PWG4 | ACTIVE | TSSOP | PW | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HT574 | Samples |
| SN74HCT574PWLE | OBSOLETE | TSSOP | PW | 20 | | TBD | Call TI | Call TI | -40 to 85 | | |
| SN74HCT574PWR | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HT574 | Samples |
| SN74HCT574PWRG4 | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HT574 | Samples |
| SN74HCT574PWT | ACTIVE | TSSOP | PW | 20 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HT574 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74HCT574DBR | SSOP | DB | 20 | 2000 | 330.0 | 16.4 | 8.2 | 7.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74HCT574DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74HCT574NSR | SO | NS | 20 | 2000 | 330.0 | 24.4 | 9.0 | 13.0 | 2.4 | 12.0 | 24.0 | Q1 |
| SN74HCT574PWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |
| SN74HCT574PWT | TSSOP | PW | 20 | 250 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74HCT574DBR | SSOP | DB | 20 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74HCT574DWR | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74HCT574NSR | SO | NS | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74HCT574PWR | TSSOP | PW | 20 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74HCT574PWT | TSSOP | PW | 20 | 250 | 367.0 | 367.0 | 38.0 |

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - $\triangle D$ The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW0020A



PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

IMPORTANT NOTICE

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