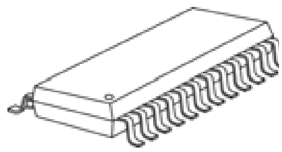
16-Channel SPWM Constant Current LED Driver with Low Knee Voltage

Features

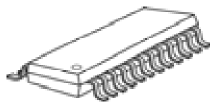
- 16 constant-current output channels
- 16-bit color depth PWM control
- Scrambled-PWM technology to improve refresh rate
- Compulsory open circuit detection to detect individual LED errors
  - -Full panel, data independent
  - -Silent error detection with 0.1mA
- 6-bit programmable output current gain
- Constant output current range: 2~45mA
  - -2~ 45mA at 5.0V supply voltage
  - -2~30mA at 3.3V supply voltage
- Output current accuracy:
  - -Between channels: <±3% (typ.), and
  - -Between ICs: <±3% (typ.)
- Staggered delay of output, preventing from current surge
- Maximum data clock frequency: 30MHz
- Schmitt trigger input
- 3.0V-5.5V supply voltage

Small Outline Package



GF: SOP24L-300-1.00

Shrink SOP



GP: SSOP24L-150-0.64

Product Description

MBI5045 is designed for LED video applications using internal Pulse Width Modulation (PWM) control with 16-bit color depth which features a 16-bit shift register to convert serial input data into each pixel gray scale of output port. Also, the function is a 16-channel constant current LED driver with V_{DS}=0.2V @ I_{OUT}=20mA, which is excellent compared to the conventional design. MBI5045 is dedicated to lowering power consumption in LED video display application. The low knee voltage (LKV) design makes MBI5045 work at a constant output current with low V_{DS} and still guarantee PrecisionDrive™ feature. The output current can be preset through an external resistor. Moreover, the preset current of MBI5045 can be further programmed to 64 gain steps for LED global brightness adjustment.

With Scrambled-PWM (S-PWM) technology, MBI5045 enhances Pulse Width Modulation by scrambling the “on” time into several “on” periods. The enhancement equivalently increases the visual refresh rate. When building a 16-bit color depth video, S-PWM reduces the flickers and improves the fidelity. MBI5045 offloads the signal timing generation of the host controller which just needs to feed data into drivers. MBI5045 drives the corresponding brightness of LEDs by specifying image data. With MBI5045, all output channels can be built with 16-bit color depth (65,536 gray scales). Each LED’s brightness can be calibrated with the compensated gamma correction or LED deviation information inside the 16-bit image data.

MBI5045 provides a silent error detection which detects LED open circuit error and the execution won’t be observed.

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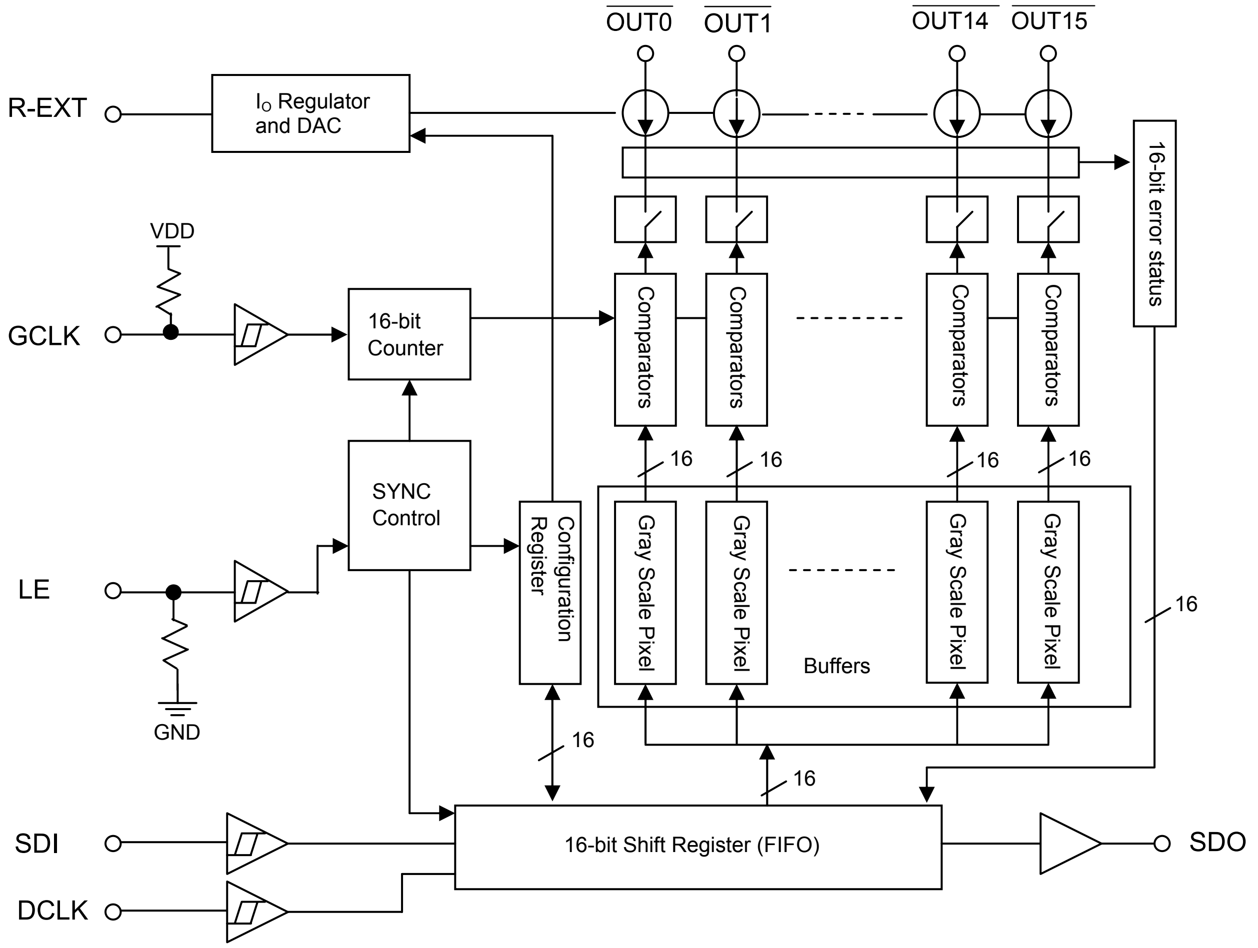
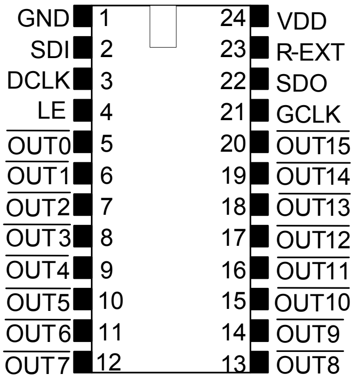
Block Diagram



Pin Configuration



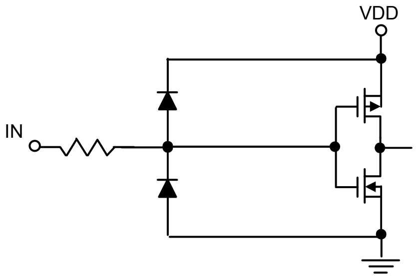
MBI5045GF/GP

Terminal Description

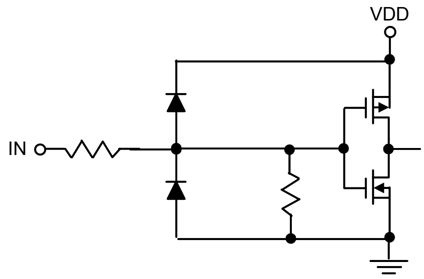
Pin Name	Function
GND	Ground terminal for control logic and current sink
SDI	Serial-data input to the shift register
DCLK	Clock input terminal used to shift data on rising edge and carries command information when LE is asserted.
LE	Data strobe terminal and controlling command with DCLK
$\overline{\text{OUT0}}$ ~ $\overline{\text{OUT15}}$	Constant current output terminals
GCLK	Gray scale clock terminal Clock input for gray scale. The gray scale display is counted by gray scale clock comparing with input data.
SDO	Serial-data output to the receiver-end SDI of next driver IC
R-EXT	Input terminal used to connect an external resistor for setting up output current for all output channels
VDD	3.3V/5V supply voltage terminal

Equivalent Circuits of Inputs and Outputs

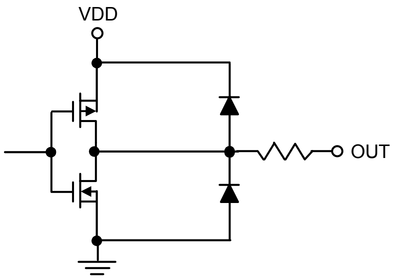
GCLK, DCLK, SDI terminal



LE terminal



SDO terminal



Maximum Rating

Characteristic		Symbol	Rating	Unit
Supply Voltage		V_{DD}	7	V
Input Pin Voltage (SDI)		V_{IN}	-0.4~V_{DD}+0.4	V
Output Current		I_{OUT}	+45	mA
Sustaining Voltage at OUT Port		V_{DS}	17	V
GND Terminal Current		I_{GND}	+720	mA
Power Dissipation (On PCB, Ta=25°C)*	GF Type	P_D	2.41	W
	GPType		1.95	
Thermal Resistance (On PCB, Ta=25°C)*	GF Type	$R_{th(j-a)}$	66.69	°C/W
	GP Type		69.50	
Junction Temperature		$T_{j,max}$	150**	°C
Operating Ambient Temperature		T_{opr}	-40~+85	°C
Storage Temperature		T_{stg}	-55~+150	°C
ESD Rating	Human Body Mode (MIL-STD-883G Method 3015.7)	HBM	Class 3A (4000V~7999V)	-
	Machine Mode (JEDEC EIA/JESD22-A115)	MM	Class C (≧400V)	-

*The PCB size is 76.2mm*114.3mm in simulation. Please refer to JEDEC JESD51.

** Operation at the maximum rating for extended periods may reduce the device reliability; therefore, the suggested junction temperature of the device is under 125°C.

Note: The performance of thermal dissipation is strongly related to the size of thermal pad, thickness and layer numbers of the PCB. The empirical thermal resistance may be different from simulative value. Users should plan for expected thermal dissipation performance by selecting package and arranging layout of the PCB to maximize the capability.

Electrical Characteristics (V_{DD}=5.0V)

Characteristics		Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage		V_{DD}	-	4.5	5.0	5.5	V
Sustaining Voltage at OUT Ports		V_{DS}	$\overline{OUT0}$ ~ $\overline{OUT15}$	-	-	17.0	V
Output Current		I_{OUT}	Refer to "Test Circuit for Electrical Characteristics"	2	-	45	mA
Output Current		I_{OH}	SDO	-	-	-1.0	mA
Output Current		I_{OL}	SDO			1.0	mA
Input Voltage	"H" level	V_{IH}	Ta=-40~85ºC	0.7xV_{DD}	-	V_{DD}	V
Input Voltage	"L" level	V_{IL}	Ta=-40~85ºC	GND	-	0.3xV_{DD}	V
Output Leakage Current		I_{OH}	V_{DS}=17.0V	-	-	0.5	μA
Output Voltage	SDO	V_{OL}	I_{OL}=+1.0mA	-	-	0.4	V
Output Voltage	SDO	V_{OH}	I_{OH}=-1.0mA	V_{DD}-0.4	-	-	V
Current Skew (Channel)		dI_{OUT}	I_{OUT}=20mA, V_{DS}=0.25V; R_{ext}=680Ω	-	±3.0	±4.0	%
Current Skew (IC)		dI_{OUT2}	I_{OUT}=20mA, V_{DS}=0.25V; R_{ext}=680Ω	-	±3.0	±6.0	%
Output Current vs. Output Voltage Regulation*		%/dV_{DS}	V_{DS} within 0.25V and 1.5V, R_{ext}=680Ω@20mA	-	±0.2	±0.5	% / V
Output Current vs. Supply Voltage Regulation*		%/dV_{DD}	V_{DD} within 4.5V and 5.5V	-	±1.0	±2.0	% / V
LED Open Error Detection Threshold		$V_{DS,TH}$	-	-	0.15	0.20	V
Pull-down Resistor		R_{IN}(down)	LE	250	450	800	KΩ
Supply Current	"Off"	I_{DD}(off) 1	R_{ext}=Open, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off	-	5.5	9.0	mA
Supply Current	"Off"	I_{DD}(off) 2	R_{ext}=6KΩ, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off	-	6.5	8.5	mA
Supply Current	"Off"	I_{DD}(off) 3	R_{ext}=680Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off	-	8.0	11.0	mA
Supply Current	"Off"	I_{DD}(off) 4	R_{ext}=348Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off	-	10.0	13.0	mA
Supply Current	"On"	I_{DD}(on) 1	R_{ext}=6KΩ, $\overline{OUT0}$ ~ $\overline{OUT15}$ =On	-	6.5	9.0	mA
Supply Current	"On"	I_{DD}(on) 2	R_{ext}=680Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =On	-	8.0	11.5	mA
Supply Current	"On"	I_{DD}(on) 3	R_{ext}=348Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =On		10.0	13.5	mA

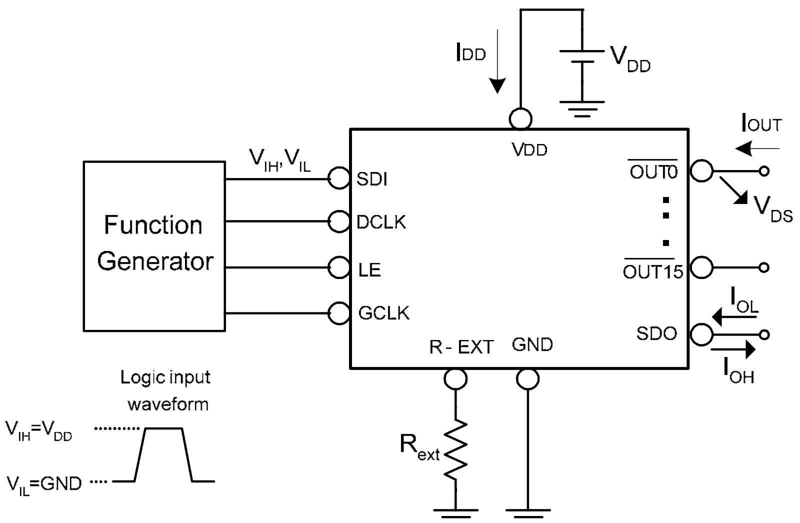
*One channel on.

Electrical Characteristics (V_{DD}=3.3V)

Characteristics		Symbol	Condition		Min.	Typ.	Max.	Unit
Supply Voltage		V_{DD}	-		3.0	3.3	3.6	V
Sustaining Voltage at OUT Ports		V_{DS}	$\overline{\text{OUT0}}$ ~ $\overline{\text{OUT15}}$		-	-	17.0	V
Output Current		I_{OUT}	Refer to “Test Circuit for Electrical Characteristics”		2	-	30	mA
		I_{OH}	SDO		-	-	-1.0	mA
		I_{OL}	SDO		-	-	1.0	mA
Input Voltage	“H” level	V_{IH}	Ta=-40~85ºC		0.7xV_{DD}	-	V_{DD}	V
	“L” level	V_{IL}	Ta=-40~85ºC		GND	-	0.3xV_{DD}	V
Output Leakage Current		I_{OH}	V_{DS}=17.0V		-	-	0.5	μA
Output Voltage	SDO	V_{OL}	I_{OL}=+1.0mA		-	-	0.4	V
		V_{OH}	I_{OH}=-1.0mA		V_{DD}-0.4	-	-	V
Current Skew (Channel)		dI_{OUT}	I_{OUT}=20mA V_{DS}=0.25V	R_{ext}=680Ω	-	±3.0	±4.0	%
Current Skew (IC)		dI_{OUT2}	I_{OUT}=20mA V_{DS}=0.25V	R_{ext}=680Ω	-	±3.0	±6.0	%
Output Current vs. Output Voltage Regulation*		%/dV_{DS}	V_{DS} within 0.25V and 1.5V R_{ext}=680Ω@20mA		-	±0.2	±0.5	%/ V
Output Current vs. Supply Voltage Regulation*		%/dV_{DD}	V_{DD} within 3.0V and 3.6V		-	±1.0	±2.0	%/ V
LED Open Error Detection Threshold		$V_{DS,TH}$	-		-	0.15	0.20	V
Pull-down Resistor		R_{IN}(down)	LE		250	450	800	KΩ
Supply Current	“Off”	I_{DD}(off) 1	R_{ext}=Open,	$\overline{\text{OUT0}}$ ~ $\overline{\text{OUT15}}$ =Off	-	4.5	8.0	mA
		I_{DD}(off) 2	R_{ext}=6KΩ,	$\overline{\text{OUT0}}$ ~ $\overline{\text{OUT15}}$ =Off	-	5.5	7.5	
		I_{DD}(off) 3	R_{ext}=680Ω,	$\overline{\text{OUT0}}$ ~ $\overline{\text{OUT15}}$ =Off	-	7.0	10.0	
		I_{DD}(off) 4	R_{ext}=460Ω,	$\overline{\text{OUT0}}$ ~ $\overline{\text{OUT15}}$ =Off	-	8.0	11.0	
	“On”	I_{DD}(on) 1	R_{ext}=6KΩ,	$\overline{\text{OUT0}}$ ~ $\overline{\text{OUT15}}$ =Off	-	5.5	8.0	
		I_{DD}(on) 2	R_{ext}=680Ω,	$\overline{\text{OUT0}}$ ~ $\overline{\text{OUT15}}$ =Off	-	7.0	10.5	
		I_{DD}(on) 3	R_{ext}=460Ω,	$\overline{\text{OUT0}}$ ~ $\overline{\text{OUT15}}$ =Off	-	8.0	11.5	

*One channel on.

Test Circuit for Electrical Characteristics



Switching Characteristics (V_{DD}=5.0V)

(Test condition: Ta=25°C)

Characteristics		Symbol	Condition	Min.	Typ.	Max.	Unit
Setup Time	SDI - DCLK↑	t_{SU0}	V_{IH}=V_{DD} V_{IL}=GND Rext=680Ω R_L=150Ω C_L=10PF I_{OUT}=20mA C1=100nF C2=22uF C_{SDO}=10PF V_L=3.3V	7	-	-	ns
	LE↑ – DCLK↑	t_{SU1}		7	-	-	ns
	LE↓ – DCLK↑	t_{SU2}		7	-	-	ns
Hold Time	DCLK↑ - SDI	t_{H0}		7	-	-	ns
	DCLK↑ - LE↓	t_{H1}		7	-	-	ns
Propagation Delay Time	DCLK - SDO	t_{PD0}		-	25	30	ns
	GCLK – $\overline{OUT2n}$ *	t_{PD1}		-	50	80	ns
	LE–SDO**	t_{PD2}		-	40	50	ns
Staggered Delay of Output	$\overline{OUT2n}$ - $\overline{OUT2n+1}$ *	t_{DL}		-	5	-	ns
Pulse Width	LE	$t_{w(L)}$		15	-	-	ns
	DCLK	$t_{w(DCLK)}$		10	-	-	ns
	GCLK	$t_{w(GCLK)}$		35	-	-	ns
	GCLK, 2x	$t_{w(GCLK,\ 2x)}$		35	-	-	ns
Output Rise Time of Output Ports		t_{OR}		-	35	45	ns
Output Fall Time of Output Ports		t_{OR}		-	35	45	ns
SDO Rise Time		$t_{r,SDO}$		-	10	-	ns
SDO Fall Time		$t_{f,SDO}$		-	10	-	ns
Data Clock Frequency		F_{DCLK}		-	-	30	MHz
Gray Scale Clock Frequency***		F_{GCLK}		-	-	14	MHz
2x Gray Scale Clock Frequency***		$F_{GCLK,2x}$		-	-	7	MHz

* Refer to the Timing Waveform, where n=0~7

**In timing of “Read Configuration” and “Read Error Status Code”, the next DCLK rising edge should be t_{PD2} after the falling edge of LE.

***With uniform output current.

Switching Characteristics (V_{DD}=3.3V)

(Test condition: Ta=25°C)

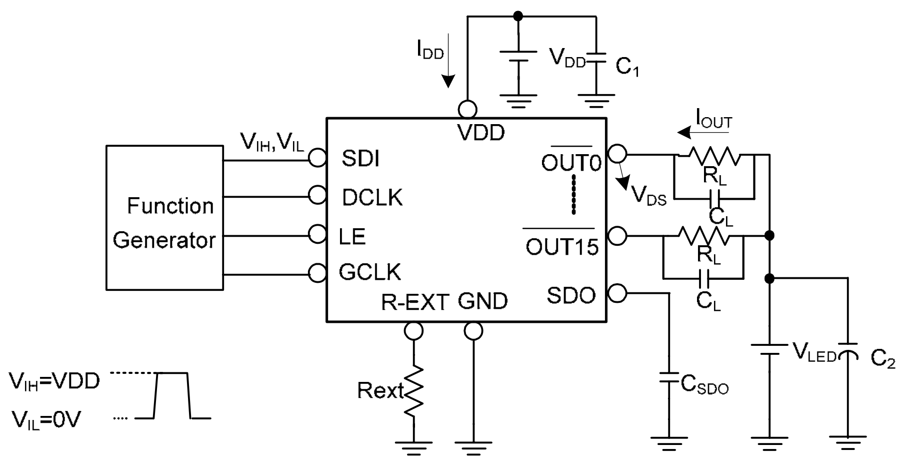
Characteristics		Symbol	Condition	Min.	Typ.	Max.	Unit
Setup Time	SDI - DCLK↑	t_{SU0}	$V_{IH}=V_{DD}$ V_{IL}=GND Rext=680Ω R_L=150Ω C_L=10PF I_{OUT}=20mA C1=100nF C2=22uF C_{SDO}=10PF V_L=3.3V	10	-	-	ns
	LE↑ – DCLK↑	t_{SU1}		10	-	-	ns
	LE↓ – DCLK↑	t_{SU2}		10	-	-	ns
Hold Time	DCLK↑ - SDI	t_{H0}		10	-	-	ns
	DCLK↑ - LE↓	t_{H1}		10	-	-	ns
Propagation Delay Time	DCLK – SDO	t_{PD0}		-	30	35	ns
	GCLK – $\overline{OUT2n}$ *	t_{PD1}		-	80	120	ns
	LE–SDO**	t_{PD2}		-	50	60	ns
Staggered Delay of Output	$\overline{OUT2n}$ - $\overline{OUT2n+1}$ *	t_{DL}		-	5	-	ns
Pulse Width	LE	$t_{w(L)}$		20	-	-	ns
	DCLK	$t_{w(DCLK)}$		15	-	-	ns
	GCLK	$t_{w(GCLK)}$		45	-	-	ns
	GCLK, 2x	$t_{w(GCLK, 2x)}$		45	-	-	ns
Output Rise Time of Output Ports		t_{OR}		-	45	55	ns
Output Fall Time of Output Ports		t_{OR}		-	45	55	ns
SDO Rise Time		$t_{r,SDO}$		-	10	-	ns
SDO Fall Time		$t_{f,SDO}$		-	10	-	ns
Data Clock Frequency		F_{DCLK}		-	-	25	MHz
Gray Scale Clock Frequency		F_{GCLK}		-	-	11	MHz
2x Gray Scale Clock Frequency***		$F_{GCLK,2x}$		-	-	5.5	MHz

* Refer to the Timing Waveform, where n=0~7

**In timing of "Read Configuration" and "Read Error Status Code", the next DCLK rising edge should be t_{PD2} after the falling edge of LE.

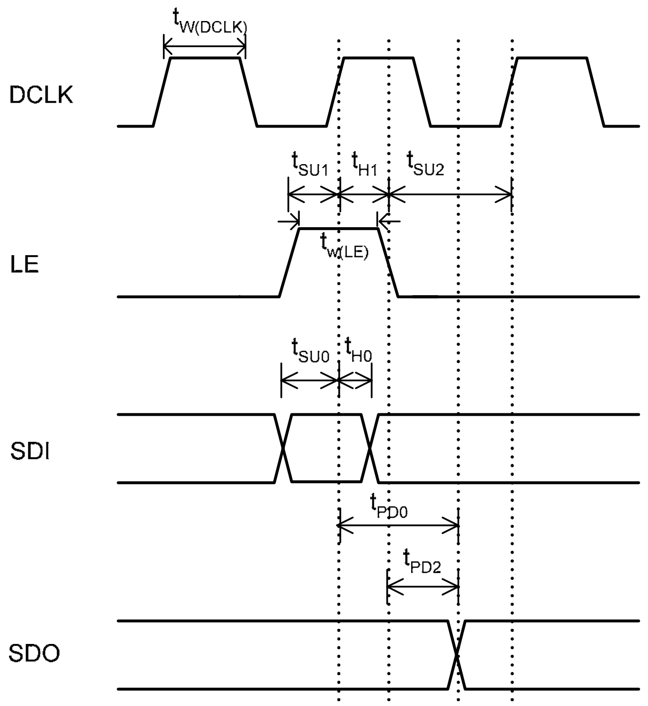
***With uniform output current.

Test Circuit for Switching Characteristics

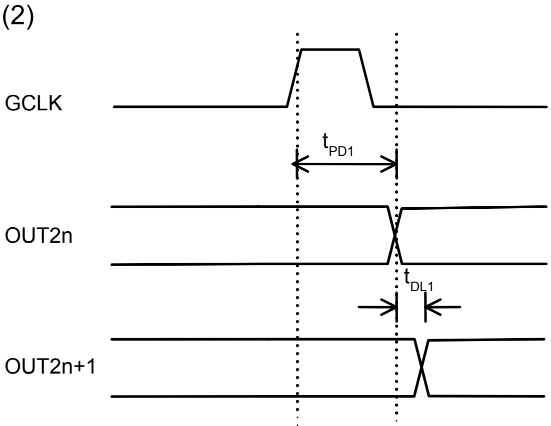


Timing Waveform

(1)



(2)



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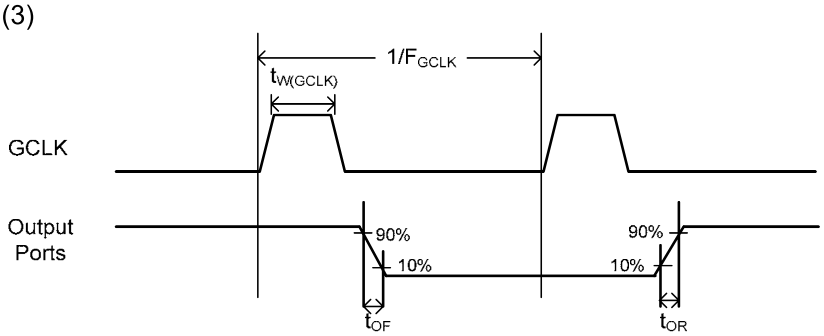
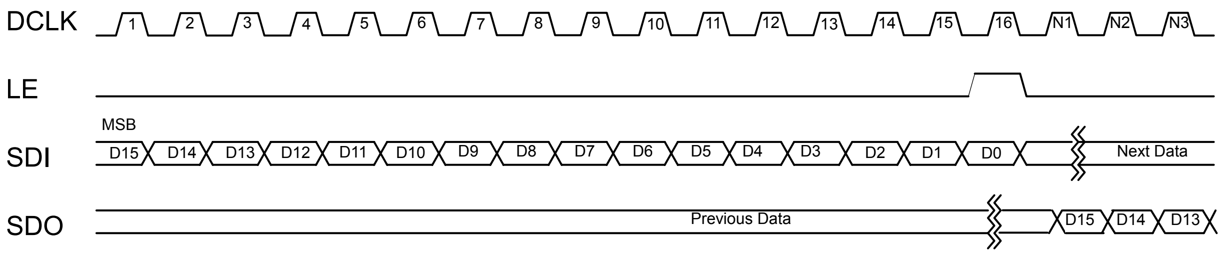


Principle of Operation

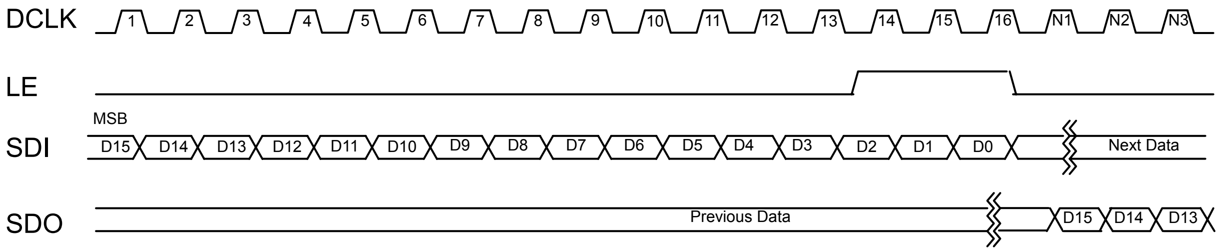
Control Command

Command Name	Signals Combination: LE	Signals Combination: Number of DCLK Rising Edge when LE is asserted	Description: The Action after a Falling Edge of LE
Data Latch	High	1	Serial data are transferred to the buffers
Global Latch	High	3	Buffer data are transferred to the comparators
Read Configuration	High	5	Move out “configuration register” to the shift registers
Write Configuration	High	11	Serial data are transferred to the “configuration register”
Enable Write Configuration	High	15	To enable “Write Configuration”
Enable “Error Detection”	High	17	To detect the status of each output’s LED

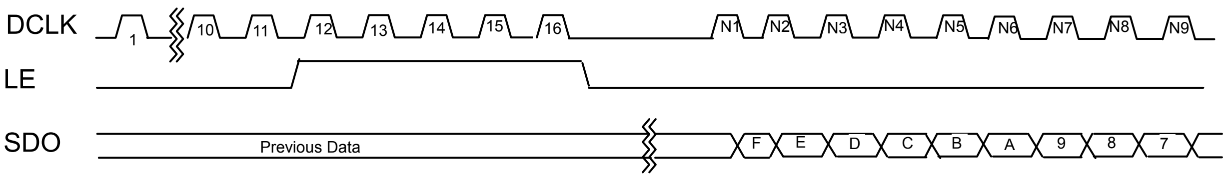
Data Latch



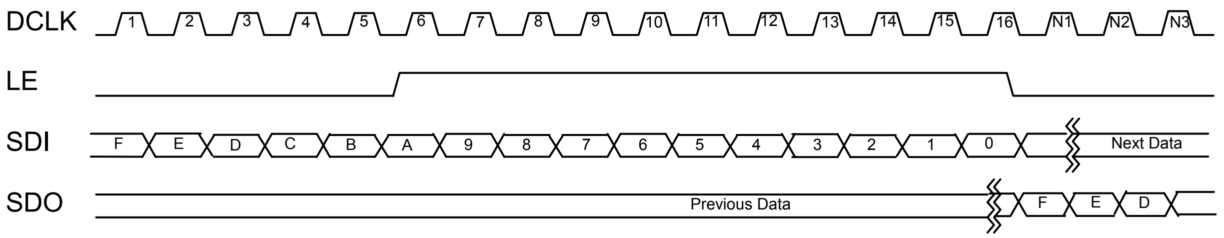
Global Latch



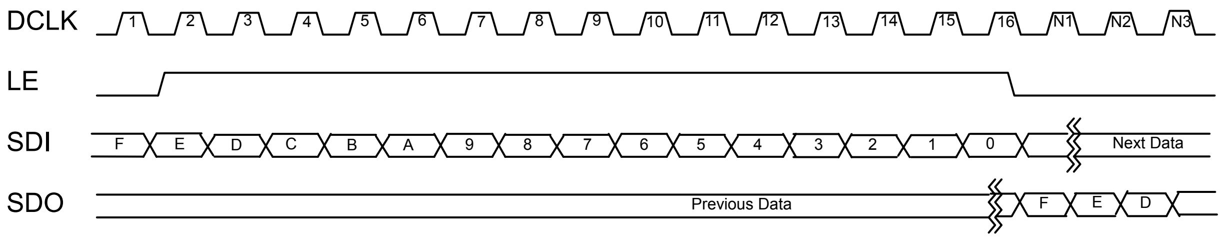
Read Configuration



Write Configuration



Enable Write Configuration

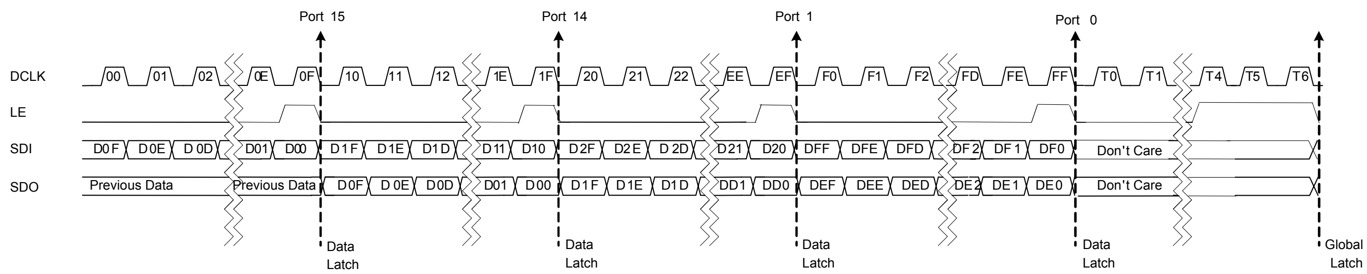


Setting Gray Scales of Pixels

MBI5045 implements the gray level of each output port using the S-PWM control algorithm. With the 16-bit data, all output channels can be built with 65,536 gray scales.

The 16-bit input shift register latches 16 times of the gray scale data into each data buffer with a “data latch” command sequentially. With a “global latch” command for additional latch, the 256-bit data buffers will be clocked in with the MSB first, loading the data from port 15 to port 0.

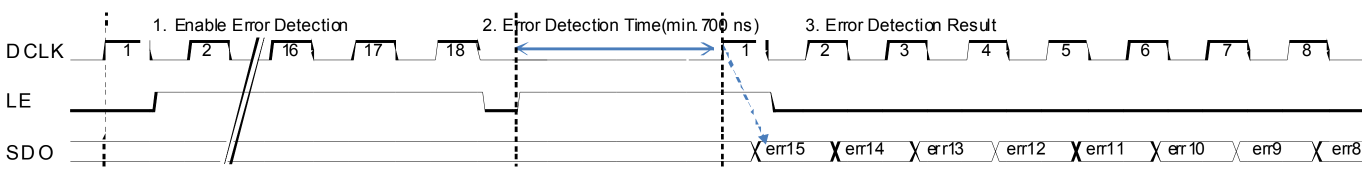
Full Timing for Data Loading



Error Detection Principle

The principle of MBI5045 LED open-circuit detection (LE+17DCLK) is based on the fact that the LED loading status is judged by comparing the effective voltage value (V_{DS}) of each output port with the target voltage ($V_{DS,TH}$) = 0.15V. Thus, after the command of “error detection”, the output ports of MBI5045 will be turned on with current 0.1mA for open-circuit detection.

The error detection time (t_{EDD}) is from the LE falling edge of “enable error detection” command to the LE falling edge of “read error status code” command. The detection time shall be controlled within a proper length. Longer error detection time may cause flickers. Conversely, if the error detection time is shorter; the detection result may not be stable. In general case, LE is suggested to last over 700ns. When the detection is finished, the LE falling edge should follow the first DCLK falling edge for reading the error detection result.

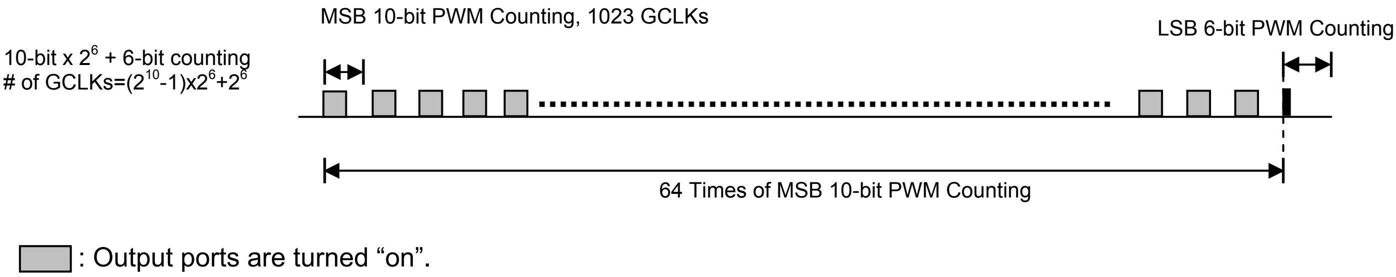


The relationship between the error status code and the effective output point is shown below:

State of Output Port	Condition of Effective Output Point		Detected Error Status Code	Meaning
On / Off	I_{OUT}=0.1mA,	$V_{DS}<V_{DS,\ TH}$	"0"	Error
		$V_{DS} \geqq V_{DS,\ TH}$	"1"	Normal

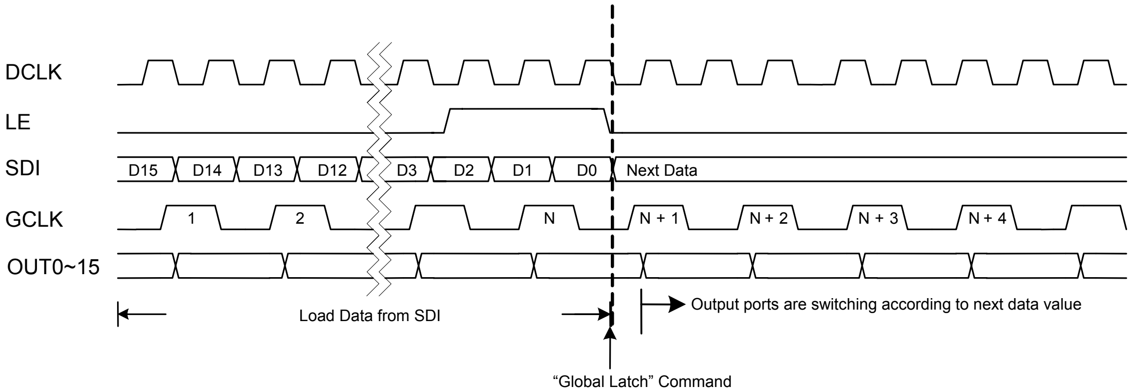
The PWM Counting Mode

MBI5045 supports S-PWM, scrambled PWM, technology. With S-PWM , the total PWM cycles can be broken down into MSB (Most Significant Bits) and LSB (Least Significant Bits) of gray scale cycles, and the MSB information can be dithered across many refresh cycles to achieve overall same high bit resolution.



Synchronization for PWM Counting

MBI5045 updates the next image data into output buffer immediately, no matter the counting status of previous image data is. In this mode, system controller will synchronize the GCLK according image data outside MBI5045 by itself. Otherwise, the conflict of previous image data and next image data will cause the data lost.



Definition of Configuration Register

MSB LSB

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0

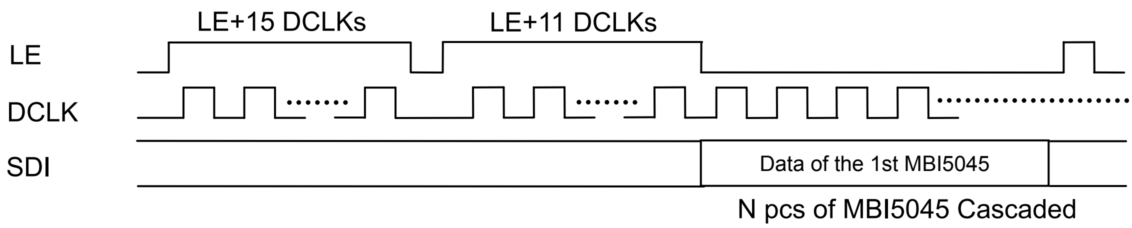
e.g. Default Value

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	6'b101011						0	0	0	0

Bit	Attribute	Definition	Value	Function
F~A	Read	Reserved	000000	Please keep "000000"
9~4	Read/Write	Current gain adjustment	000000~ 111111	6'b101011 (Default) 000000:12.5% 101011:100% 111111:200%
3	Read/Write	GCLK multiplier	0 (Default)	Disable
			1	Enable
2~1	Read/Write	Reserved	00	Please keep "00"
0	Read/Write	Lower ghost reduction	0 (Default)	Disable
			1	Enable

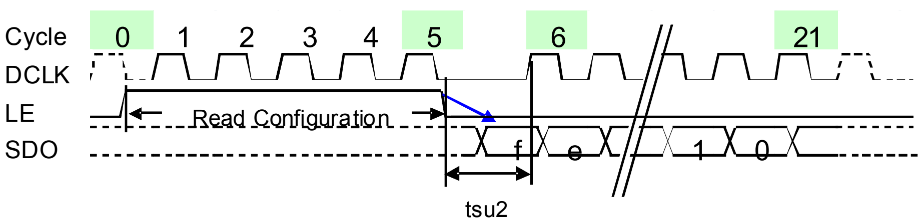
Write Configuration Register

MBI5045 can write a configuration register when receiving one LE pulse containing 11 DCLKs, and then send a 16-bit configuration setting to each LED driver. It is necessary to send an "Enable Write Configuration" command, LE pulse containing 15 DCLKs before setting the configuration register to keep it from being re-written by noise. The following figure shows the input signal waveform when cascading N pieces of MBI5045:



Read Configuration Register

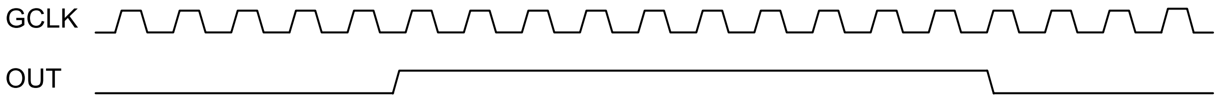
"Read configuration" command is used to read the configuration register of MBI5045. When this command is received, the 16-bit data of configuration register will be shifted out from SDO pin and MSB bit will be shifted out first.



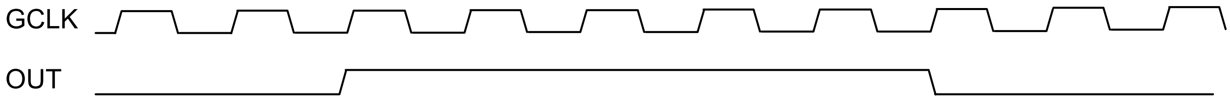
GCLK Rising/ Falling Edge Trigger

It will enable GCLK multiplier function to set bit 3 of control register to “1”. Compared to output channel triggered by traditional rising edge, MBI5045 provides a feature in rising/ falling edge trigger mode that can realize higher refresh rate at lower GCLK frequency to lower the impact of EMI. In rising/ falling edge trigger mode, a 16-bit PWM cycle can be accomplished in 32,768 GCLK counts.

Rising edge trigger
GCLK=14Mhz, PWM=10



Rising/falling edge trigger
GCLK=7Mhz, PWM=10



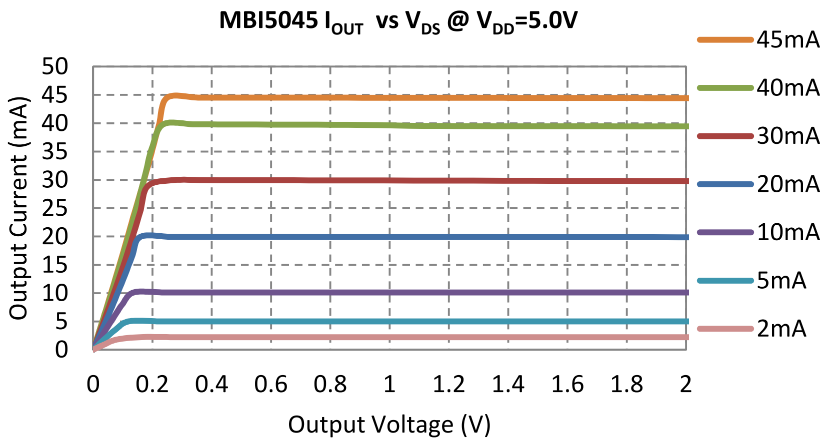
Please be noted that maximum frequency of GCLK should be within 7Mhz in rising/ falling edge trigger mode because of the limitation of the output ports t_{OR} and t_{OF} to ensure getting a constant output current.

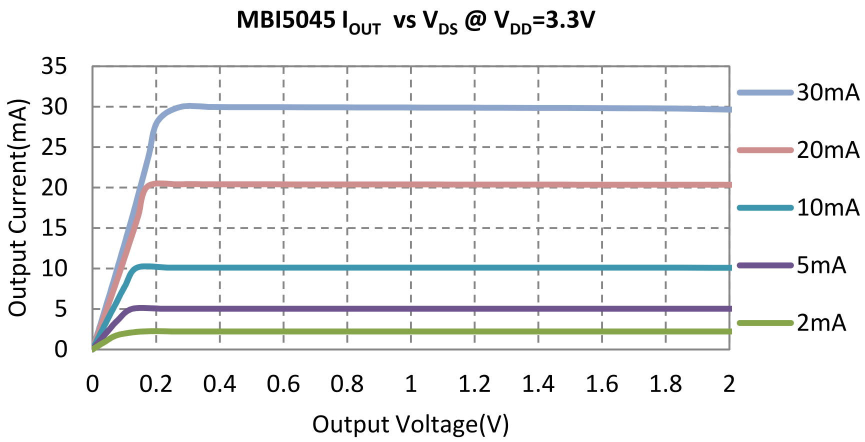
Constant Current

In LED display application, MBI5045 provides nearly no variation in current from channel to channel and from IC to IC. This can be achieved by:

1) The typical current variation between channels is less than ±4%, and that between ICs is less than ±6.0%.

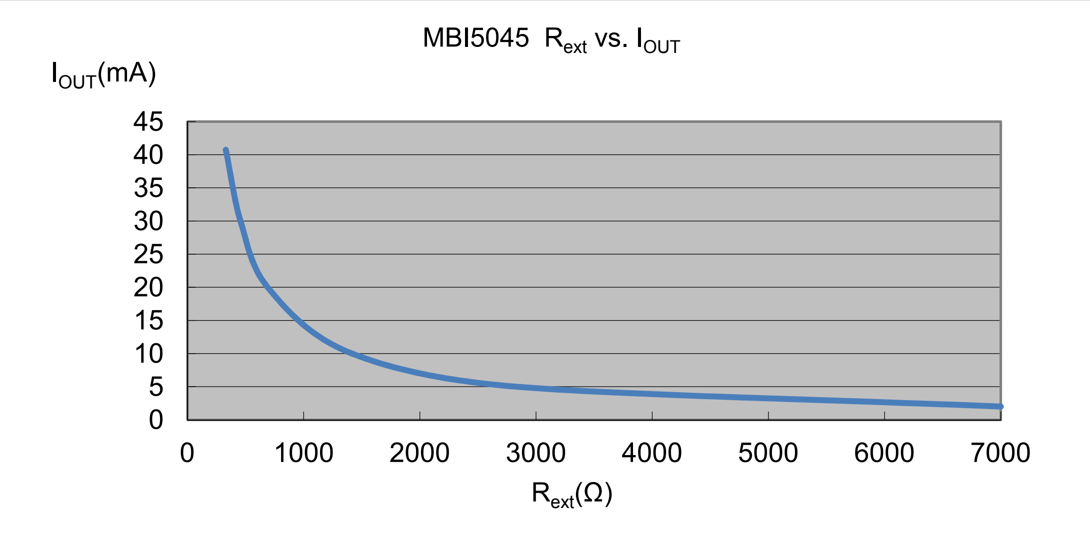
2) In addition, the current characteristic of output stage is flat and users can refer to the figure as shown below. The output current can be kept constant regardless of the variations of LED forward voltages (V_F). This guarantees LED to be performed on the same brightness as user's specification.





Setting Output Current

The output current (I_{OUT}) is set by an external resistor, R_{ext}. The default relationship between I_{OUT} and R_{ext} is shown in the following figure.

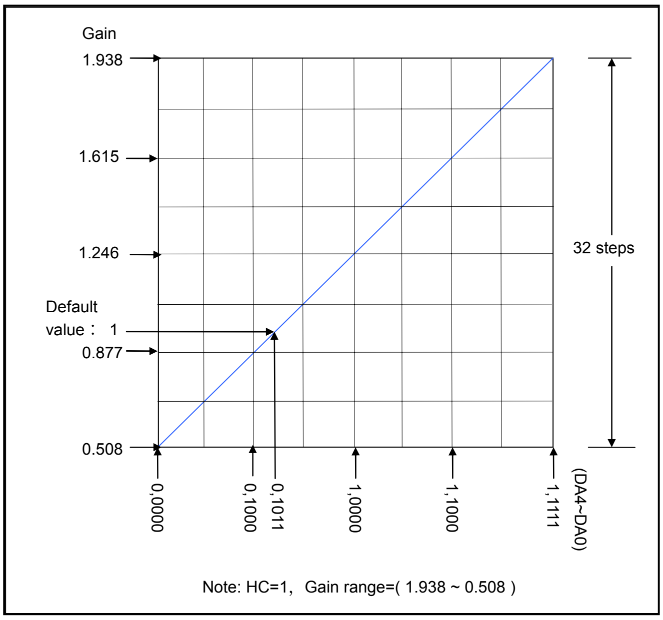


Also, the output current can be calculated from the equation:

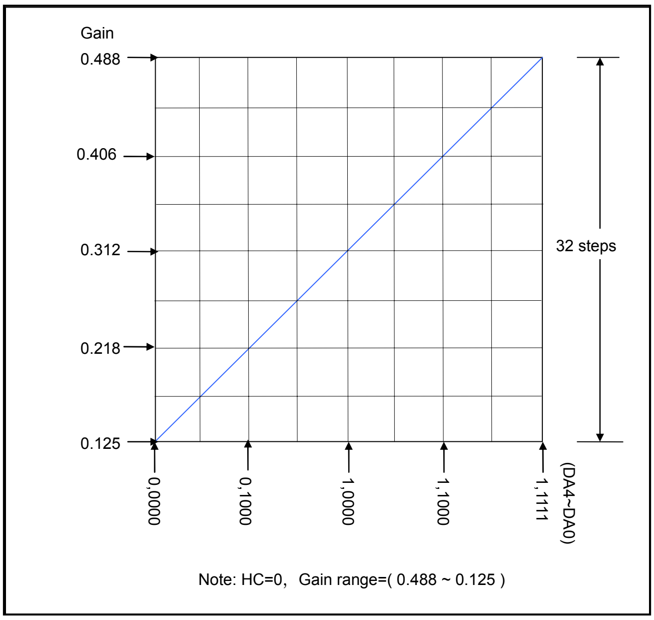
$V_{R\text{-}EXT}$=0.61Volt x G; I_{OUT}=($V_{R\text{-}EXT}$/ R_{ext})x22.5

Whereas R_{ext} is the resistance of the external resistor connected to R-EXT terminal and $V_{R\text{-}EXT}$ is its voltage. G is the digital current gain, which is set by the bit9 – bit2 of the configuration register. The default value of G is 1. For your information, the output current is about 20mA when R_{ext}=680Ω if G is set to default value The formula and setting for G are described in next section.

Current Gain Adjustment



Note: HC=1, Gain range=(1.938 ~ 0.508)



Note: HC=0, Gain range=(0.488 ~ 0.125)

The bit 9 to bit 4 of the configuration register set the gain of output current, i.e., G. As totally 6-bit in number, i.e., ranged from 6’b000000 to 6’b111111, these bits allow the user to set the output current gain up to 64 levels. These bits can be further defined inside Configuration Register as follows:

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	HC	DA4	DA3	DA2	DA1	DA0	-	-	-	-

1. Bit 9 is HC bit. The setting is in low current band when HC=0, and in high current band when HC=1.
2. Bit 8 to bit 4 are DA4 ~ DA0.

The relationship between these bits and current gain G is:

HC=1, D=(65xG-33)/3

HC=0, D=(256xG-32)/3

and D in the above decimal numeration can be converted to its equivalent in binary form by the following equation:

D= DA4x2^4+DA3x2^3+DA2x2^2+DA1x2^1+DA0x2^0

In other words, these bits can be looked as a floating number with 1-bit exponent HC and 5-bit mantissa DA4~DA0.

For example,

HC=1, G=1.246, D=(65x1.246-33)/3=16

the D in binary form would be:

D=16=1x2^4+0x2^3+0x2^2+0x2^1+0x2^0

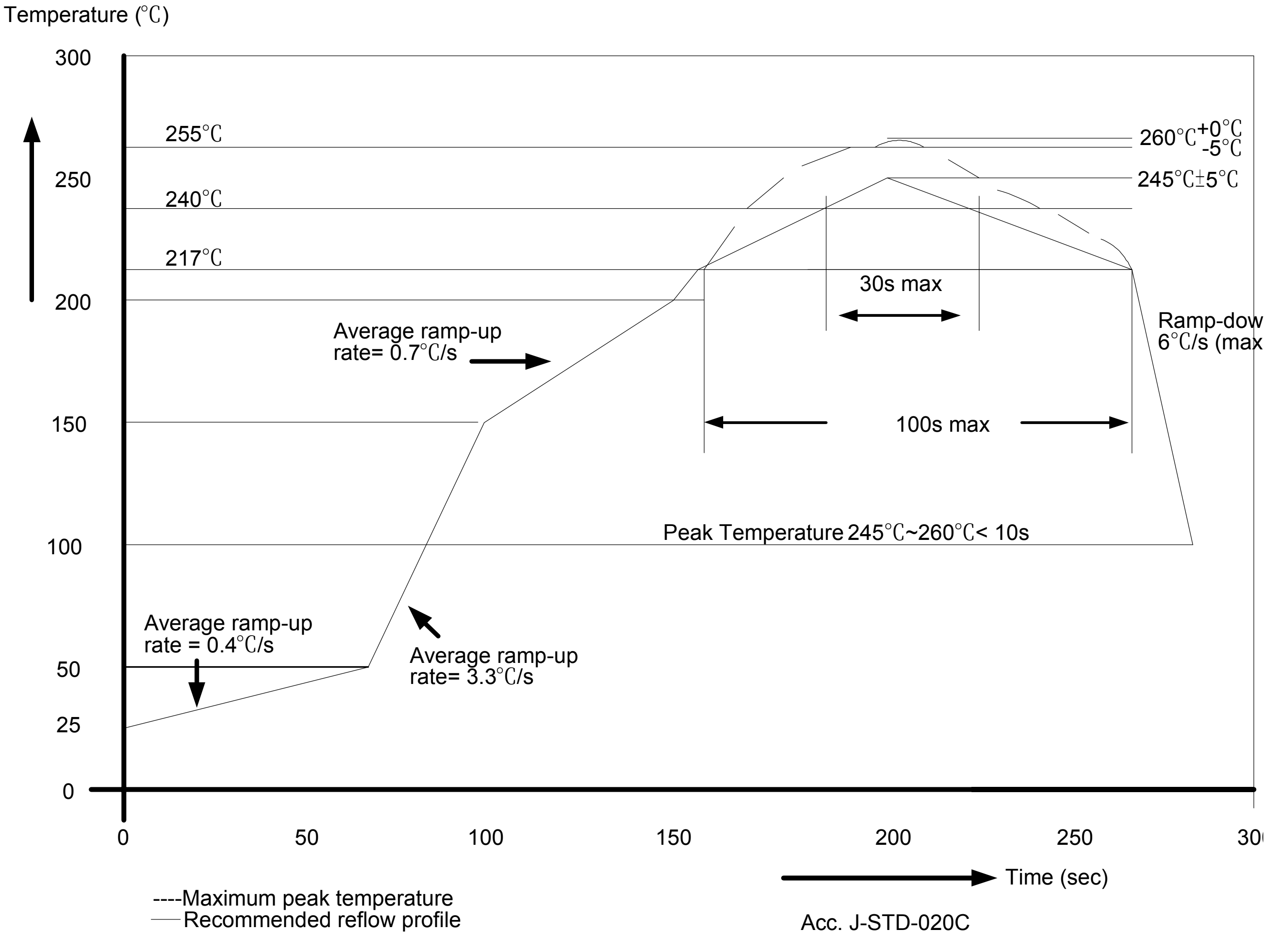
The 6 bits (bit 5~bit 0) of the configuration register are set to 6’b110000.

Staggered Delay of Output

MBI5045 has a built-in staggered circuit to perform delay mechanism. Among output ports exist a graduated 5ns delay time between $\overline{\text{OUT2n}}$ and $\overline{\text{OUT2n+1}}$ by which the output ports will be divided to two groups at a different time so that the instant current from the power line will be lowered.

Soldering Process of "Pb-free & Green" Package*

Macroblock has defined "Pb-Free & Green" to mean semiconductor products that are compatible with the current RoHS requirements and selected **100% pure tin** (Sn) to provide forward and backward compatibility with both the current industry-standard SnPb-based soldering processes and higher-temperature Pb-free processes. Pure tin is widely accepted by customers and suppliers of electronic devices in Europe, Asia and the US as the lead-free surface finish of choice to replace tin-lead. Also, it is backward compatible to reflow processes which adopt tin/lead (SnPb) solder paste, pleased refer to J-STD-020C for temperature setting. However, in the whole Pb-free soldering processes and materials, 100% pure tin (Sn), will all require up to 260°C for proper soldering on boards, referring to J-STD-020C as shown below.



Package Thickness	Volume mm³ <350	Volume mm³ 350-2000	Volume mm³ ≧2000
<1.6mm	260 +0 °C	260 +0 °C	260 +0 °C
1.6mm – 2.5mm	260 +0 °C	250 +0 °C	245 +0 °C
≧2.5mm	250 +0 °C	245 +0 °C	245 +0 °C

*For details, please refer to Macroblock's "Policy on Pb-free & Green Package".

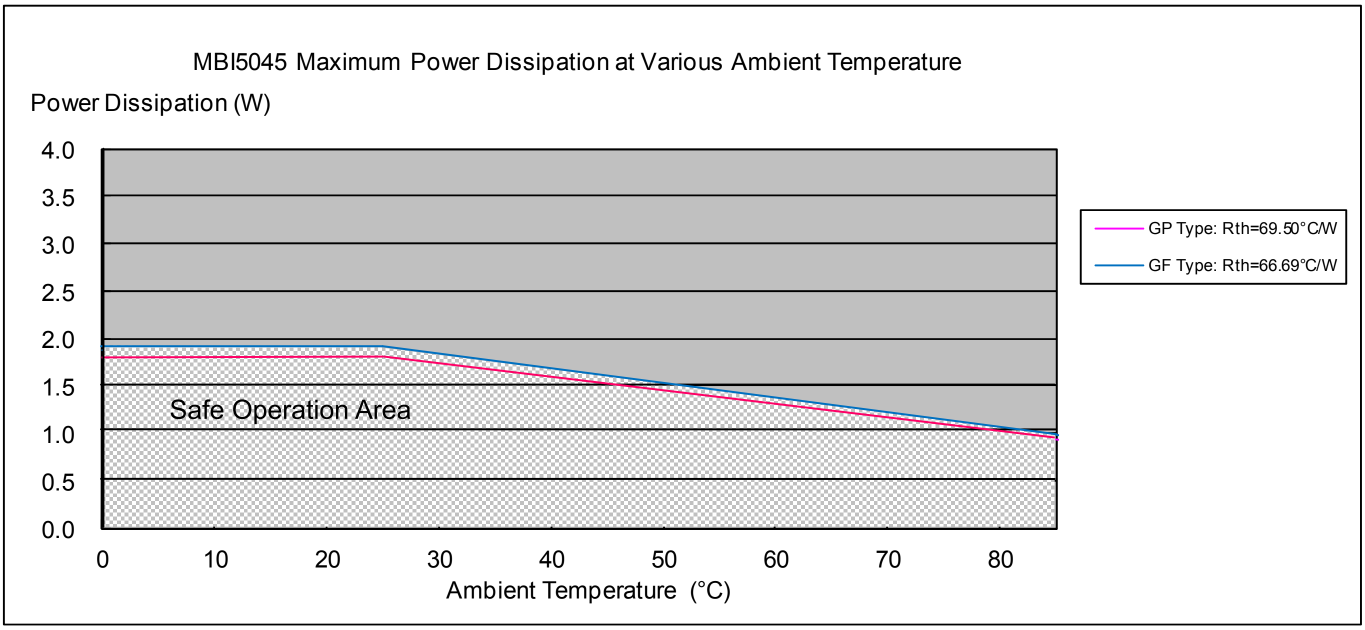
Package Power Dissipation (PD)

The maximum allowable package power dissipation is determined as $P_D(max)=(Tj–Ta)/R_{th(j-a)}$. When 16 output channels are turned on simultaneously, the actual package power dissipation is $P_D(act)=(I_{DD}xV_{DD})+(I_{OUT}xDutyxV_{DS}x16)$. Therefore, to keep $P_D(act)≤P_D(max)$, the allowable maximum output current as a function of duty cycle is:

$I_{OUT}=\{[(Tj–Ta)/R_{th(j-a)}]–(I_{DD}xV_{DD})\}/V_{DS}$ /Duty/16, where Tj=150°C.

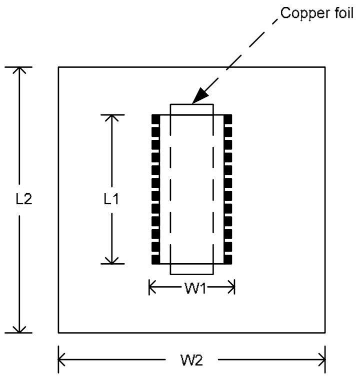
Device Type	$R_{th(j-a)}$ (°C/W)
GF	66.69
GP	69.50

The maximum power dissipation, $P_D(max)=(Tj–Ta)/R_{th(j-a)}$, decreases as the ambient temperature increases.



Usage of Thermal Pad

The PCB area L2xW2 is 4 times of the IC's area L1xW1.The thickness of the PCB is 1.6mm, copper foil 1 Oz. The thermal pad on the IC's bottom has to be mounted on the copper foil.

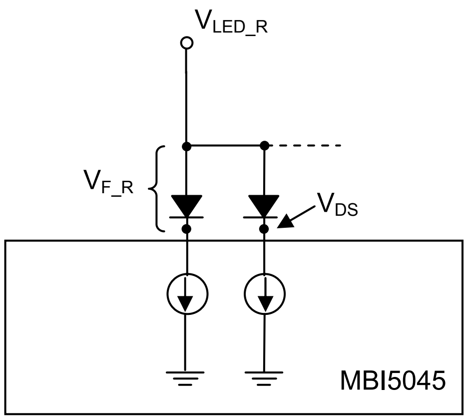


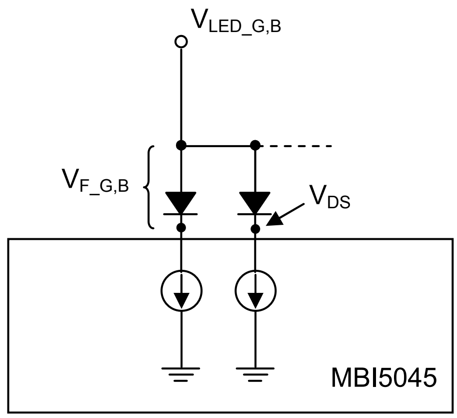
LED Supply Voltage (V_{LED})

MBI5045 are designed to operate with V_{DS} ranging from 0.2V to 0.6V (depending on I_{OUT}=2~45mA) to lower the heat dissipation and reduce the temperature on the package. In this case, it is recommended to use the lowest possible supply voltage V_{LED}. Because the V_F of red LED differs from green and blue LED, we suggest to separate V_{LED_R} from $V_{LED\_G,B}$.

$V_{DS}=V_{LED}-V_F$, with V_{DS} ranging from 0.2V to 0.6V

The applications are shown in the following figures.

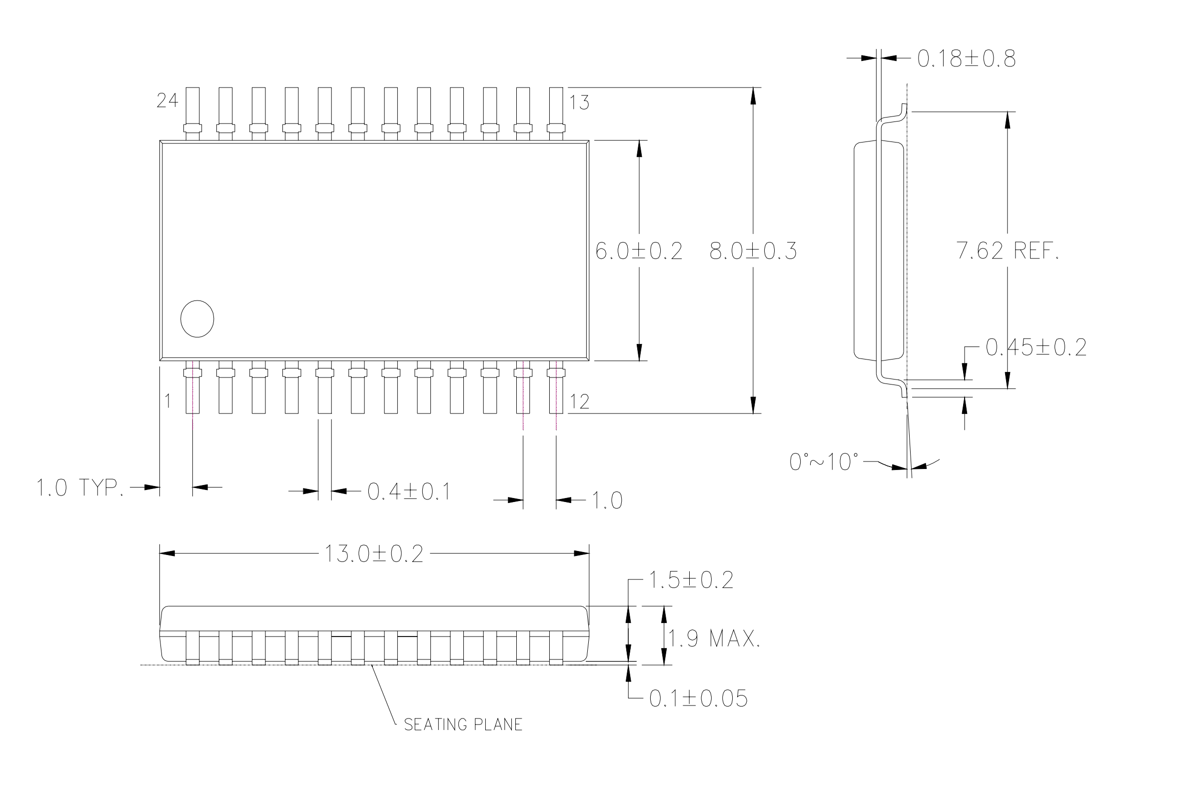




Switching Noise Reduction

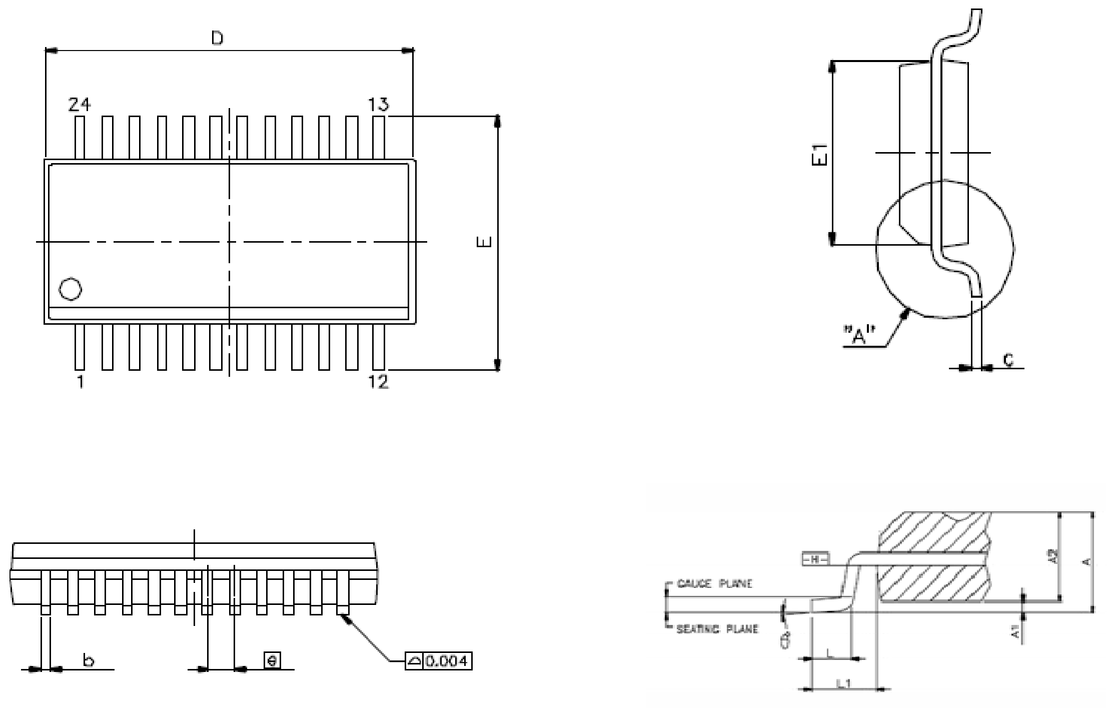
LED drivers are frequently used in switch-mode applications which always behave with switching noise due to the parasitic inductance on PCB. To eliminate switching noise, refer to "Application Note for 8-bit and 16-bit LED Drivers- Overshoot".

Package Outline



MBI5045GF Outline Drawing

Note: The unit for the outline drawing is mm.

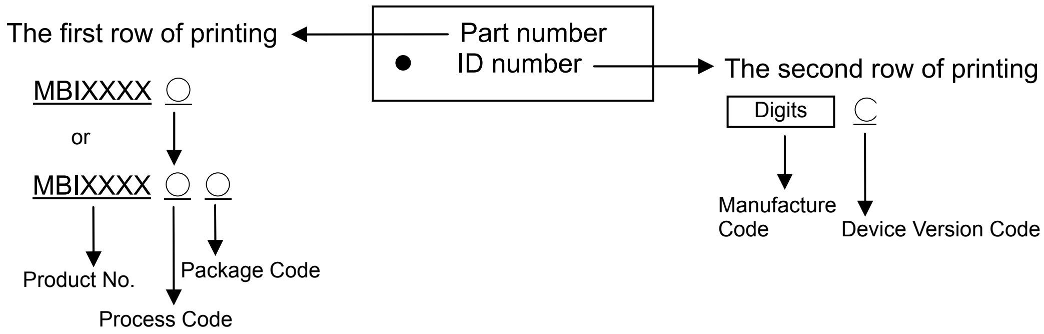


SYMBOLS	Dimensions shown in inches			Dimensions shown in millimeters		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.053	0.064	0.069	1.346	1.626	1.753
A1	0.004	0.006	0.010	0.102	0.152	0.254
A2	—	—	0.059	—	—	1.499
D	0.337	0.341	0.344	8.560	8.661	8.738
E	0.228	0.236	0.244	5.791	5.994	6.198
E1	0.150	0.154	0.157	3.810	3.912	3.988
b	0.008	—	0.012	0.203	—	0.305
c	0.007	—	0.010	0.178	—	0.254
L	0.016	0.025	0.050	0.406	0.635	1.270
e	0.025 BASIC			0.635 BASIC		
L1	0.041 BASIC			1.0414 BASIC		
Θ°	0	—	8	0	—	8

MBI5045GP Outline Drawing

Note: The unit for the outline drawing is mm.

Product Top Mark Information



Product Revision History

Advance information version	Device Version Code
V1.00	A

Product Ordering Information

Part Number	"Pb-free & Green" Package Type	Weight (g)
MBI5045GF-A	SOP24L-300-1.00	0.28
MBI5045GP-A	SSOP24L-150-0.64	0.11

*Please place your order with the ***"product ordering number"*** information on your purchase order (PO).

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