TPS782 500-nA I_Q,150-mA, Ultra-Low Quiescent Current Low-Dropout Linear Regulator

1 Features

- Low I_Q: 500 nA
- 150-mA, Low-Dropout Regulator
- Input Voltage Range: 2.2 V to 5.5 V
- Low-Dropout at 25°C, 130 mV at 150 mA
- Low-Dropout at 85°C, 175 mV at 150 mA
- 3% Accuracy Over Load, Line, and Temperature
- Stable with a 1.0-μF Ceramic Capacitor
- Thermal Shutdown and Overcurrent Protection
- CMOS Logic Level-Compatible Enable Pin
- Available in DDC (TSOT23-5) or DRV (2-mm x 2-mm SON-6) Packages

2 Applications

- TI MSP430 Attach Applications
- Wireless Handsets and Smart Phones
- MP3 Players
- Battery-Operated Handheld Products

3 Description

The TPS782 family of low-dropout regulators (LDOs) offers the benefits of ultra-low power and miniaturized packaging.

This LDO is designed specifically for battery-powered applications where ultra-low quiescent current is a critical parameter. The TPS782, with ultra-low I_Q (500 nA), is ideal for microprocessors, microcontrollers, and other battery-powered applications.

The ultra-low power and miniaturized packaging allow designers to customize power consumption for specific applications.

The TPS782 family is designed to be compatible with the TI MSP430 and other similar products. The enable pin (EN) is compatible with standard CMOS logic. This device allows for minimal board space because of miniaturized packaging and a potentially small output capacitor. The TPS782 series also features thermal shutdown and current limit to protect the device during fault conditions. All packages have an operating temperature range of T_J = –40°C to 125°C.

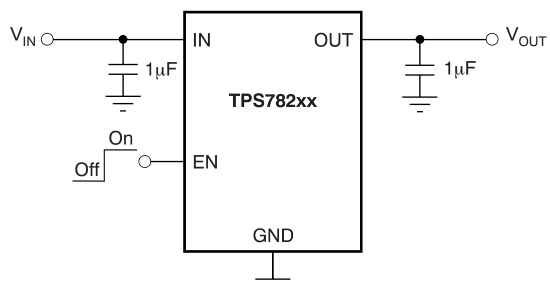
For high-performance applications that require a dual-level voltage option, consider the TPS780 series, with an I_Q of 500 nA and dynamic voltage scaling.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS782	SOT (5)	2.90 mm x 1.60 mm
	SON (6)	2.00 mm x 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (January 2014) to Revision D — **Page**

- Added *ESD Ratings* table, *Thermal Information* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Changed document format to latest data sheet standards; moved existing sections ... 1
- Changed factory programming feature bullet ... 1
- Added input voltage range feature bullet ... 1
- Changed *Applications* list ... 1
- Changed *Description* section text (all paragraphs) ... 1
- Added simplified schematic to front page ... 1
- Deleted footnotes from pin configuration drawings ... 3
- Changed pin descriptions throughout *Pin Functions* table ... 3
- Changed *operating junction temperature range* maximum value in Absolute Maximum Ratings table ... 4
- Deleted *Dissipation Ratings* table; see Thermal Information table ... 4
- Changed symbol and parameter names for clarity in *Electrical Characteristics* table ... 5

Changes from Revision B (May 2010) to Revision C — **Page**

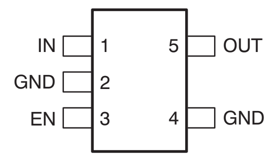
- Changed I_Q value in *Description* section from 1 µA to 500 nA ... 1

Changes from Revision A (September 2008) to Revision B — **Page**

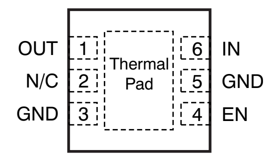
- Changed first bullet of *Features* list ... 1
- Updated title of data sheet ... 1
- Changed *ground pin current,* I_{OUT} *= 0mA* typical specification from 1.0 µA to 0.42 µA ... 5
- Added Figure 6 ... 6

5 Pin Configuration and Functions

DDC PACKAGE
TSOT23-5
(TOP VIEW)



DRV PACKAGE
2-mm x 2-mm SON-6
(TOP VIEW)



Pin Functions

PIN			I/O	DESCRIPTION
NAME	DRV	DDC		
OUT	1	5	O	Regulated output voltage pin. A small (1-µF) ceramic capacitor is needed from this pin to ground to assure stability. See the *Input and Output Capacitor Requirements* in the *Application and Implementation* section for more details.
NC	2	—	—	No internal connection.
EN	4	3	I	Enable pin. Drive this pin over 1.2 V to turn on the regulator. Drive this pin below 0.4 V to put the regulator into shutdown mode, reducing operating current to 18 nA typical.
GND	3, 5	2, 4	—	Ground pin. Tie all ground pins to ground for proper operation.
IN	6	1	I	Input pin. For stable operation, place a small, 0.1-µF capacitor from this pin to ground; typical input capacitor = 1.0 µF. Tie back both input and output capacitor grounds to the IC ground, with no significant impedance between them.
Thermal pad	Thermal pad	—	—	Connect the thermal pad to ground.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Voltage	Input voltage range	–0.3	6	V
	Enable	–0.3	V_{IN} + 0.3	V
	Output voltage range	–0.3	V_{IN} + 0.3	V
Current	Maximum output current	Internally limited		A
Output short-circuit duration		Indefinite		
Total continuous power dissipation, P_{DISS}		See *Thermal Information*		
Operating junction temperature, T_J		–40	160	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	2.2		5.5	V
V_{OUT}	Output voltage	1.8		4.2	V
V_{EN}	Enable voltage	0		V_{IN}	V
I_{OUT}	Output current	0		150	mA
T_J	Junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC (1)		TPS782 DRV 6 PINS	TPS782 DDC 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	65.9	193.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	87.3	40.1	
$R_{\theta JB}$	Junction-to-board thermal resistance	35.4	34.3	
ψ_{JT}	Junction-to-top characterization parameter	1.7	0.9	
ψ_{JB}	Junction-to-board characterization parameter	35.8	34.1	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	6.1	—	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Over operating temperature range (T_J = –40°C to 125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2.2 V, whichever is greater; I_{OUT} = 100 µA, V_{EN} = V_{IN}, C_{OUT} = 1.0 µF, fixed V_{OUT} test conditions, unless otherwise noted. Typical values at T_J = 25°C.

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range				2.2		5.5	V
V_{OUT}	DC output accuracy	Nominal	T_J = 25°C		–2%	±1%	+2%	
		Over V_{IN}, I_{OUT}, temperature	$V_{OUT(nom)}$ + 0.5 V ≤ V_{IN} ≤ 5.5 V, 0 mA ≤ I_{OUT} ≤ 150 mA		–3%	±2%	3%	
$\Delta V_{OUT(\Delta VIN)}$	Line regulation		$V_{OUT(nom)}$ + 0.5 V ≤ V_{IN} ≤ 5.5 V, I_{OUT} = 5 mA			±1%		
$\Delta V_{OUT(\Delta IOUT)}$	Load regulation		0 mA ≤ I_{OUT} ≤ 150 mA			±2%		
V_{DO}	Dropout voltage(1)		V_{IN} = 95% $V_{OUT(nom)}$, I_{OUT} = 150 mA			130	250	mV
I_{LIM}	Output current limit		V_{OUT} = 0.90 × $V_{OUT(nom)}$		150	230	400	mA
I_{GND}	Ground pin current		I_{OUT} = 0 mA			0.42	1.3	µA
			I_{OUT} = 150 mA			8		µA
I_{EN}	EN pin current		V_{EN} = 5.5V				40	nA
I_{SHDN}	Shutdown current (I_{GND})		V_{EN} ≤ 0.4 V, 2.2 V ≤ V_{IN} < 5.5 V, T_J = –40°C to 100°C			18	130	nA
PSRR	Power-supply rejection ratio		V_{IN} = 4.3 V, V_{OUT} = 3.3 V, I_{OUT} = 150 mA	f = 10 Hz		40		dB
				f = 100 Hz		20		dB
				f = 1 kHz		15		dB
V_n	Output noise voltage		BW = 100 Hz to 100 kHz, V_{IN} = 3.2 V, V_{OUT} = 2.7 V, I_{OUT} = 1 mA			108		μV_{RMS}
t_{STR}	Startup time(2)		C_{OUT} = 1.0 µF, V_{OUT} = 10% $V_{OUT(nom)}$ to V_{OUT} = 90% $V_{OUT(nom)}$			500		µs
t_{SHDN}	Shutdown time(3)		I_{OUT} = 150 mA, C_{OUT} = 1.0 µF, V_{OUT} = 2.8 V, V_{OUT} = 90% $V_{OUT(nom)}$ to V_{OUT} = 10% $V_{OUT(nom)}$			500(4)		µs
T_{sd}	Thermal shutdown temperature		Shutdown, temperature increasing			160		°C
			Reset, temperature decreasing			140		°C
T_J	Operating junction temperature				–40		125	°C

(1) V_{DO} is not measured for devices with $V_{OUT(nom)}$ ≤ 2.3 V because minimum V_{IN} = 2.2 V.
(2) Time from V_{EN} = 1.2 V to V_{OUT} = 90% ($V_{OUT(nom)}$).
(3) Time from V_{EN} = 0.4 V to V_{OUT} = 10% ($V_{OUT(nom)}$).
(4) See *Shutdown* in the *Feature Description* section for more details.

6.6 Typical Characteristics

Over the operating temperature range of T_J = –40°C to 125°C, V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2.2 V, whichever is greater; I_{OUT} = 100 µA, V_{EN} = V_{IN}, C_{OUT} = 1 µF, and C_{IN} = 1 µF, unless otherwise noted.

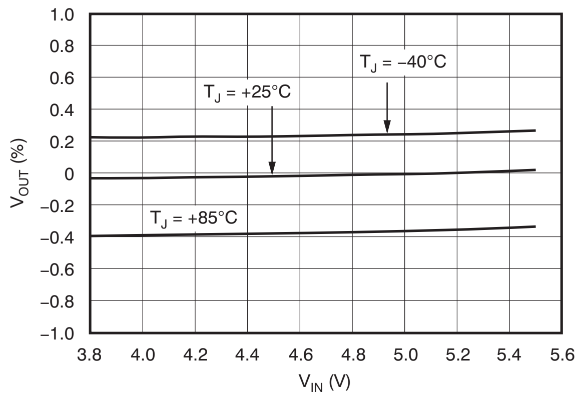


Figure 1. Line Regulation, I_{OUT} = 5 mA, TPS78227

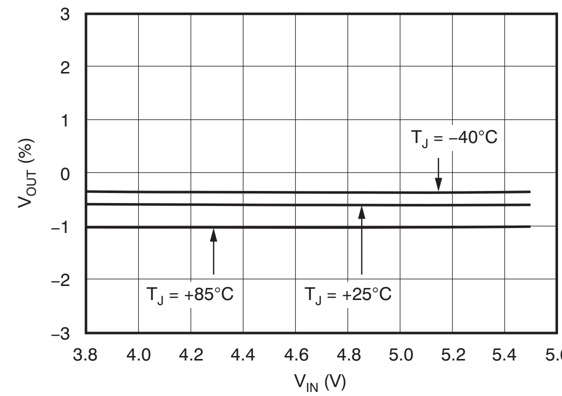


Figure 2. Line Regulation, I_{OUT} = 150 mA, TPS78227

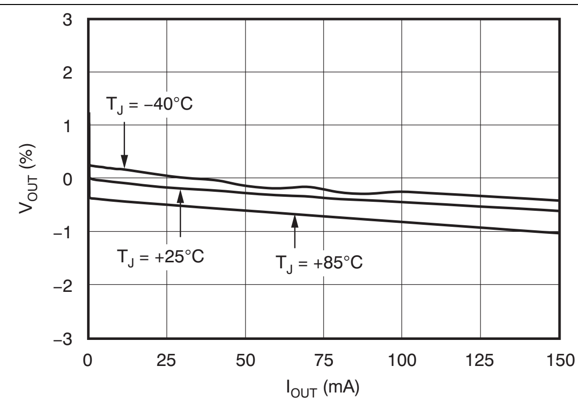


Figure 3. Load Regulation, V_{IN} = 3.8 V, TPS78227

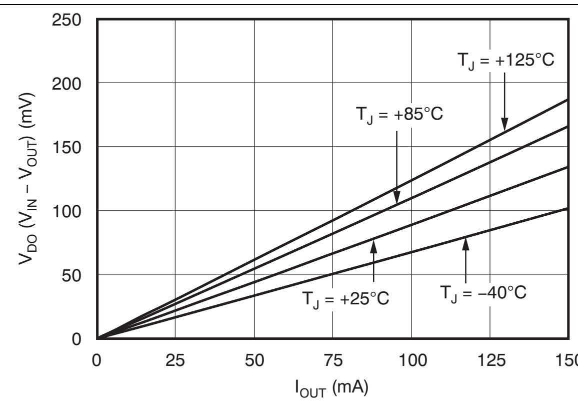


Figure 4. Dropout Voltage vs Output Current, V_{IN} = 0.95 × $V_{OUT(nom)}$, TPS78227

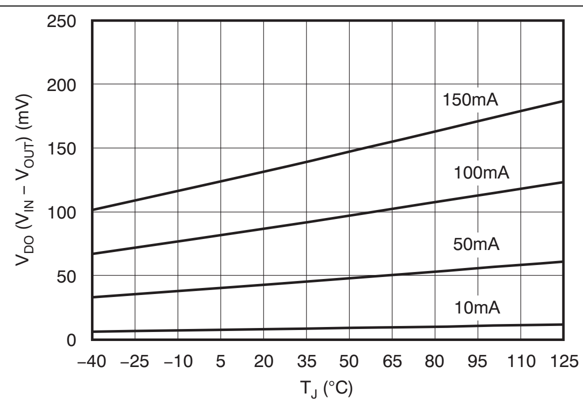


Figure 5. Dropout Voltage vs Junction Temperature, V_{IN} = 0.95 × $V_{OUT(nom)}$, TPS78227

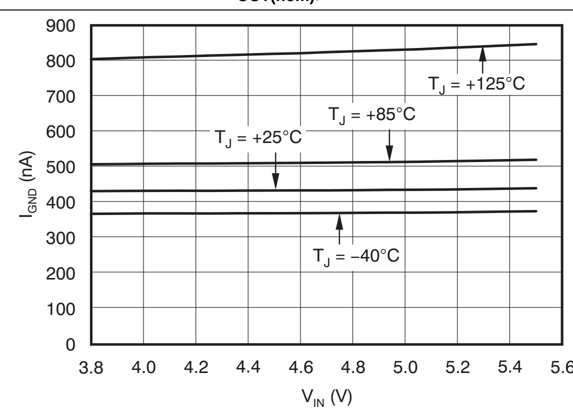


Figure 6. Ground Pin Current vs Input Voltage, I_{OUT} = 0 mA, TPS78233

Typical Characteristics (continued)

Over the operating temperature range of T_J = –40°C to 125°C, V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2.2 V, whichever is greater; I_{OUT} = 100 µA, V_{EN} = V_{IN}, C_{OUT} = 1 µF, and C_{IN} = 1 µF, unless otherwise noted.

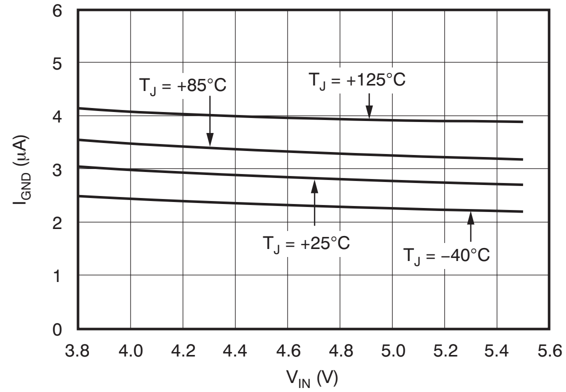


Figure 7. Ground Pin Current vs Input Voltage, I_{OUT} = 50 mA, TPS78227

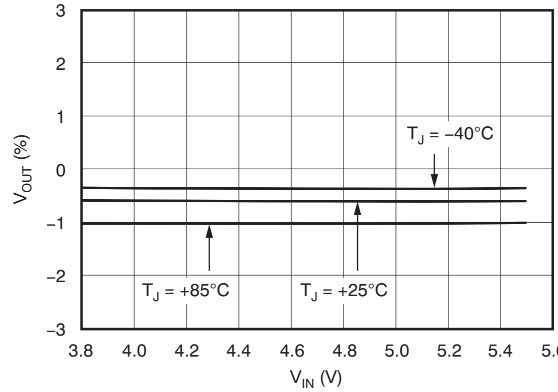


Figure 8. Ground Pin Current vs Input Voltage, I_{OUT} = 150 mA, TPS78227

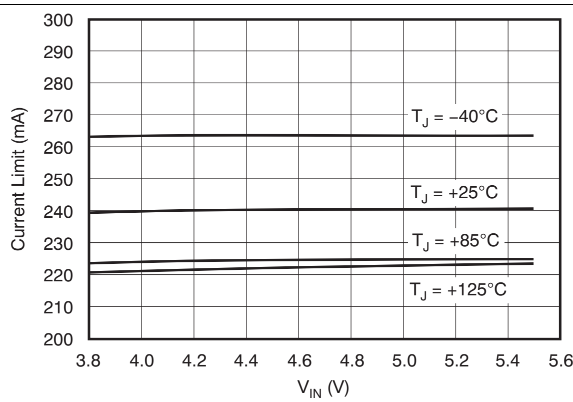


Figure 9. Current Limit vs Input Voltage, V_{OUT} = 95% $V_{OUT(nom)}$, TPS78227

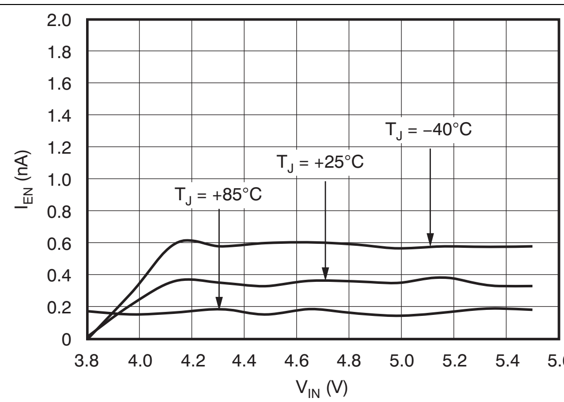


Figure 10. Enable Pin Current vs Input Voltage, I_{OUT} = 100 µA, TPS78227

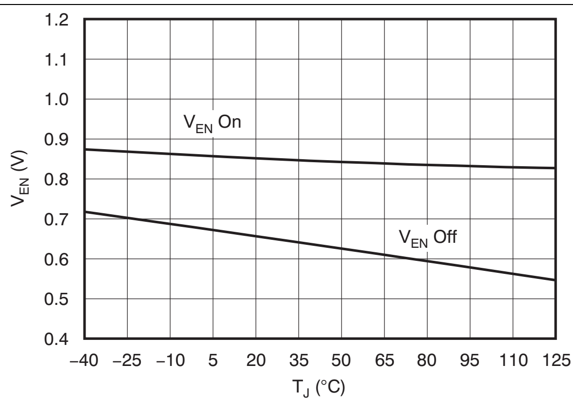


Figure 11. Enable Pin Hysteresis vs Junction Temperature, I_{OUT} = 1 mA, TPS78227

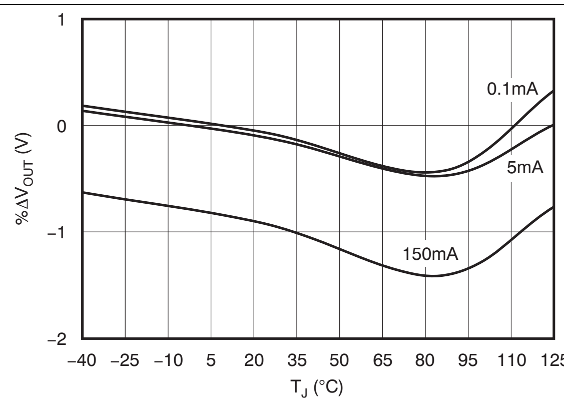


Figure 12. %ΔV_{OUT} vs Junction Temperature, V_{IN} = 3.3 V, TPS78227

Typical Characteristics (continued)

Over the operating temperature range of T_J = –40°C to 125°C, V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2.2 V, whichever is greater; I_{OUT} = 100 μA, V_{EN} = V_{IN}, C_{OUT} = 1 μF, and C_{IN} = 1 μF, unless otherwise noted.

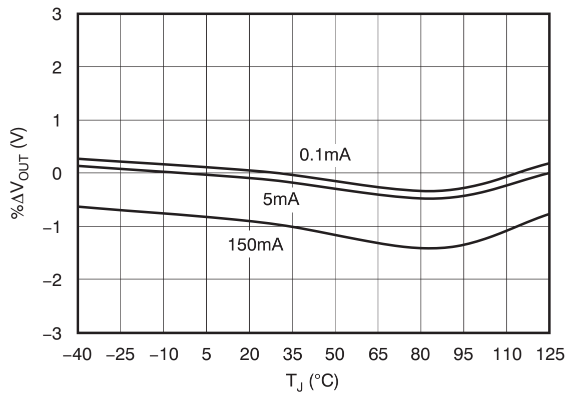


Figure 13. %ΔV_{OUT} vs Junction Temperature, V_{IN} = 3.7 V, TPS78227

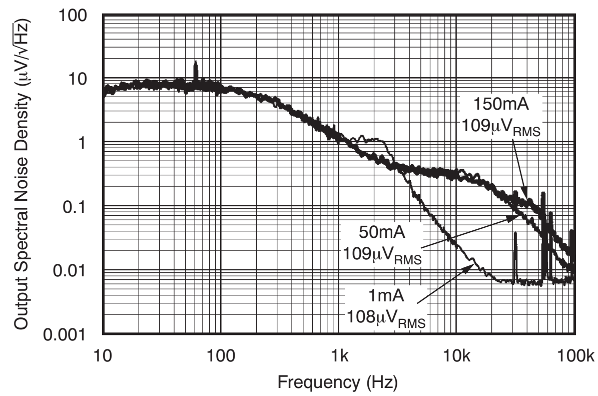


Figure 14. Output Spectral Noise Density vs Frequency, C_{IN} = 1 μF, C_{OUT} = 2.2 μF, V_{IN} = 3.2 V, TPS78227

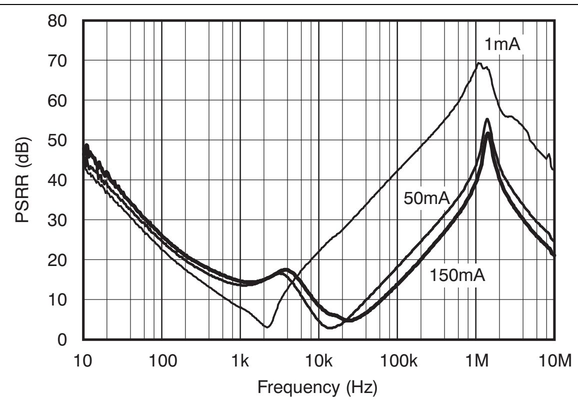


Figure 15. Ripple Rejection vs Frequency, V_{IN} = 4.2 V, V_{OUT} = 2.7 V, C_{OUT} = 2.2 μF, TPS78227

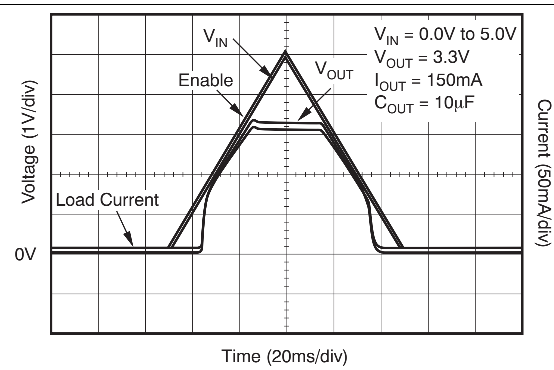


Figure 16. Input Voltage Ramp vs Output Voltage, TPS78233

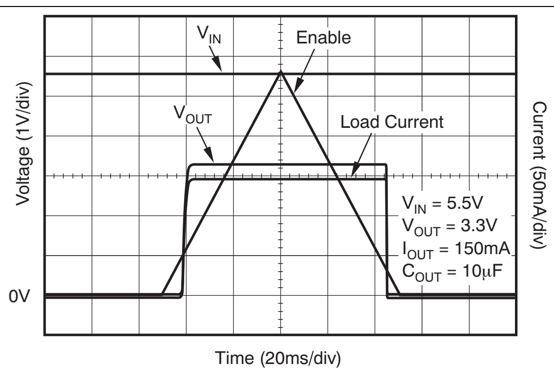


Figure 17. Output Voltage vs Enable (Slow Ramp), TPS78233

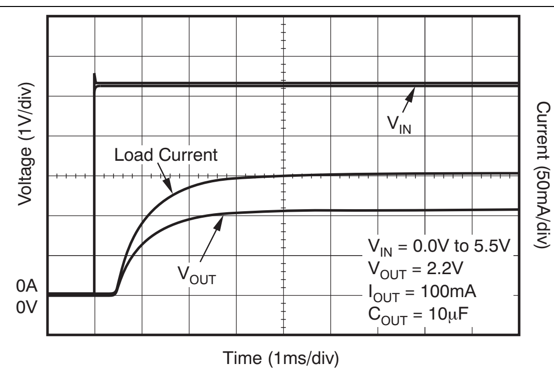


Figure 18. Input Voltage vs Delay to Output, TPS78222

Typical Characteristics (continued)

Over the operating temperature range of T_J = –40°C to 125°C, V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2.2 V, whichever is greater; I_{OUT} = 100 µA, V_{EN} = V_{IN}, C_{OUT} = 1 µF, and C_{IN} = 1 µF, unless otherwise noted.

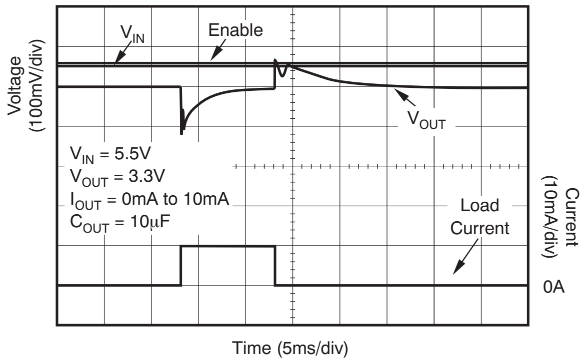


Figure 19. Load Transient Response, TPS78233

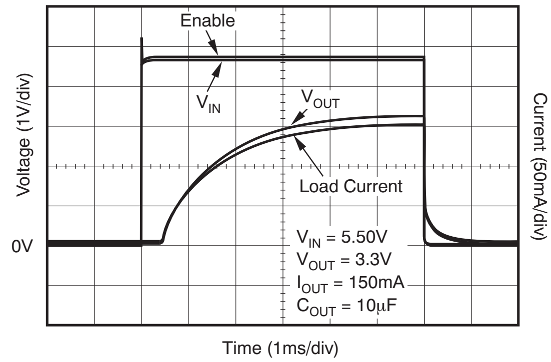


Figure 20. Enable Pin vs Output Voltage Response and Output Current, TPS78233

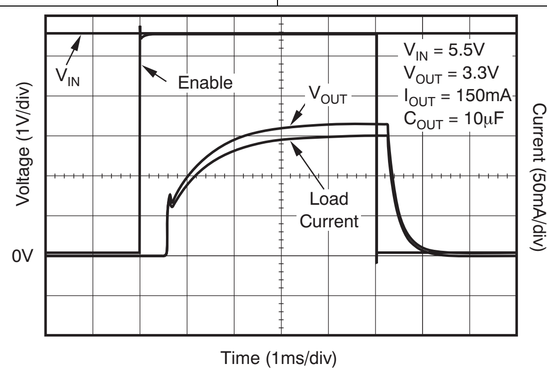


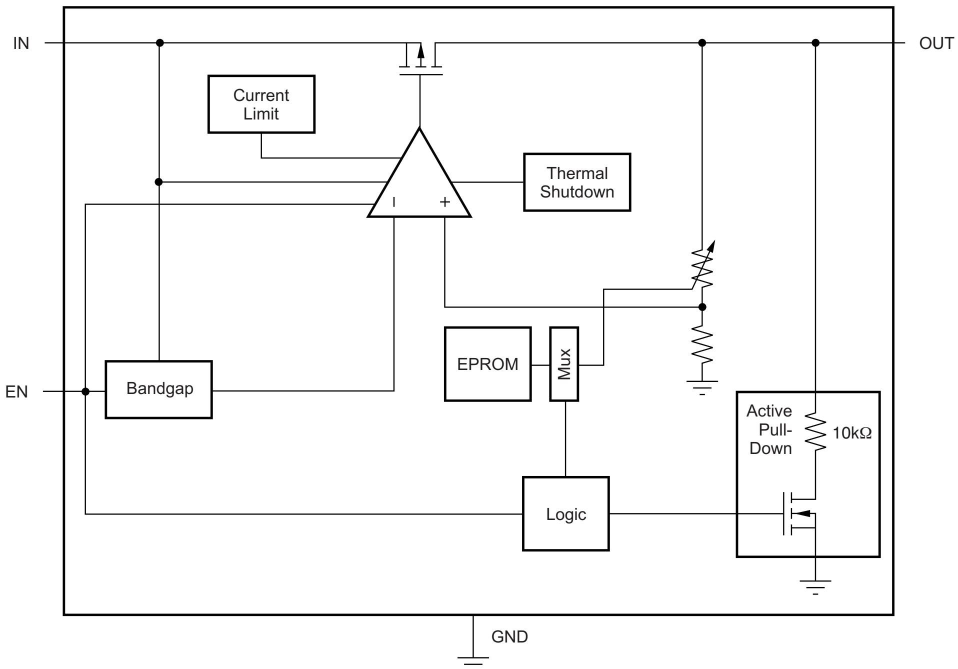
Figure 21. Enable Pin vs Output Voltage Delay, TPS78233

7 Detailed Description

7.1 Overview

The TPS782 family of low-dropout regulators (LDOs) is designed specifically for battery-powered applications where ultralow quiescent current is a critical parameter. The TPS782 family is compatible with the TI MSP430 and other similar products. The enable pin (EN) is compatible with standard CMOS logic. This LDO family is stable with any output capacitor greater than 1.0 µF.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Internal Current Limit

The TPS782 is internally current-limited to protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of output voltage. For reliable operation, the device should not be operated in a current limit state for extended periods of time.

The PMOS pass element in the TPS782 series has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting to 5% of rated output current may be appropriate.

7.3.2 Active V_{OUT} Pulldown

In the TPS782 series, the active pulldown discharges V_{OUT} when the device is off. However, the input voltage must be greater than 2.2 V for the active pulldown to work.

Feature Description (continued)

7.3.3 Shutdown

The enable pin (EN) is active high and is compatible with standard and low-voltage CMOS levels. When shutdown capability is not required, EN should be connected to the IN pin, as shown in Figure 22. The TPS782 series, with internal active output pulldown circuitry, discharges the output to within 5% V_{OUT} with a time (t) shown in Equation 1:

$$t = 3\left(\frac{10k\Omega \times R_L}{10k\Omega + R_L}\right) \times C_{OUT} \quad (1)$$

Where:

R_L= output load resistance

C_{OUT} = output capacitance

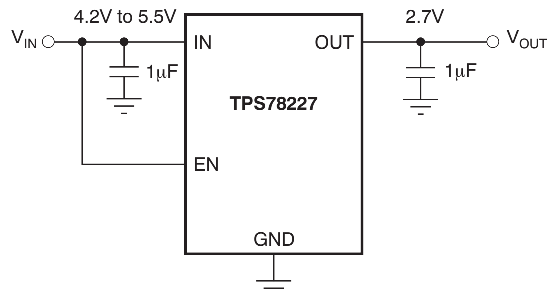


Figure 22. Circuit Showing EN Tied High When Shutdown Capability Is Not Required

7.4 Device Functional Modes

Table 1 provides a quick comparison between the normal, dropout, and disabled modes of operation.

Table 1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	EN	I_{OUT}	T_J
Normal	$V_{IN} > V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{LIM}$	$T_J < T_{SD}$
Dropout	$V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{LIM}$	$T_J < T_{SD}$
Disabled	—	$V_{EN} < V_{EN(LO)}$	—	$T_J > T_{SD}$

7.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$).
- The enable voltage has previously exceeded the enable rising threshold voltage and not yet decreased below the enable falling threshold.
- The output current is less than the current limit ($I_{OUT} < I_{LIM}$).
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD}$).

7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass device is in a triode state and no longer controls the current through the LDO. Line or load transients in dropout can result in large output-voltage deviations.

7.4.3 Disabled

The device is disabled under the following conditions:

- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold.
- The device junction temperature is greater than the thermal shutdown temperature ($T_J > T_{SD}$).

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS782 family of LDOs is factory-programmable to have a fixed output. Note that during startup or steady-state conditions, it is important that the EN pin voltage never exceed V_{IN} + 0.3V.

8.2 Typical Application

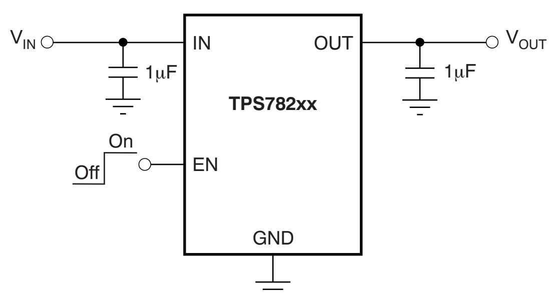


Figure 23. Typical Application Circuit

8.2.1 Design Requirements

Select the desired device based on the output voltage.

Provide an input supply with adequate headroom to account for dropout and output current to account for the GND pin current, and power the load. Select input and output capacitors based on application needs.

8.2.2 Detailed Design Procedure

8.2.2.1 Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, it is good analog design practice to connect a 0.1-μF to 1.0-μF low equivalent series resistance (ESR) capacitor across the input supply near the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated, or if the device is not located near the power source. If source impedance is not sufficiently low, a 0.1-μF input capacitor may be necessary to ensure stability.

The TPS782 series is designed to be stable with standard ceramic capacitors with values of 1.0 μF or larger at the output. X5R- and X7R-type capacitors are best because they have minimal variation in value and ESR over temperature. Maximum ESR should be less than 1.0 Ω. With tolerance and dc bias effects, the minimum capacitance to ensure stability is 1 μF.

Typical Application (continued)

8.2.2.2 Dropout Voltage

The TPS782 uses a PMOS pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass device is the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} approximately scales with output current because the PMOS device behaves like a resistor in dropout. As with any linear regulator, PSRR and transient response are degraded as (V_{IN} – V_{OUT}) approaches dropout. This effect is shown in the *Typical Characteristics* section. Refer to application report SLVA207, *Understanding LDO Dropout*, available for download from www.ti.com.

8.2.2.3 Transient Response

As with any regulator, increasing the size of the output capacitor reduces over/undershoot magnitude but increases duration of the transient response. For more information, see Figure 19.

8.2.2.4 Minimum Load

The TPS782 series is stable with no output load. Traditional PMOS LDO regulators suffer from lower loop gain at very light output loads. The TPS782 employs an innovative, low-current circuit under very light or no-load conditions, resulting in improved output voltage regulation performance down to zero output current. See Figure 19 for the load transient response.

8.2.3 Application Curves

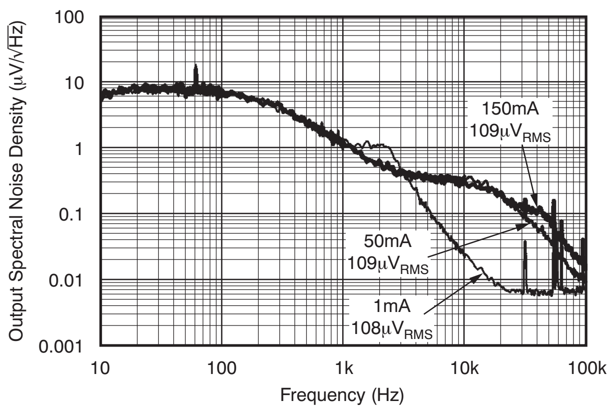


Figure 24. Output Spectral Noise Density vs Frequency, C_{IN} = 1 µF, C_{OUT} = 2.2 µF, V_{IN} = 3.2 V, TPS78227

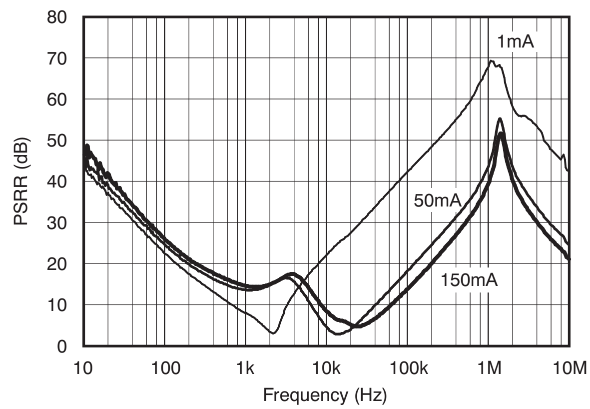


Figure 25. Ripple Rejection vs Frequency, V_{IN} = 4.2 V, V_{OUT} = 2.7 V, C_{OUT} = 2.2 µF, TPS78227

8.3 Do's and Don'ts

Do place at least one 1-µF ceramic capacitor as close as possible to the OUT pin of the regulator.

Do not place the output capacitor more than 10 mm away from the regulator.

Do connect a 0.1-µF to 1.0-µF low equivalent series resistance (ESR) capacitor across the IN pin and GND of the regulator.

Do not exceed the absolute maximum ratings.

9 Power Supply Recommendations

For best performance, connect a low-output impedance power supply directly to the IN pin of the TPS782 series. Inductive impedances between the input supply and the IN pin create significant voltage excursions at the IN pin during startup or load transient events. If inductive impedances are unavoidable, use an input capacitor.

10 Layout

10.1 Layout Guidelines

To improve ac performance (such as PSRR, output noise, and transient response), it is recommended that the printed circuit board (PCB) be designed with separate ground planes for V_{IN} and V_{OUT}, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor should connect directly to the GND pin of the device. High ESR capacitors may degrade PSRR.

10.2 Layout Example

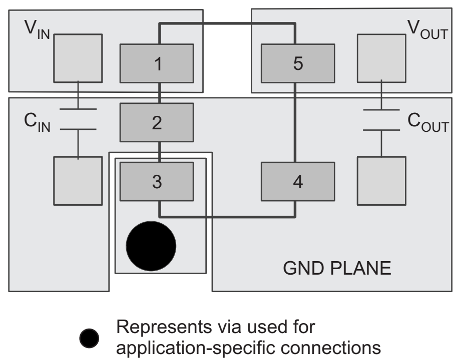


Figure 26. Layout Example for DDC Package

10.3 Thermal Protection

Thermal protection disables the device output when the junction temperature rises to approximately 160°C, allowing the device to cool. Once the junction temperature cools to approximately 140°C, the output circuitry is enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off again. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to 125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least 35°C above the maximum expected ambient condition of your particular application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS782 series has been designed to protect against overload conditions. However, it is not intended to replace proper heatsinking. Continuously running the TPS782 series into thermal shutdown degrades device reliability.

10.4 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low- and high-K boards are given in the *Thermal Information* table. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves the heatsink effectiveness. Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) is equal to the product of the output current times the voltage drop across the output pass element (V_{IN} to V_{OUT}), as shown in Equation 2:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (2)$$

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Evaluation Modules

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TPS782. The TPS782xxEVM evaluation modules (and related user guide) can be requested at the Texas Instruments website through the product folders or purchased directly from the TI eStore.

11.1.1.2 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TPS782 family is available through the product folders under *Simulation Models*.

11.1.2 Device Nomenclature

Table 2. Device Nomenclature(1)

PRODUCT	V_{OUT}
TPS782**xx*yyyz***	**XX** is the nominal output voltage **YYY** is the package designator. **Z** is the tape and reel quantity (R = 3000, T = 250).

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:
- Application report. *Understanding LDO Dropout*, SLVA207
- Product information. *Low-power MCUs*, MSP430
- Reference design.*Water Meter Implementation with FRAM Microcontroller*, TIDU517

11.3 Trademarks

All trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS78218DDCR	ACTIVE	SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SJY	Samples
TPS78218DDCT	ACTIVE	SOT	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SJY	Samples
TPS78218DRVR	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SAF	Samples
TPS78218DRVT	ACTIVE	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SAF	Samples
TPS78222DRVR	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	RAR	Samples
TPS78222DRVT	ACTIVE	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	RAR	Samples
TPS78223DDCR	ACTIVE	SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	NXM	Samples
TPS78223DDCT	ACTIVE	SOT	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	NXM	Samples
TPS78225DDCR	ACTIVE	SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CVD	Samples
TPS78225DDCRG4	ACTIVE	SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CVD	Samples
TPS78225DDCT	ACTIVE	SOT	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CVD	Samples
TPS78225DDCTG4	ACTIVE	SOT	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CVD	Samples
TPS78225DRVR	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CVD	Samples
TPS78225DRVT	ACTIVE	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CVD	Samples
TPS78225DRVTG4	ACTIVE	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CVD	Samples
TPS78227DDCR	ACTIVE	SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CVE	Samples
TPS78227DDCRG4	ACTIVE	SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CVE	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS78227DDCT	ACTIVE	SOT	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CVE	Samples
TPS78227DDCTG4	ACTIVE	SOT	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CVE	Samples
TPS78227DRVR	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CVE	Samples
TPS78227DRVT	ACTIVE	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CVE	Samples
TPS78227DRVTG4	ACTIVE	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CVE	Samples
TPS78228DDCR	ACTIVE	SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CVF	Samples
TPS78228DDCRG4	ACTIVE	SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CVF	Samples
TPS78228DDCT	ACTIVE	SOT	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CVF	Samples
TPS78228DDCTG4	ACTIVE	SOT	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CVF	Samples
TPS78228DRVR	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CVF	Samples
TPS78228DRVRG4	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CVF	Samples
TPS78228DRVT	ACTIVE	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CVF	Samples
TPS78230DDCR	ACTIVE	SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OCK	Samples
TPS78230DDCT	ACTIVE	SOT	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OCK	Samples
TPS78230DRVR	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	ODE	Samples
TPS78230DRVT	ACTIVE	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	ODE	Samples
TPS78233DDCR	ACTIVE	SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OAH	Samples
TPS78233DDCT	ACTIVE	SOT	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OAH	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS78236DDCR	ACTIVE	SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SCE	Samples
TPS78236DDCT	ACTIVE	SOT	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SCE	Samples
TPS78236DRVR	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SCE	Samples
TPS78236DRVT	ACTIVE	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SCE	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TPS782 :

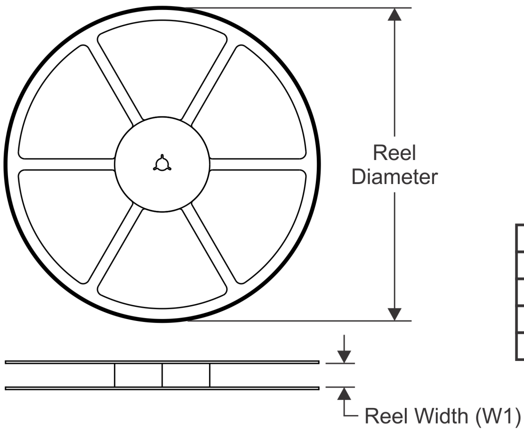
- Automotive: TPS782-Q1

NOTE: Qualified Version Definitions:

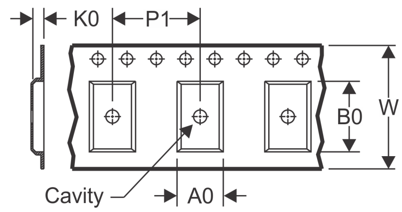
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

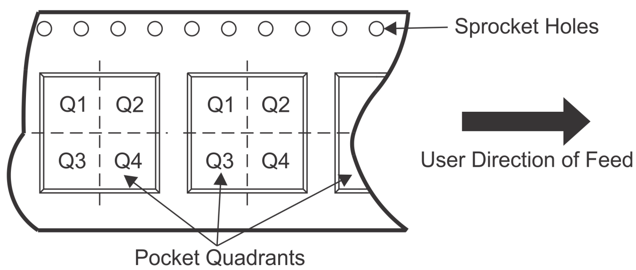


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

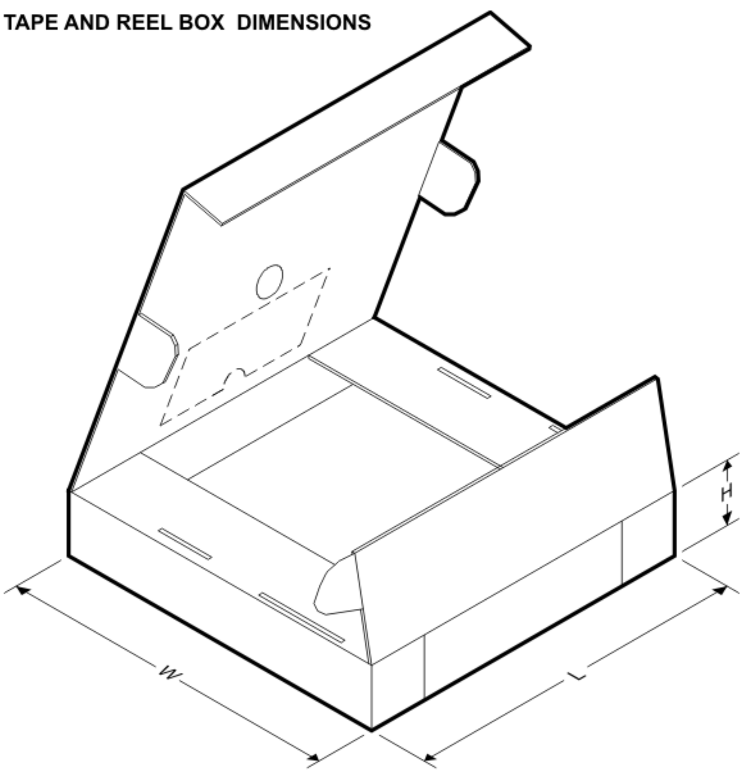


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS78218DDCR	SOT	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS78218DDCT	SOT	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS78218DRVR	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS78218DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS78222DRVR	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS78222DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS78223DDCR	SOT	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS78223DDCT	SOT	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS78225DDCR	SOT	DDC	5	3000	180.0	8.4	3.1	3.05	1.1	4.0	8.0	Q3
TPS78225DDCR	SOT	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS78225DDCT	SOT	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS78225DDCT	SOT	DDC	5	250	180.0	8.4	3.1	3.05	1.1	4.0	8.0	Q3
TPS78225DRVR	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS78225DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS78227DDCR	SOT	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS78227DDCT	SOT	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS78227DRVR	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS78227DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS78228DDCR	SOT	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS78228DDCT	SOT	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS78228DRVR	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS78228DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS78230DDCR	SOT	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS78230DDCT	SOT	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS78230DRVR	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS78230DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS78233DDCR	SOT	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS78233DDCR	SOT	DDC	5	3000	180.0	8.4	3.1	3.05	1.1	4.0	8.0	Q3
TPS78233DDCT	SOT	DDC	5	250	180.0	8.4	3.1	3.05	1.1	4.0	8.0	Q3
TPS78233DDCT	SOT	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS78236DDCR	SOT	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS78236DDCT	SOT	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS78236DRVR	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS78236DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS

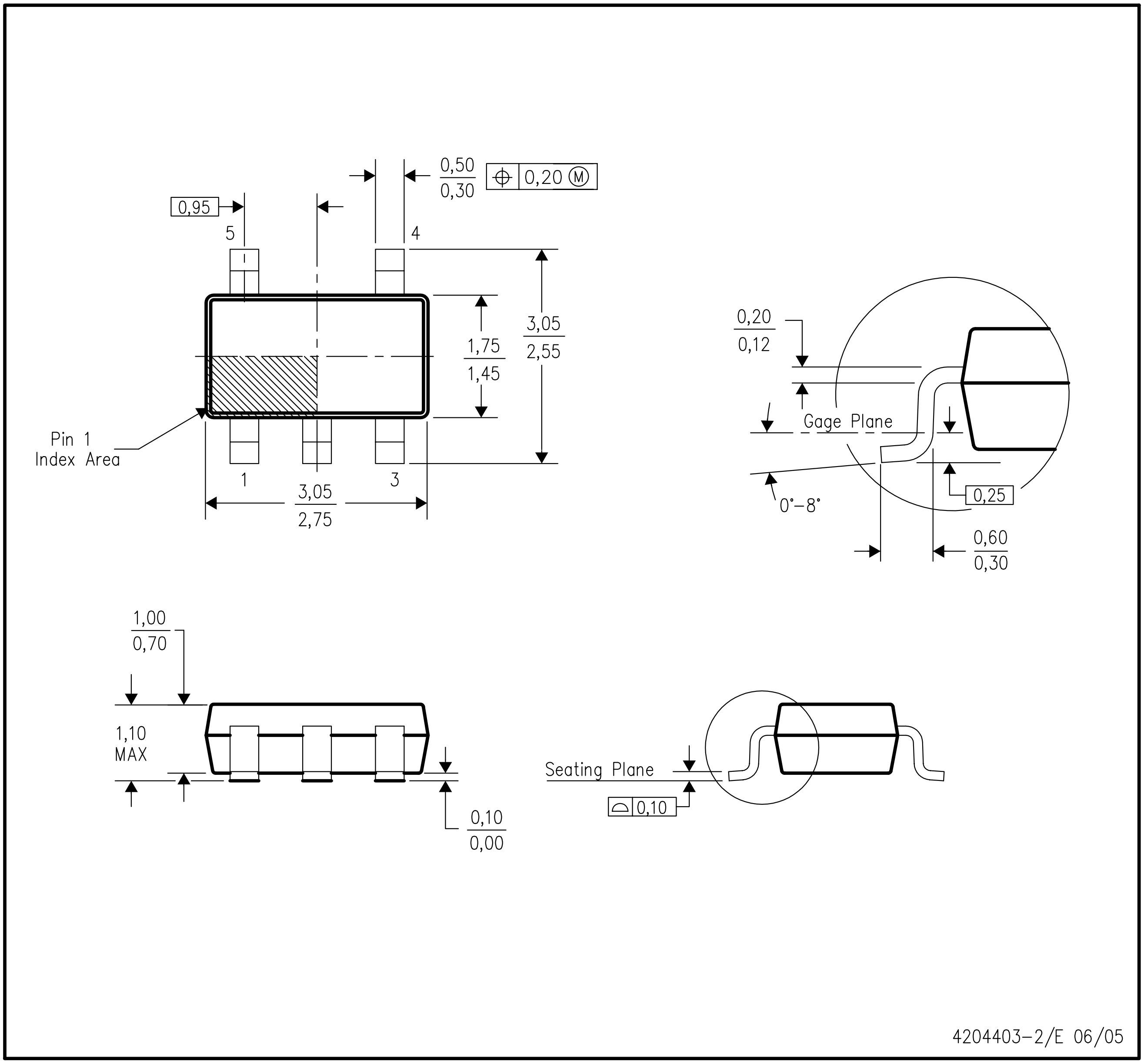


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS78218DDCR	SOT	DDC	5	3000	195.0	200.0	45.0

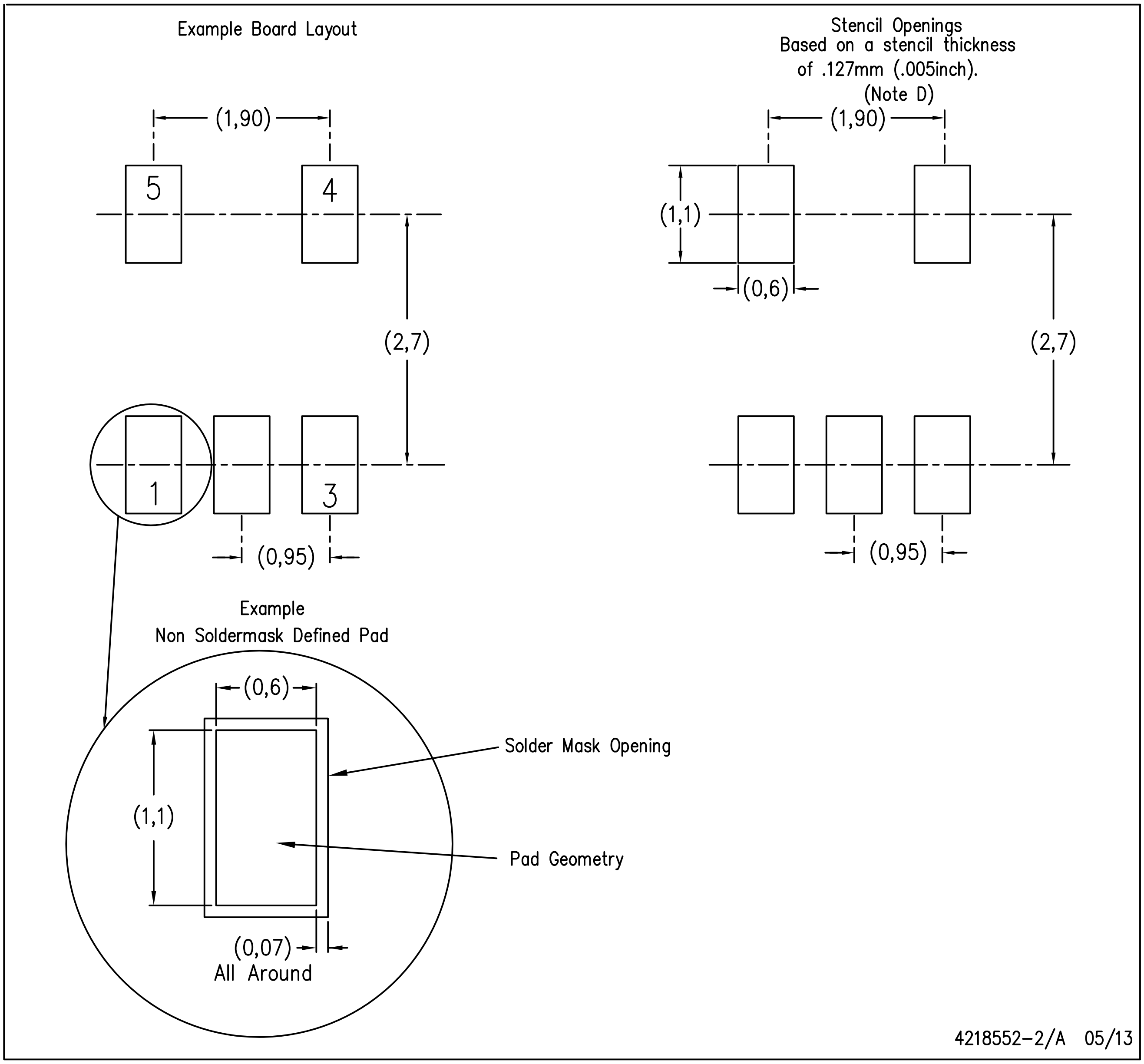
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS78218DDCT	SOT	DDC	5	250	195.0	200.0	45.0
TPS78218DRVR	WSON	DRV	6	3000	203.0	203.0	35.0
TPS78218DRVT	WSON	DRV	6	250	203.0	203.0	35.0
TPS78222DRVR	WSON	DRV	6	3000	203.0	203.0	35.0
TPS78222DRVT	WSON	DRV	6	250	203.0	203.0	35.0
TPS78223DDCR	SOT	DDC	5	3000	195.0	200.0	45.0
TPS78223DDCT	SOT	DDC	5	250	195.0	200.0	45.0
TPS78225DDCR	SOT	DDC	5	3000	223.0	270.0	35.0
TPS78225DDCR	SOT	DDC	5	3000	195.0	200.0	45.0
TPS78225DDCT	SOT	DDC	5	250	195.0	200.0	45.0
TPS78225DDCT	SOT	DDC	5	250	223.0	270.0	35.0
TPS78225DRVR	WSON	DRV	6	3000	203.0	203.0	35.0
TPS78225DRVT	WSON	DRV	6	250	203.0	203.0	35.0
TPS78227DDCR	SOT	DDC	5	3000	195.0	200.0	45.0
TPS78227DDCT	SOT	DDC	5	250	195.0	200.0	45.0
TPS78227DRVR	WSON	DRV	6	3000	203.0	203.0	35.0
TPS78227DRVT	WSON	DRV	6	250	203.0	203.0	35.0
TPS78228DDCR	SOT	DDC	5	3000	195.0	200.0	45.0
TPS78228DDCT	SOT	DDC	5	250	195.0	200.0	45.0
TPS78228DRVR	WSON	DRV	6	3000	203.0	203.0	35.0
TPS78228DRVT	WSON	DRV	6	250	203.0	203.0	35.0
TPS78230DDCR	SOT	DDC	5	3000	195.0	200.0	45.0
TPS78230DDCT	SOT	DDC	5	250	195.0	200.0	45.0
TPS78230DRVR	WSON	DRV	6	3000	203.0	203.0	35.0
TPS78230DRVT	WSON	DRV	6	250	203.0	203.0	35.0
TPS78233DDCR	SOT	DDC	5	3000	203.0	203.0	35.0
TPS78233DDCR	SOT	DDC	5	3000	223.0	270.0	35.0
TPS78233DDCT	SOT	DDC	5	250	223.0	270.0	35.0
TPS78233DDCT	SOT	DDC	5	250	203.0	203.0	35.0
TPS78236DDCR	SOT	DDC	5	3000	195.0	200.0	45.0
TPS78236DDCT	SOT	DDC	5	250	195.0	200.0	45.0
TPS78236DRVR	WSON	DRV	6	3000	203.0	203.0	35.0
TPS78236DRVT	WSON	DRV	6	250	203.0	203.0	35.0

DDC (R–PDSO–G5) PLASTIC SMALL–OUTLINE



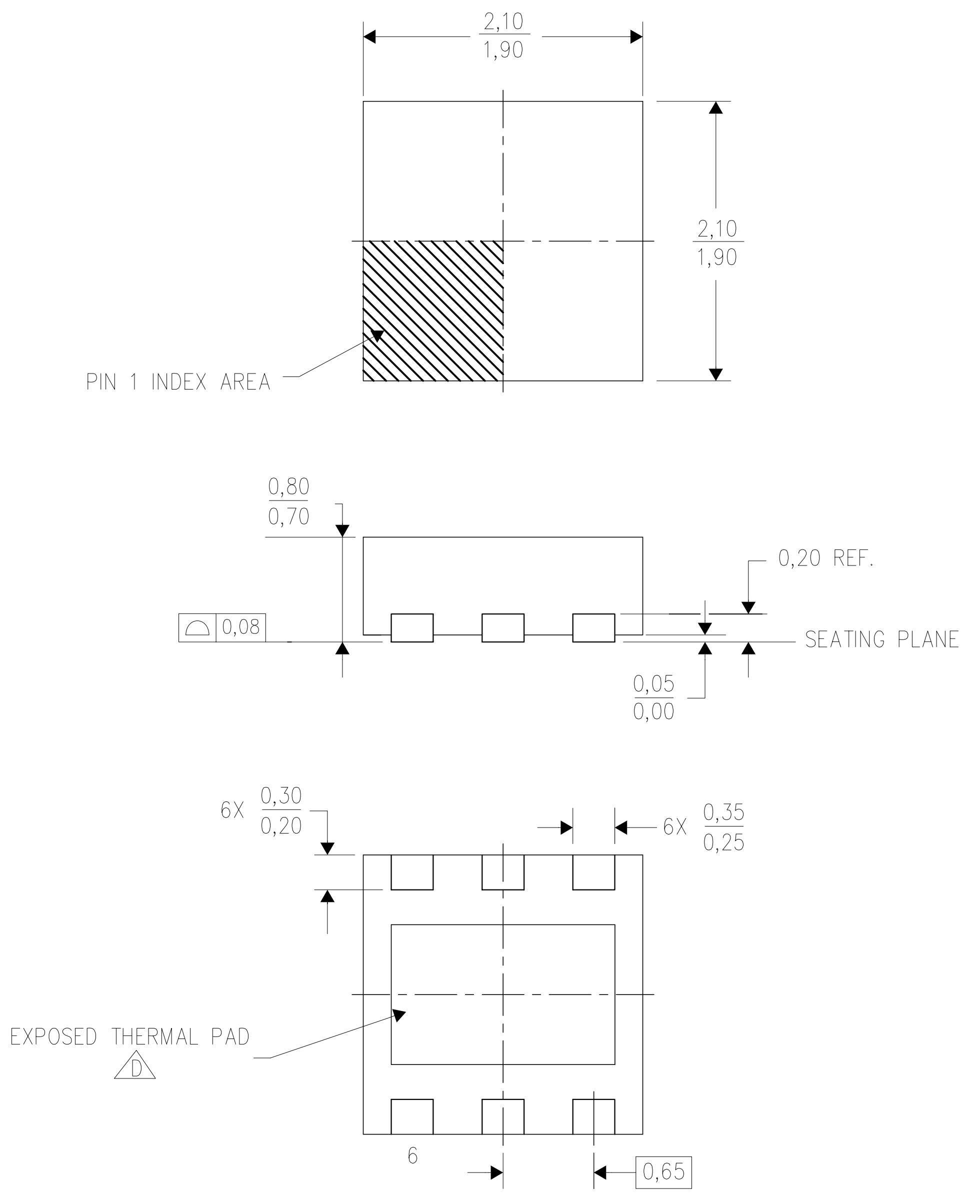
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–193 variation AB (5 pin).

DDC (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

DRV (S-PWSON-N6) PLASTIC SMALL OUTLINE NO-LEAD



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NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- B. This drawing is subject to change without notice.
- C. Small Outline No-Lead (SON) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

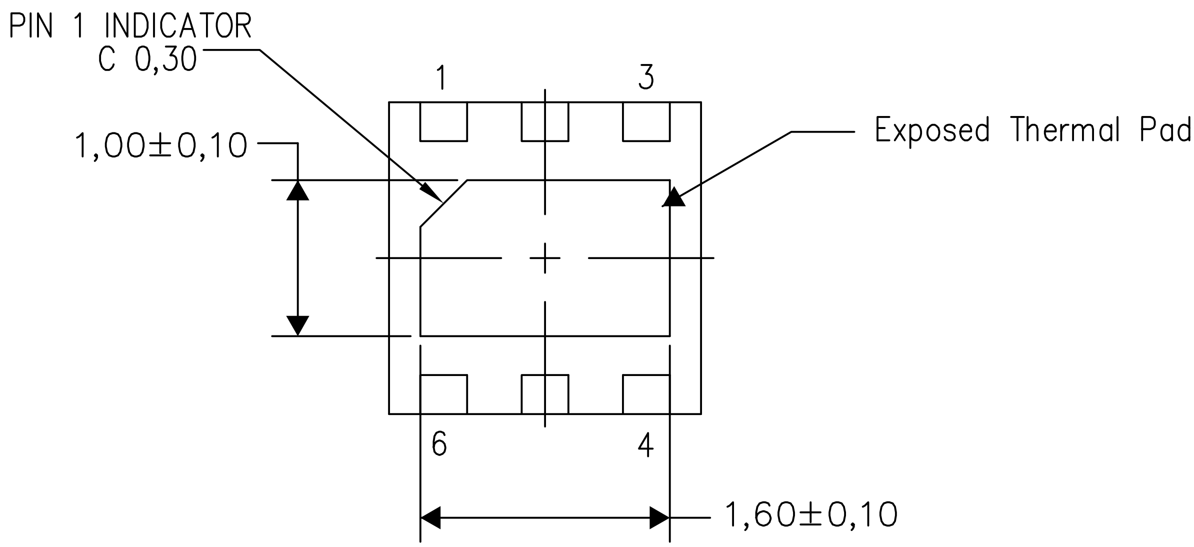
DRV (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

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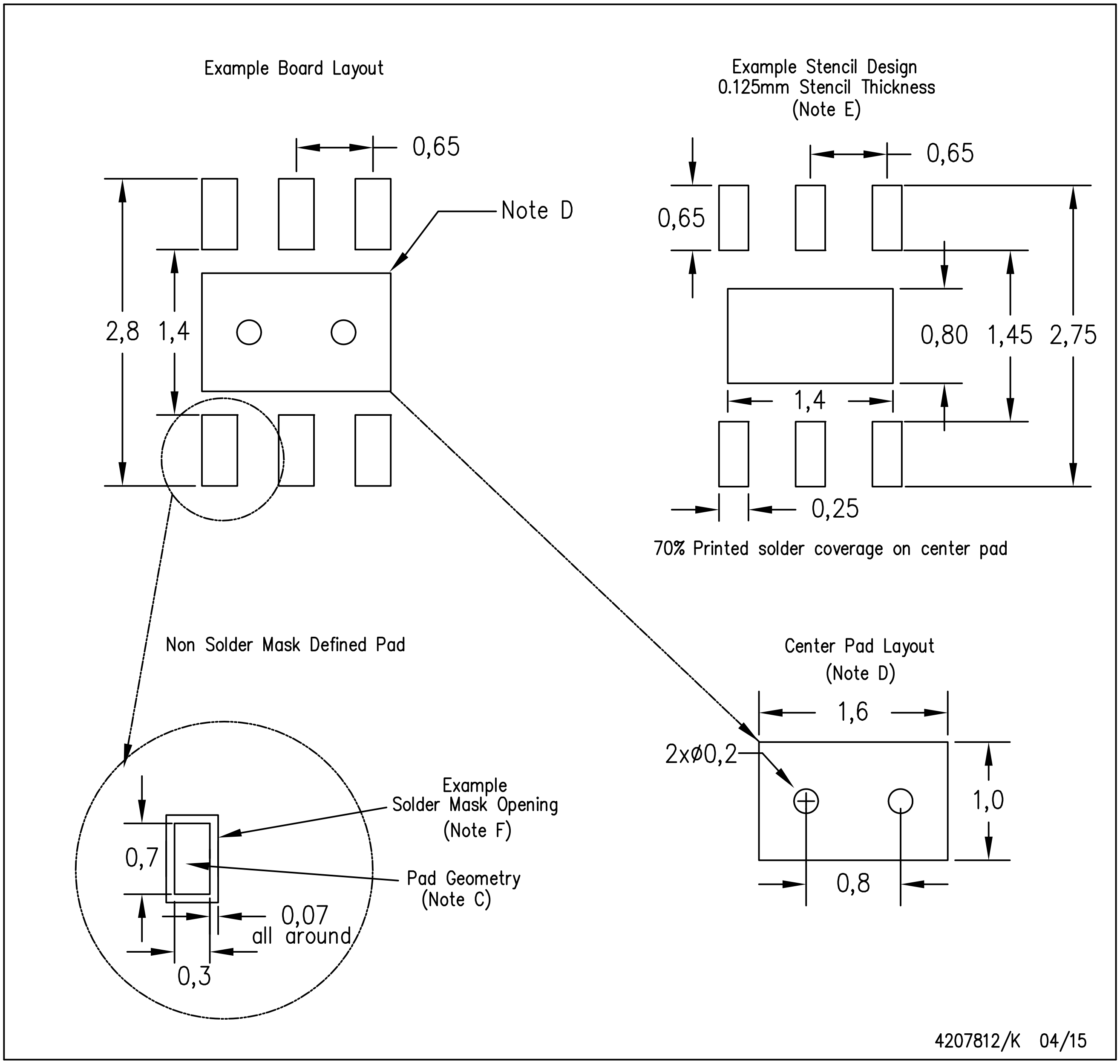
NOTE: All linear dimensions are in millimeters

DRV (S-PWSON-N6) PLASTIC SMALL OUTLINE NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for solder mask tolerances.